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Heat Sink Design Flow for EMC

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Abstract

This study focuses on establishing a heat sink design flow from an EMC perspective. The current EMC design on heat sinks is reactive rather than proactive. Mechanical engineers design heat sinks based on thermal constraints. The EMC team only becomes involved when there is a resonance problem in testing weeks or months later. In this paper, we develop a methodology including pre-design guidelines, post-design simulation, and correlation with lab measurements. An example is also provided to illustrate the methodology.

Biographies

Federico Pio Centola received his Laurea degree in electrical engineering from the University of L'Aquila, Italy in 2001 and the M.S. degree in electrical engineering from the University of Missouri Rolla in 2003. From 2001 to 2003 he has been with the Electromagnetic Compatibility Laboratory at the University of Missouri Rolla where he was a visiting scholar and a graduate research assistant. His research interests included electrostatic discharge, shielding and numerical simulations.
He has been an EMC instructor and consultant for Flomerics Inc. where he currently works as an Electromagnetic Application Engineer.
At Flomerics, he specialized in applying numerical simulations to solve EMC problems.

Alpesh U. Bhobe was born in India. He received his B.E. degree in Electrical and Telecommunication Engineering from the University of Bombay in 1996 and Ph.D. in Electrical Engineering from the University of Colorado at Boulder, Colorado in 2003. He was a Post-Doc at NIST in Boulder, Colorado. While at the University of Colorado and at NIST his research interest included the development of FDTD and FEM code for EM and Microwave applications. Currently, he is working as a Hardware Engineer at Cisco Systems, San Jose, CA where he is working on EMC design. Prior to joining Cisco, he was working as a Hardware Engineer at NVIDIA Corp. in Santa Clara, CA.

Philippe Sochoux received his B.S. and M.S. degrees in Electrical Engineering from Marquette University, Milwaukee WI in 1990 and in 1994, respectively. He joined Cisco Systems in 1998 and worked as an EMC and a Signal Integrity Engineer on the Cat6K family of Switches. Since 2001 he has managed CAD, Signal Integrity and EMC Design groups within Cisco Systems. Prior to joining Cisco, he was a Regulatory Engineer at U.S. Robotics/3COM in Chicago, IL. He is currently working towards his MBA degree at Santa Clara University, CA.

Jinghan Yu received his B.S. in Control Science and Engineering from Zhejiang University, China in 1998 and M.S. degree in Electrical Engineering from Louisiana State University, LA in 2001. He has been an EMC design engineer in Cisco Systems, Inc. supporting Cisco's GSBU and CSIBU for Catalyst 4000 series and Sypixx products since 2004. Before joining Cisco, he was an EMC engineer at Andiamo Systems, Inc.

Introduction

Operating frequencies and transistor integration of ICs have been steadily increasing ever since their invention. Also due to demand for multi-functionality, the I/O count and the power consumption of the ASICs also increasing. Heatsinks are placed on the chip surface to effectively draw the heat away and keep the components within the operating temperature range. However at higher speeds the dimensions of these metallic heat sinks are comparable to the operating frequencies and can worsen the EMI. Distributed grounding schemes have been implemented to mitigate the resonating EMI effects of the heat sinks [1-2]. However such implementations add to production cost and also consume real estate on the PCB. The radiation characteristics of heat sinks are studied in [3] but a comprehensive methodology to design heat sinks to mitigate EMI have not been developed (to the best of our knowledge).

To the best of our knowledge, there is little or no design input from EMC engineers during the initial design phase of heatsinks. Most of the EMC designs for heatsinks are left to pure luck. Mechanical engineers design heat sinks based on thermal and mechanical constraints. The EMC team only becomes involved when there is a resonance problem at the end of the design cycle, which could incur costs and production delays.

In this paper, we describe a proactive heatsink design methodology for ASIC operating at SerDes data rates. Based on typical heatsink dimensions given to us from the mechanical engineering team as a starting point, a large number of heat sink sizes (representative of typical midsize ASIC package sizes) were simulated and a database consisting in tables of their total radiated power for frequencies in the range of 1 – 15 GHz was created. These guidelines will serve as heatsink   In the early design phases of a heatsink, a mechanical engineer can vary several design parameters and still be able to achieve the required thermal performance. Using the EMI tables, the mechanical engineers will now be able to select the design that will minimize EMI at the frequencies of interest.

We verified our simulations with lab measurements and we considered various scenarios that may impact the accuracy of our results.

Unloaded Case

An ASIC has I/O busses running at speeds that are known well before its heatsink is designed. A typical ASIC may have some low speed interfaces (such as JTAG), medium speed interfaces such as source synchronous DDR interfaces (100-500 MHz), and several high speed SerDes differential pair busses running at various data rates (3.125, 6.25 Gb/s and 10.3 Gb/s). The proposed EMI design guidelines focus on the frequencies related to the SerDes data rates. Frequencies that are not directly related to the SerDes data rates are not taken into consideration because it is assumed that there is no source of energy at those frequencies (however, note that our methodology is flexible enough that information at any frequency can be extracted). As an example, if an ASIC has a SerDes I/O bus that runs at 6.25 Gb/s, the methodology considers the EMI values only at the fundamental frequency of the clock rate and its first few significant harmonics, namely 3.125, 6.25, 9.375 and 12.5 GHz. Should an ASIC have two distinct SerDes busses, then the frequencies related to both data rates need to be considered.

Mechanical engineers follow a set of design guidelines for heat sink dimensions to meet thermal requirements. During the design phase, they typically vary the fin height, heatsink depth and the number of fins (W in Figure 2). The fin height (H) varied from 0.12 to 0.92 inches. The depth (D) of the heatsink can vary from 0.61 to 1.96 inches. The width (W), which is driven by the number of fins on the heatsink, can vary from 0.61 to 7 inches. The mechanical engineers add fins by pairs, and each pair adds 0.25 inches to the width of the heatsink. For each ASIC package size, the number of fins varies within a range determined by the Mechanical Engineering team. The smallest package size can have a heatsink with 6 up to 18 fins, whereas the largest package size can have a heatsink with 16 up to 60 fins.

For the cases under consideration, the width of the first and last fins (0.04" in Figure 1) is always slightly larger than the other fins (0.025"). The spacing between fins (0.1") as well as the base of the heatsink (0.08") are always constant. The heatsink is made of extruded aluminum and is anodized.

In this paper we present the methodology for design of heatsinks for mid-size ASIC packages (0.91, 1.06 and 1.21 inches) operating at 6.25Gb/s. We studied the EMI performance of the heatsinks by varying the fin heights and number of fins.
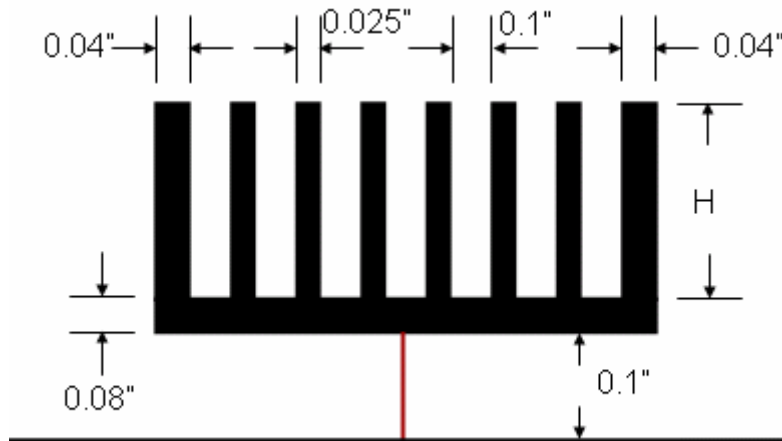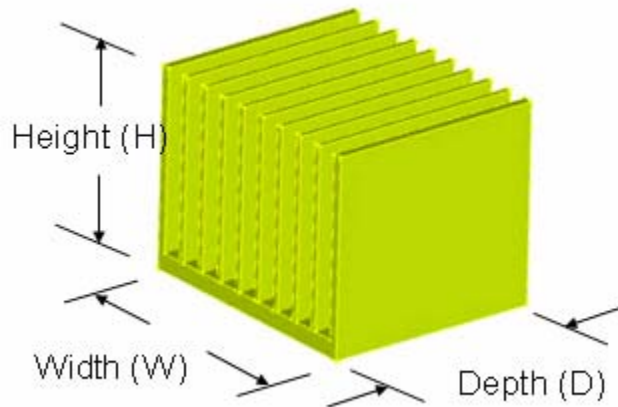
Figure 1 Heatsink dimensions

Figure 2 3D representation with dimensions

For these three heatsink depth sizes, a database of all possible heatsink dimensions (117) was created and each case was simulated. All the other parameters were held constant as indicated by the mechanical engineers.

The 3-D Transmission Lime Matrix based simulation software Microstripes [TM] from Flomerics was used for this study [4].   The mesh density, size of the computational domain and the simulation time were first varied until the solutions converged and stabilized. Various other simulation parameters (sub grid, type of absorbing boundary conditions, ground plane dimensions, distance between the heat sink top and the boundary conditions) were then tuned to reduce the simulation time while keeping a reasonable accuracy. The difference between the results obtained using the optimized model and full detailed model was less than 1 dB.

Simulations were run on two Dell ^{TM} dual quad-cores 64 bit Windows ^{TM} machines with 8 Gbyte of memory each. The Microstripes ^{TM} TLM solver is capable of parallel processing thus reducing the computational time. The number of simulations ran is 117 (for the unloaded cases only) and, on average, each simulation took 4 hours to complete. The total simulation time was approximately 234 hours on each Dell ^{TM} machines.

Due to the capacitive coupling, we modeled the ASIC source as a 1-V dipole source between the heatsink and the PCB ground plane as shown in Figure 1. The source which was located at the center of the heat sink had a 1-V flat spectrum in the frequency of interest (1 – 15 GHz). The distance between the ground plane and the heat sink was 0.1 inch which is typical height of a complete IC Package assembly. We varied the capacitance between the heat sink and the ground plane and did not observe any significant change in the results.

We considered the total radiated power radiating from heatsinks at specific frequencies to compare their relative EMI performances. Due to the enclosures in which the heatsinks reside, as well as the effects of other nearby heatsinks and metallic structures, the directivity of the radiation will change significantly and cannot be used effectively to compare relative performances of radiation from heatsinks.

The following example shows the design for a heatsink for a 1.06" size ASIC package operating at 6.25 Gb/s SerDes speed. For this heatsink we varied the fin heights in 3 steps at 0.12, 0.52 and 0.92 inches respectively. The number of fins was ranging from 10 – 34. The EMI values (in dB) are plotted for frequencies 3.125, 6.250, 9.375 and 12.5 GHz in Figures 3, 4, 5 and 6 respectively. From the plots we make the following observations:

- The fin heights do not make a significant difference at 6.25, 9.375 and 12.5 GHz (approximately 1dB variation).
- Varying the number of fins from 12 to 36 in pairs significantly changes the total radiated power of the heatsink (7 dB variation at 6.25 GHz) for 3.125 and 6.25 GHz.
- At 9.375 and 12.5 GHz, little variation in total radiated power is observed.
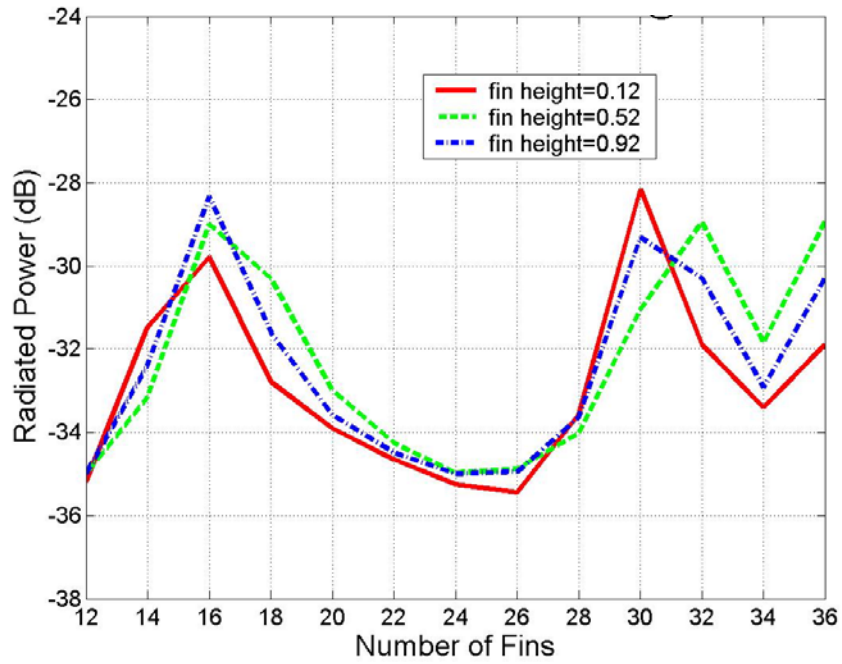
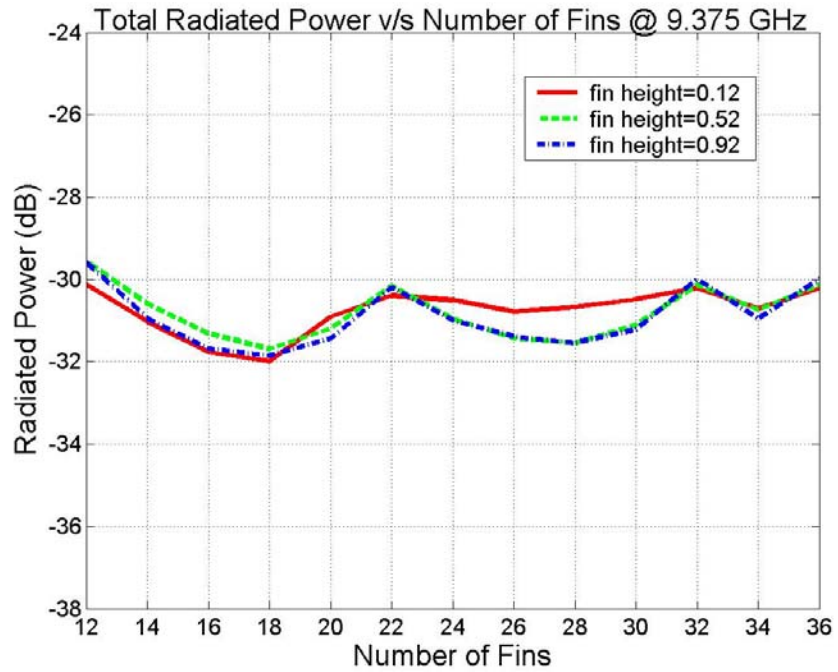Figure 3 Total radiated power v/s number of fins @ 3.125 GHz
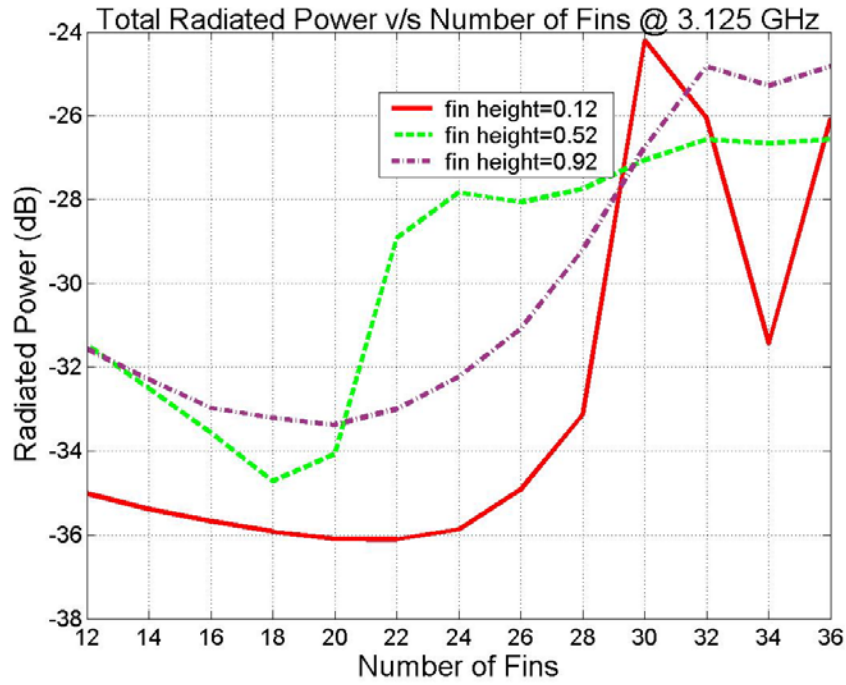
Figure 4 Total radiated power v/s number of fins at 6.25 GHz

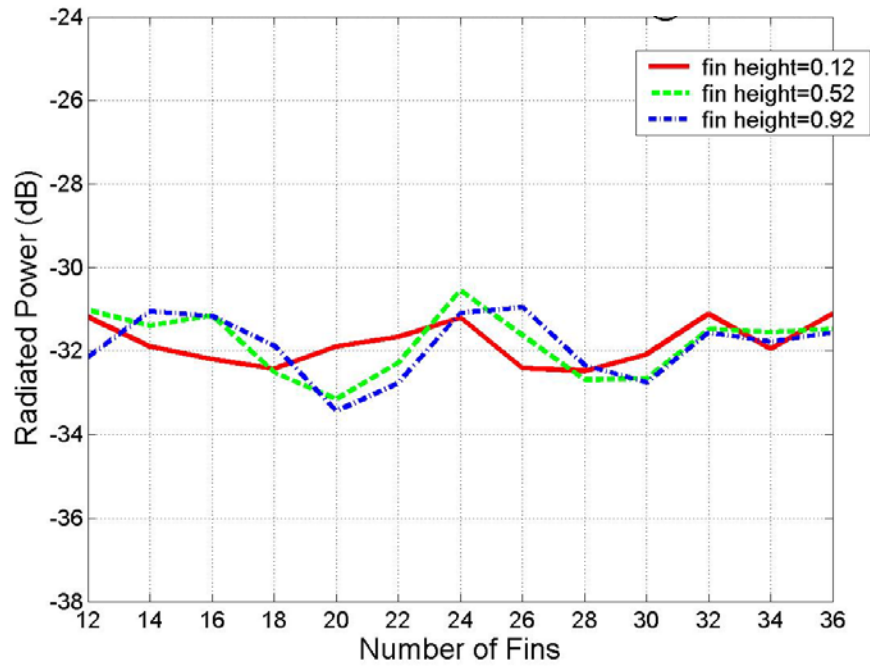**Figure 5 Total radiated power v/s number of fins at 9.375 GHz**

Figure 6 Total radiated power v/s number of fins at 12.5 GHz

As an example to illustrate the design methodology, the preliminary heatsink design from the mechanical engineer is D = 1.06 inches, fin height = 0.52 inches and number of fins = 14. From Figure 3 it is observed that the total radiated power at 3.125 GHz is -33.5 dB. Figure 4 depicts a

very strong resonance at 6.25 GHz with an EMI value of -28 dB. There is little variation in total radiated power At 9.375 and 12.5 GHz as seen in Figures 5 and 6 respectively.

Since it is still early in the design phase, the number of fins, width and base lengths can be modified to achieve the same cooling effectiveness while lowering the EMI from the heatsink.

The Mechanical engineer can propose to increase the number of fins to 20 and decrease the fin heights to 0.12" which would reduce EMI at 3.125 and 6.25 GHz. If this is not feasible, then further negotiations can take place between the EMI and mechanical teams to find a mutually acceptable solution. The depth D of the heatsink can be varied as well.

There could be cases where conflicts exist. For example, changing a dimension may decrease the total radiated power at one frequency but may increase it elsewhere. In this case, it is generally preferred to favor lowering the total radiated power at the higher frequencies since the shielding effectiveness decreases as frequencies increase.

Note that the EMI values can be obtained at any other operating frequencies from this methodology. For example, should the ASIC have an interface operating at 10.3 GHz then similar plots can be easily derived for all corresponding harmonics of the data rate. Should the ASIC have several SerDes data rates, then the EMC engineer may have to find the best solution space.

Correlation with lab measurements

The following correlations were done to validate the accuracy of the Microstripes ^{TM} software. The experimental setup is shown in Figure 7. We built a test fixture consisting of a heatsink above a 50×50 cm^2 copper ground plane. The dimensions of the heatsink were D=1", 10 fins and H=0.83". A SMA connector was punched through the center of the plate and its inner conductor connected to the center of the heat sink. The SMA connector provided a good 360 degree connection between the ground plane and the coaxial cable's outer shield.
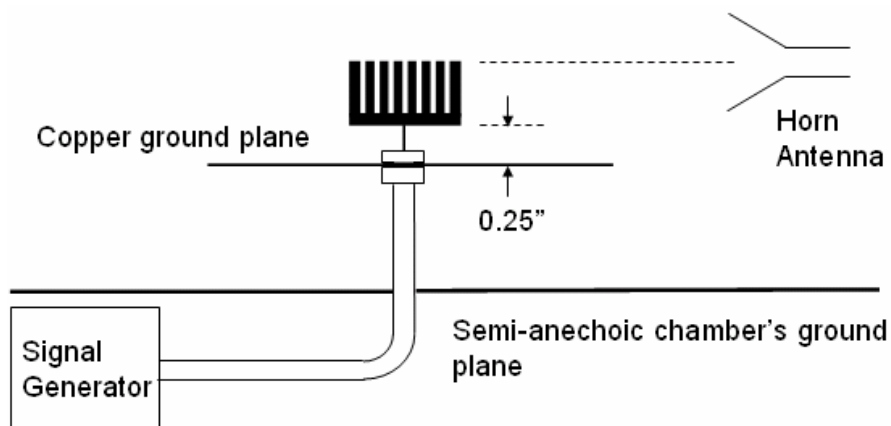

Figure 7 Setup for correlation measurements

The heat sink was excited at discrete frequencies ranging from 1 GHz to 15 GHz in steps of 500 MHz using a signal generator HP 83650L and the resulting field strength was measured using an

Agilent 7405A Spectrum Analyzer. A horn antenna was placed 3 meters away from the heatsink. The heatsink was rotated at 0, 45 and 90 degrees with respect to the horn antenna, where the angle shown in Figure 7 is 90. The height and the angle between the horn antenna and the heatsink were not changed during the measurements. The data was correlated to simulations using Microstripes [TM] and plotted in Figures 8, 9 and 10 respectively.
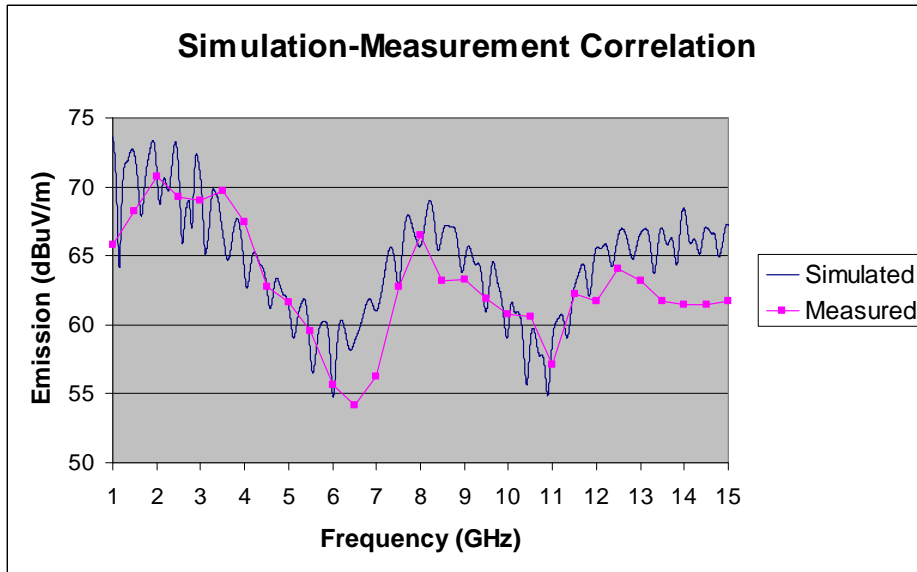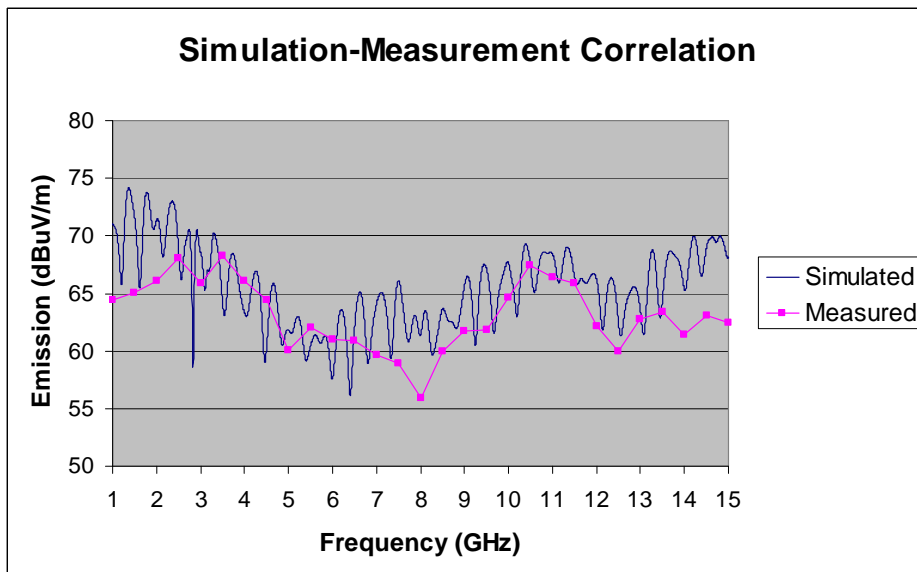

Figure 8 Correlation for 0 degree angle

Figure 9 Correlation for 45 degree angle

10
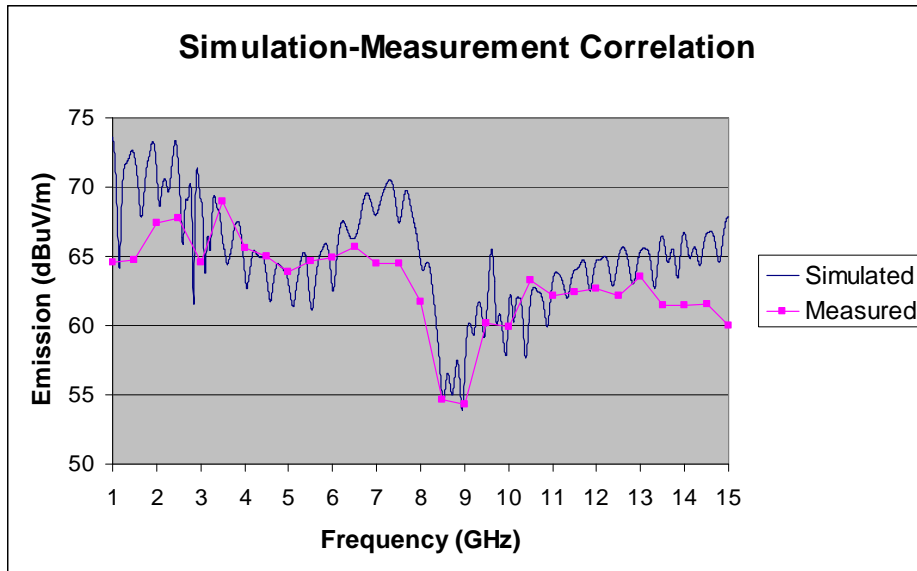
Figure 10 Correlation for 90 degree angle

The simulations and the measurements agree well in the three cases.

Effects of loading

In an actual application, additional heatsinks are placed near the heatsink under consideration. The additional metallic structures will influence the current distribution on the heatsink and therefore its total radiated power.

We started from an unloaded case and added a "picture frame" of perfectly conductive material at distances of 1, 3 and 5 inches from the heatsinks of base widths of 0.91 and 1.26 inches and studied the effects on the total radiated power (see Figure 11). This provided insight into how much the total radiated power will vary when the heat sink is placed within a chassis with other heatsinks nearby.
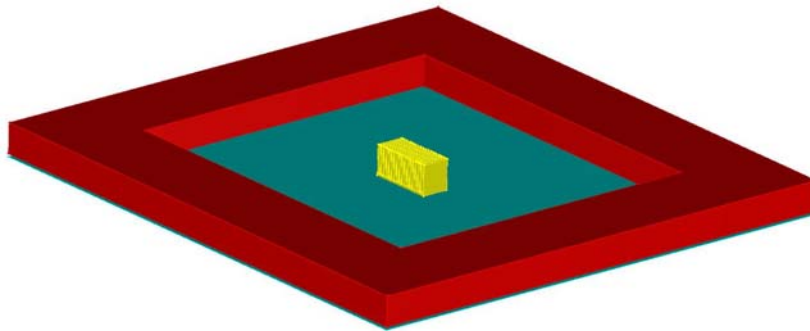
Figure 11 Picture frame of conductive material surrounding the heatsink

Figures 12, 13, 14 and 15 depict the total radiated power for various combinations of fins heights, picture frame heights and separations for a constant heatsink size (D=0.91")
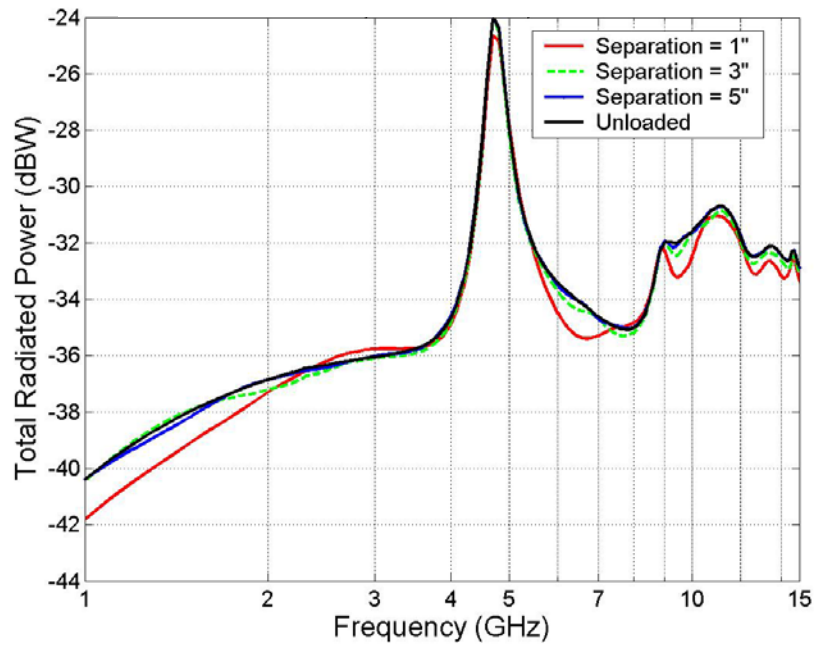

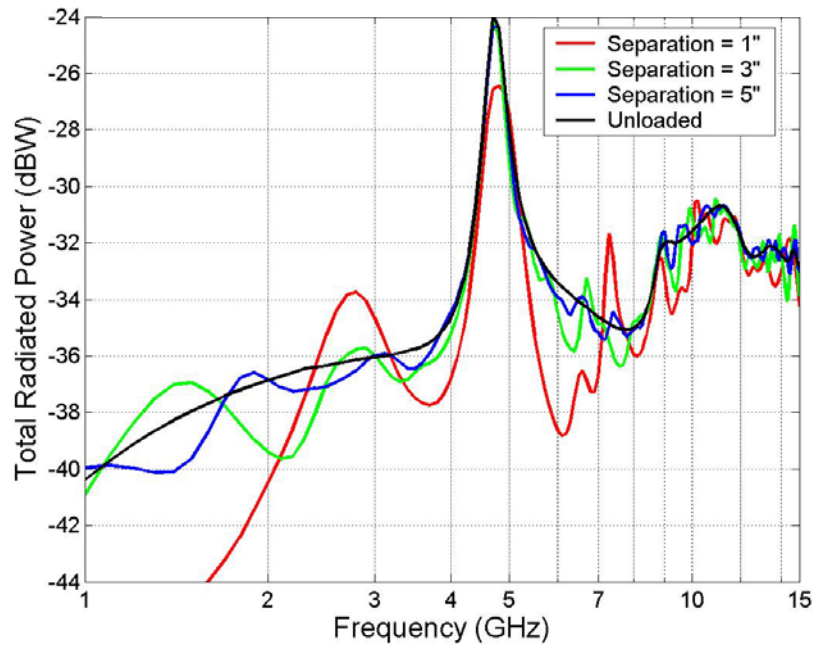**Figure 12 Fin height = 0.12", frame height = 0.2", size = 0.91"**

Figure 13 Fin height = 0.12", frame height = 1", size = 0.91"
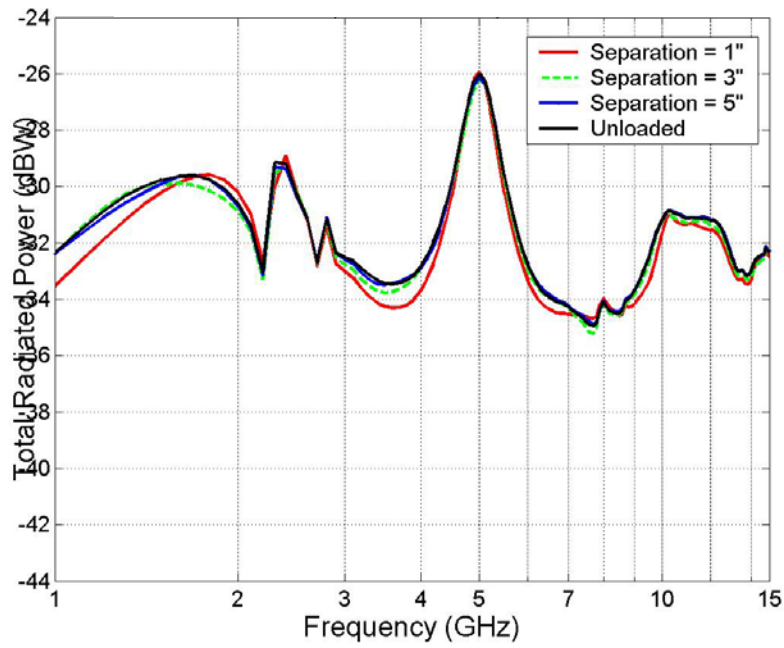
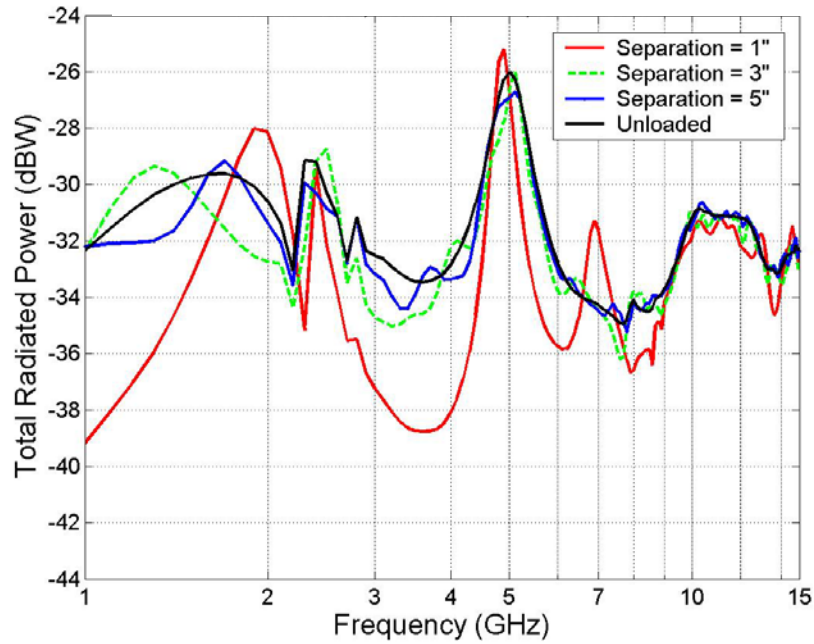**Figure 14 Fin height = 0.92", frame height = 0.2", size = 0.91"**

Figure 15 Fin height = 0.92", frame height = 1", size = 0.91

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Figures 16, 17, 18 and 19 depict the total radiated power for various combinations of fins heights, picture frame heights and separations for a constant heatsink size (D=0.91")
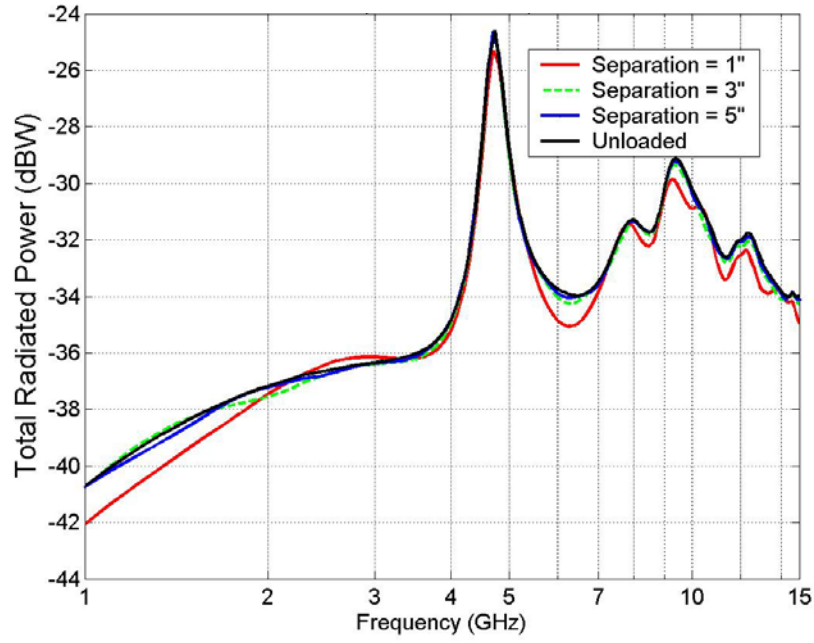
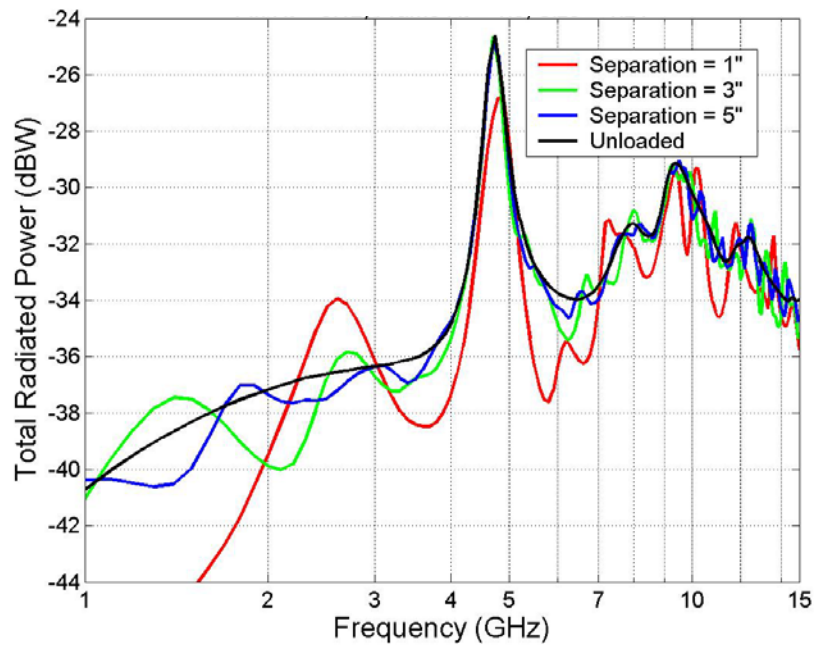**Figure 16 Fin height = 0.12", frame height = 0.2", size = 1.21"**

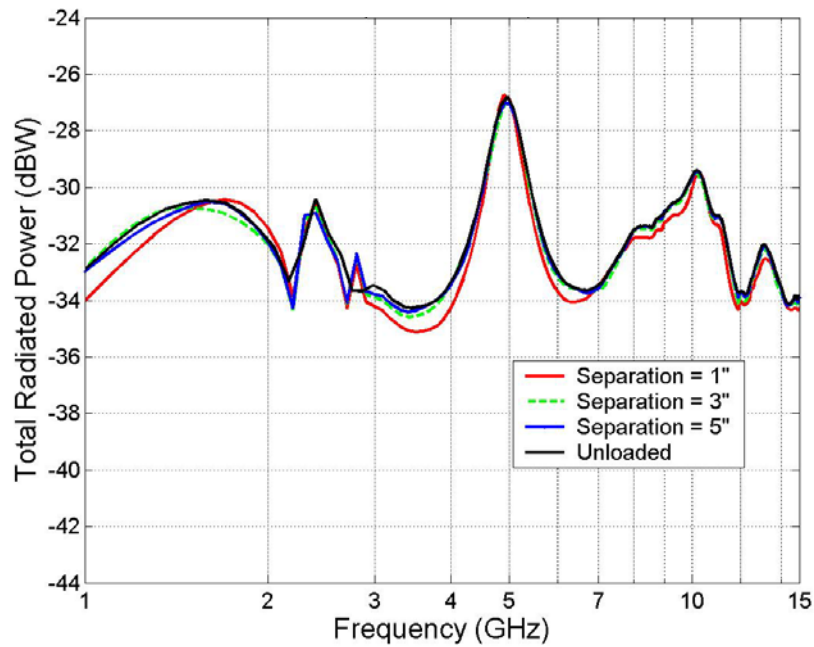**Figure 17 Fin height = 0.12", frame height = 1", size = 1.21"**

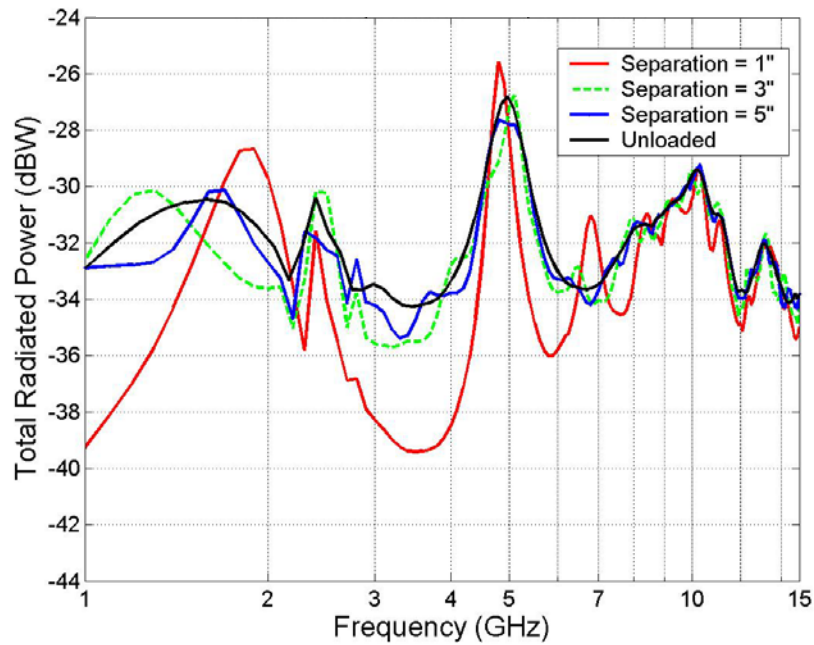**Figure 18 Fin height = 0.92", frame height = 0.2", size = 1.21"**

Figure 19 Fin height = 0.92", frame height = 1", size = 1.21"

The above simulation reasonably approximates the effects of having additional heatsinks nearby inside a chassis.

The following observations can be made:
- In all cases, there is little variation in total radiated power from the heatsink when the picture frame is further than 3 inch away from the heatsink.
- In all cases, there is little variation in total radiated power from the heatsink when the height of the fins is equal to or greater than the height of the picture frame.

However there are a very large number of possible combinations of heatsinks and it is not feasible to simulate each possibility. Therefore it is always recommended to perform a post layout simulation of the heat sink inside the chassis. A database from FloTherm ^{TM} [4] can be used for that purpose.

Conclusion

In this paper the authors have described a pre-layout heat sink design flow for EMC for ASICs operating at SerDes data rates. A large number of heatsink sizes were simulated to obtain their total radiated powers and the results were organized in a set of tables and plots. During the initial phases of the heatsink design, the EMC and mechanical engineering teams work together to select a set of heatsink dimensions that meet thermal requirements and minimize EMI.

Good correlations to lab measurements were obtained and discussed. The effects of loading the heatsink with a picture frame of conductive material were studied and discussed. The results provide good insights into how the total radiated power may vary when it's placed in its final configuration.

It is important to note that this research is preliminary and additional work needs to be conducted in this area. However, the authors believe that this methodology will be able to provide significant guidance for heatsink design for EMC.

References

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Volume 2, 13-17 Aug. 2001 Page(s):1341 - 1346 vol.2
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[4] Flomerics, www.flomerics.com

Acknowledgments

with lab measurements.