

Just Ask!

COMPILATION

HAPPY HOLDEN • JOHN MITCHELL • JOE FJELSTAD
TARA DUNN • HEIDI BARNES

Educational Resource Center



Throughout 2020, we asked you to send us your questions for Happy Holden, John Mitchell, Joe Fjelstad, Tara Dunn, and Heidi Barnes. You all had plenty of questions for these industry experts. The following is a compilation of your questions and their answers all rolled into this one document for easy reference.

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Just Ask Happy Holden



Ranking the Top Countries by Fab Technology and Production

Q: *In terms of overall PCB fabrication capability, how would you rank these countries in terms of technology and production, today and in 10 years: USA, Japan, Korea, Taiwan, China, Thailand, Vietnam, India, Germany, and the U.K.?*

A: I don't have a crystal ball, but here is my best guess:

Technology		Production	
Today	10 Years	Today	10 Years
Japan	Taiwan	Taiwan	Taiwan
Taiwan	China	China	China
Germany	Korea	Japan	USA
Korea	Japan	USA	Japan
China	Germany	Germany	Germany
USA	USA	Korea	Korea
UK	UK	UK	India
Thailand	India	India	UK
India	Thailand	Thailand	Thailand
Vietnam	Vietnam	Vietnam	Vietnam

Flexible Circuit Technology of the Future

Q: What do you think will be the next leading-edge technology for flexible circuits?

A: Disposable and wearable substrates, including paper.

Manufacturing Issues From a Designer's Viewpoint

Q: *What do you think are the biggest PCB fabrication/assembly issues from a designer's perspective?*

A: Communication and education! Designers need to know a lot about electrical circuits and their performance, but equally important is knowing how that circuit will be manufactured. But manufacturing is usually *not* part of a designer's education, so designers have to go out of their way to meet the manufacturing community and to communicate with them on issues related to their designs. IPC and SMTA make this type of training available, but a designer has to be aggressive in learning about manufacturing and all the do's and don'ts.

Monitoring Via Reliability on a Lot-by-Lot Basis

Q: *What is the best way to monitor microvia reliability on a lot-by-lot basis for high-volume production?*

A: What I recommend, and practice, is this: Do a thorough qualification of a fabricator using a HATS Qualification Panel (an IPC PCQRR-like panel) that includes an IPC D coupon resized for the runner on your SMT panel. Run these panel coupons through IPC-TM-650-2.6.27B and then TM-650-2.6.7.2 thermal cycles for 500 cycles. This is your baseline.

Then, by incorporating this smaller D coupon on all your boards' assembly runners—requiring each lot to have a plating process control coupon for X number of solder float tests at 288°C and then microsections to look at TH quality—you have a way of comparing that lot's performance to your initial qualification for that vendor. This should be redone each year and kept for records on each lot in case needed later.

The Future of 3D Printing

Q: *What is your opinion on the 3D printers that can utilize both conductive and non-conductive inks? Is this the future of PCBs?*

A: These 3D printers are evolving rapidly. A must is that the printer has the ability to use a number of different inks for the different components of a PCB, including the curing of the inks. At a minimum, that is:

1. Insulating substrate
2. Low-ohmic conductive ink
3. Non-conductive insulating crossover

As the equipment improves, solder masks, resistive/capacitive and solder paste inks, and even semiconductor inks would be nice. Currently, this is a quick-turn application for a few breadboards.

Whether this technology moves into being a source of operational electronics with sufficient reliability will depend on the innovations in creating future inks. Conventional PCB production continues to innovate to reduce their turnaround times and costs, forcing 3D printing to work that much harder on their solutions.

What Would You Change About the Industry?

Q: *If you could change/improve one aspect of this industry, what would it be, and why?*

A: TQM/continuous improvement (or Six Sigma) is a philosophy that has stuck with me since I was first exposed to it. I even taught the engineering aspects of TQM to every one of my engineers and techs; this included engineering statistics from the free NIST Engineering Statistics Handbook, as well as enhanced problem solving. Then, I would have my engineers teach TQM to their production supervisors, foremen, and leads, who would—with the help of the engineers and techs—teach it to all of the workers.

Continuous improvement is a strategy for success. And in our challenging industry characterized by innovation and change, continuous improvement and customer satisfaction are the only ways to survive and prosper.

Is PCB Fab Returning to the U.S.?

Q: *If the U.S. brings more PCB fabrication back to America, will it more likely be to the captive or contract shops?*

A: There are only a few captive fabricators in the U.S., but I hope that more OEMs will consider going captive as a way to ensure a source of supplies, lower costs, minimum lead times, and continuous improvements. OEMs should emulate the activities of Whelen Engineering, the emergency lighting company in New Hampshire that went captive and returned all of its PCB fabrication from China. Whelen cut its costs in half, improved quality, ensured its IP security, and cut weeks off their cycle time—all with an investment that had an ROI of fewer than two years.

But if PCB fabrication is to return to the U.S. from abroad, the majority will be to contract shops. If so, I hope that the OEMs will consider partnering with those contract shops and not treating their manufacturing "as just another commodity," just as they don't consider their proprietary circuits to be commodities. How circuits are manufactured is not like making soap; each PCB is different and deserves the necessary focus and care in its construction.

Electroless Copper vs. Direct Metallization

Q: *What are your thoughts on electroless copper vs. direct metallization?*

A: Both get the job done! Electroless copper is the more traditional method but may have some problems with its internal crystalline

strength when used with stacked microvias. Direct metallization is a newer technology that has come a long way in their development and is one of the few ways to successfully metallize polyimide film for flex.

Calculating Trace Temps in a Vacuum

Q: *For space applications (without air), how should we calculate external layer current-carrying traces against the IPC-2221 (formerly IPC-D-275) charts?*

A: I have never studied that, so I turned this question over to an expert, my friend Mike Jouppi, former committee chair of IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design. This standard will provide many answers to your questions. Mike wrote Chapters 22 and 23 in the seventh edition of the *Printed Circuits Handbook*, edited by Clyde F. Coombs and me.

Mike answered: I'm a mechanical engineer who worked as a career thermal analyst. The charts in IPC-2152 in almost all cases will be conservative (both air and vacuum environments). The vacuum is for space environments. The purpose behind these charts is misconstrued by most users. My intention when they were developed was to use these charts as a baseline for developing thermal models that could be used to better understand the actual temperature rise of conductors in actual designs, which I did for my own design purposes. The concept did not catch on.

There is a significant difference between the temperature rise in a conductor, tested per IPC-TM-2.5.4.1a, and most PWB design configurations. The reason is that most designs have copper ground and power planes that conduct energy away from the traces. In addition, most designs in space applications have a significant conduction path from the PWB through-bolted fasteners or wedge locks to a sink.

Since the question does not include IPC-2152, I would recommend researching IPC-2152 and accounting for the power dissipations in the traces in the thermal design. I also recommend accounting for the conductor power dissipation in all designs, especially if the designers are not familiar with sizing parallel conductors. Parallel conductors are easily managed with accounting for conductor losses (power dissipation). FYI: It was the power dissipation in conductors that motivated me to lead the development of IPC-2152.

Two-Layer Low-Speed PCBs

Q: *Why do many two-layer boards work in low-speed applications, signal integrity-wise?*

A: Two-layer boards, properly designed, will even work in high-speed applications! Even a single-sided board will. If the signal rise times are slow, signal integrity does not enter in the solution.

Resin-Filled Vias Without Voids

Q: *What is the best way to resin-fill vias without voids?*

A: I have not used this process a lot. In the past, partially filling surface vias with solder mask was sufficient. But now, with via-in-pad and stacked microvias, the filling process must be much more complete. Several machines on the market do this job very adequately and can be seen at the IPC APEX EXPO or SMTA International.

Integrating Design Processes With IEEE HIR

Q: *How will the PCB design process change to align with the IEEE Heterogeneous Integration Roadmap (HIR), and do you think this will happen?*

A: This is happening now! New EDA system tools are being created for the growing automotive complexity of autonomous vehicles. These tools can also be applied to other electronic systems,

such as mobile phones, 5G networking, medical, space, high-performance computing, and IoT. In the past, we called these chip-on-board (COB), multi-chip modules (MCM), and system-in-packages (SIP).

The new name is heterogeneous integrated modules (HIM). Heterogeneous was chosen because the future modules will incorporate not just IC chips, but also power devices, passive discretes, photonics, MEMS, sensors, antennas, and batteries. Systems-on-chip (SoC) will continue to be an activity, but as Moore's Law has flattened out, using multiple-cores processor chips w/memory is more cost-effective for greater computing power. As applications grow—and size, cost, and weight are more critical—HIM offers the best choice to move all of these elements closely together in a module.

A good summary paper on this topic was written by Paul Wesling at the SMTA 2020 Pan-Pacific Conference, "The Heterogeneous Integrated Roadmap: Enabling Technology For Systems of the Future," available from SMTA. For more details, the 584-page HIR is available at pwesling.com/hir. Its 23 chapters cover the full gamut of topics related to integrated modules, from today to 2033, for all major electronics markets.

Mechanically Drilled Blind and Buried Vias

Q: *Why are mechanical blind and buried vias popular in certain market sectors, yet they never took off in others?*

A: Blind and buried vias have their advantages. If only a few are needed, then they can be mechanically drilled. But in markets where miniaturization is essential, and the volumes are high, the laser is the drilling machine of choice.

PCB Design For EE Undergrads?

Q: *Do you think that PCB design should be added to an undergraduate EE curriculum?*

A: I think it should be an elective that engineering students could take. It is an essential part of the electronics development process, and a PCB design course will work well with a signal and power integrity elective.

Stacked Microvia Reliability Issues

Q: *Stacked microvias look good on paper, but they may have reliability problems. What are the best rules for designing stacked microvias to ensure a reliable PCB?*

A: The current best practice is stacking no more than two layers, and then moving over for the next buried or blind via or stacking two layers there. The stacked vias should never be stacked on any buried vias.

An IPC committee is currently testing various stacked via configurations to have a comparison for reliability and testing coupons and design. Hopefully, they will also get at the root cause of why stacked microvias are failing at their interface.

Flexible Circuits and 5G

Q: *Will flexible circuits be considered an integral interconnect for 5G technology?*

A: Yes. Flex circuits will evolve to fulfill the needs of 5G. What may change are the "connections" as millimeter-wave devices, and IIoT can be used to connect signals in 3D and at angles instead of using flex.

Ground Reference Planes

Q: *How important are GND reference planes in signals that are less than 50MHz, since 1/4 wavelength is about 30 inches?*

A: GND is an essential part of the circuit. The return path for DC is the lowest resistance, but for the AC part of the signal, it is the lowest inductance.

The Future of Mechanical Blind, Buried Vias

Q: Do mechanical blind and buried vias have a future?

A: Yes, especially for the newly invented VeCS technology, which uses a mechanical drill to gain the same density as laser-drilled microvias, but with higher reliability. For more information, read this series on VeCS technology by Joan Tourné of NextGin Technology, which ran in the April 2019 issue of *PCB007 Magazine*. (Also read Part 2, Part 3, and Part 4).

Routing BGAs With High-Speed Differential Pairs

Q: *What advice can you give for routing BGAs with high-speed diff pairs when the routing of these signals so often cuts off routing channels for other signals?*

A: This can be a complex topic, as there are a lot of circumstances that require consideration. My advice is to read a great book written in 2008 by Charles Pfeil when he was an engineering director at Mentor. "BGA Breakouts and Routing: Effective Design Methods for Very Large BGAs" is available for purchase from Amazon. Charles covers all of the options and boundary conditions that can come up, and he discusses the topic in the details that it requires.

The Proper Order of Design Techniques to Improve Connectivity

Q: *There are usually several ways to improve connectivity on any board (including HDI boards). But are there any general principles for which order these features should be added to achieve the best results?*

A: From a connectivity and density improvement standpoint, the use of blind vias (either drilled or lasered) offers the greatest gain, especially since the pitch of active components that drives density is shrinking. Next is the reduction of the diameter of via holes and smaller annual rings. Reducing traces and spaces comes next if you do not run into impedance and signal losses, and then blind vias. The final step is adding more layers.

Flexible Circuit Reliability Concerns

Q: *What are the key reliability concerns for flexible circuits moving to newer technologies, materials, and processes?*

A: The reliability concerns for flex are the same as for rigid circuits, with the exception of flexing. Material performance, conductor performance, external factors, usage, cleanliness, assembly, etc., are all important. Raza Ghaffarian of the Jet Propulsion Laboratory wrote a great review of flex reliability in the 7th edition of "The Printed Circuit Handbook," which I co-edited with Clyde F. Coombs.

Just Ask John Mitchell



Are IPC's Positions Dictated by Politics?

Q: *Why does IPC take positions based on politics? For example, IPC supported globalization when that was popular but now supports onshoring. Why not take positions that are best for the U.S. market?*

A: IPC works globally to support the growth of the electronics manufacturing industry. To this end, IPC invests in standards development, workforce credentialing programs, and, yes, advocacy. Championing sound public policies that empower our members to thrive has been a core mission of IPC since its inception. Our advocacy work on a variety of issues—environmental regulations, national security, and taxes—has helped the industry, but I acknowledge that there is still far more to do. That's why we have stepped up our investments in government relations to support the policies our members favor.

IPC does support global trade growth, but we also believe (and have always believed) that trade must be fair and that it should not come at the expense of strong, secure, and resilient supply chains. IPC has long advocated for robust U.S. manufacturing policies. Our position hasn't changed. What has changed is the political climate and the newfound understanding among policymakers that the U.S. government has neglected its electronics industry base. Our voice is being heard, and we are making headway. I'm hopeful that U.S. policymakers will prioritize the U.S. manufacturing base in the same way that other countries do.

A couple of final notes. First, IPC abides by a relatively simple principle. IPC only advocates for priorities that we would be willing to pursue in any other part of the world. Our goal is to empower our members to support policies that benefit them. Second, our members, through regional government relations committees, develop and track IPC's policy priorities. If you have an interest in getting involved, please reach out to me or Chris Mitchell, IPC's VP for government relations, as well as the author of ***The Government Circuit***, his column at I-Connect007.

Blurring the Lines of Technology

Q: *Advanced interconnection technology is blurring the distinction between circuit boards and ICs. What is IPC doing to address this trend?*

A: This subject has been raised a few times over the past couple of years—the "blurring of the lines" proposal, if you will. Some examples of technical similarity include copper line/space design range overlap, high-speed laminate materials, HDI, vias/stacks, and signal integrity control, to name a few.

Currently, while there are technical similarities shared between (a) IC packaging and (b) printed circuit board assembly and test (PCBA) market segments, at IPC, we do not share this viewpoint. We think that "blurring of the lines" messaging is confusing the industry. At this time, we are not seeing a significant number of reported cases where the lines are blurring between IC packaging and PCBA. Instead, we see IC packaging and PCBA manufacturing operating as two separate,

but very complementary, supply chain operation segments. While technologies may be shared, base materials, design rules, equipment sets, assembly, electrical test processes, and quality/reliability assessment requirements can be different.

It appears the driving force may be that some EMS providers are attempting to extend their service offering beyond PCBA/test to also include IC packaging assembly/test. From an EMS perspective, this is attractive because it allows them to benefit from their manufacturing infrastructure economies of scale (EOS) and offer higher value to OEMs with increased margins.

At IPC, we continue to lead and serve the electronics manufacturing industry. Our core consists of standards, education, training and certification, and government advocacy. In the future, if this migration occurs and if EMS providers offer back-end OSAT services, IPC's network of members and standards development processes is positioned to drive new standards and technology adoption as needs arise. IPC standards can be applied to both PCBA assembly and test and IC packaging assembly. IPC "factory of the future" activities, including the connected factory exchange (CFX), are driving digital factories and modernization across the supply chain.

Plans For Knowledge Transfer?

Q: *Is IPC going to promote a plan for knowledge transfer from retiring engineers to young engineers?*

A: IPC is committed to providing engineers new to the electronics industry with the tools and resources necessary for a successful career. We have approached this at both the individual level with IPC's Emerging Engineer Program and at the group level with events such as the Industry Intelligence series and other webinar events. Recognizing that oftentimes our retiring engineers take "the secret sauce" with them, IPC is working with both groups to ensure continuity.

A Global Book-to-Bill Number?

Q: *Why doesn't IPC publish a global book-to-bill number?*

A: The book-to-bill number requires a sufficient number of company participants. Historically, we have had robust participation in North America. We are working with our members in Europe, Asia, and elsewhere to explore a global book-to-bill number in the future.

Advice on Selling Tech in Asia

Q: *How do you anticipate, either now or after the election, the means by which we could offer (i.e., sell) technical assistance and/or products to clients and organizations based in mainland China and other countries in Asia?*

A: The tensions between the U.S. and China are likely to persist regardless of the outcome of the 2020 elections. There is broad and bipartisan support among federal policymakers for a more oppositional U.S. stance toward China, and China thus far has proved willing to go tit-for-tat. All companies that do business with or in China will need to be vigilant in keeping abreast of legal restrictions and tariff changes.

IPC has three wholly-owned subsidiary companies in Asia/Greater China. These subsidiaries offer IPC products and services across the region, including technical consulting services, qualified manufacturer listings, and process audits under IPC's Validation Services Program. For further information on these services, contact Evelyn Cui, Greater China operations director.

Greenfield Capacity in North America?

Q: *What do you think will drive more greenfielding/new PCB capacity in North America? And when do you think we will see a new PCB facility built from the ground up to meet the demand in North America for locally built PCBs?*

A: Greenfield opportunities appear to be highest for high-mix, low-volume PCB manufacturing within North America. Customers requiring special supply chain security measures, rapid turn early-stage co-development, or increased new product introduction capability are well suited for North American operations, situated close to North American OEM facilities.

Operations having high levels of automation may also be attractive for North America. North American PCB operations have not historically been utilized for high volume commodity PCB supply. Instead, these plants are best utilized for their higher complexity skill, new product introduction expertise, design for manufacturing design reviews, and high-quality yield production.

As for when we will see a new PCB facility built in North America: Suppliers that are considered a trusted source are likely to be able to service special supply chain security requirements being issued by North American governments and military organizations, so now is absolutely feasible for new PCB facilities to be built.

Emerging Engineers and Managers

Q: *Does IPC have an interest in emerging managers, as well as emerging engineers?*

A: In our highly competitive industry, the knowledge and skillsets of staff directly responsible for client services and program management can make or break a company's bottom line. To help emerging managers, IPC offers a Certified Electronics Program Manager (CEPM) Training and Certification Course. Taught by an IPC-certified industry expert with 30 years of experience in the field, the six-week program utilizes interactive webinars, on-demand recorded training, job-specific exercises, and team projects to facilitate mastery of the key business and technical concepts required of program managers in the electronics industry.

We're currently exploring an emerging manager mentor program in addition to the CEPM program. More details to come on this program by Q2 2021.

Just Ask Joe Fjelstad



The Occam Process

Q: *Is the Occam process an early version of chiplets, placing chips first in assembly?*

A: There have been a number of speculative and prospective chip first package solutions over the last 15–20 or more years. GE, Intel, and others have shown ways of interconnecting chips in packages by plating and then socketing or surface mounting the resulting components on PCBs using solder as almost everything still is today.

Chiplets are a more recent manifestation where chips are tiled and interconnected in mosaic form around the edges using solder. Occam was envisioned as a way to eliminate solder from the manufacturing process by reversing the manufacturing process. That is, building a "component board" comprised ideally of packaged ICs, all having a common grid pitch for terminations and which have been tested and burned in. Circuits are then built up onto the component board as if it was a basic PCB substrate. The component board substrate can be of almost any material because soldering is not required. Aluminum is suggested because it is an excellent thermal conductor and has a CTE near that of copper. Having all components with a common grid makes routing very efficient, and layer counts can drop significantly. Because there is no soldering, there is no unintended thermal damage to components or assembly. With the reduced number of steps, the assemblies should be much less expensive.

The Land Warrior Project

Q: *Was your Land Warrior project ever implemented?*

A: The Land Warrior system was developed and fielded by a Pacific Consultants team of 40-some engineers and technicians (after winning a design competition against three top-tier military systems contractors). The contract was managed by Exponent. Approximately 100 systems were built and demonstrated in a war games exercise at Fort Polk in 2000. It exceeded all expectations. Land Warrior development has continued in one form or another since and has seen service in conflicts since 2001. The name Land Warrior was changed to Nett Warrior in 2010 to honor Medal of Honor winner Robert B. Nett. For more information, click here.

Optimum Thermal Via Farm Copper Plating

Q: *What is the optimum copper plating thickness for thermal via farms?*

A: The question is an important one, but it is not easy, or perhaps even possible, to provide a hard answer to the question as there are many variables to consider. How many vias? What is their pitch? What size (diameter and depth) are they? How much heat needs to be removed? Are they filled with copper or just hole-wall plated? Are they independent features or connected en masse to a copper plane? In a sense, the best answer is perhaps that they collectively resemble the extent possible a copper slug. I would suggest that some thermal modeling of the solution be performed beforehand.

That said, there are some interesting technologies being rolled out at the present time. One is from the Silicon Valley company, Kuprion, which has developed a nanoparticle "copper solder," which appears worth considering as an alternative to plating vias.

Automotive Conformal Coatings

Q: *Of all the various conformal coating materials available, what would you recommend for automotive electronics?*

A: The question indicates knowledge that there are different conformal coating options out there. It is not really possible to pick a definitive solution without knowing more detail about the application specifics. In general, a conformal coating is used to seal the electronics from the environment, but there may be other demands/desires placed on the material in terms of "reworkability" and/or special environmental and/or chemical resistance requirements. I'd suggest creating a list of desired qualities and performance needs/requirements, along with ease of use, rework-ability and submitting them to the various vendors for their responses. The vendors can often serve as good and reliable resources for answering questions you might not have thought to ask.

Standardized Grid Designs

Q: *Will standardized grid designs ever come to fruition?*

A: I am old enough to know that once upon a time, the electronics industry actually had a standardized grid. It was 0.100". It was the natural by-product of the fact that most early electronic packages were dual in-line packages (DIPs), and nearly all of the first DIPs had their leads on 100-mil pitch (the Soviets and Eastern Bloc nations went with 2.5 mm rather than 2.54 mm or 0.1 inches). It was a natural default, and 100-mil grid pitch design was common and the standard even today; think of hobbyist's bread boards, which are on a 100-mil grid.

Those halcyon days were disrupted as pin counts rose, and surface-mount technology took the stage to help manage the explosion in package pin counts. Then there was the "80% rule" for package leads that took effect to provide a defined roadmap for following generation component lead pitch. Thus, today (ignoring inch-based devices), we have 2.5 mm, 2.0 mm, 1.5 mm, 1.25 mm, 1.0 mm, 0.8 mm, 0.65 mm, 0.5 mm, 0.4 mm, etc.

Area array technology offered the opportunity to return to a standard grid, but the 80% rule was applied instead, which is a great pity from my perspective. Instead, what might have been done is to agree on a common base grid pitch and depopulate to the pin count desired. Everything gets easier again—no more burning off layers of circuits to accommodate escapes and differing grid pitch components. It is an easy way to return to standardized grids. All that is necessary is for component packagers to offer every component with terminations on a standard grid. My suggestion is 0.5 mm because that is where component soldering yields start to fall off.

Is it possible to return to the standard grid? Absolutely. It is more a question of customer demand for such and package foundries' willingness to do so. It could save billions of dollars annually, according to my back-of-the-napkin calculations.

Just Ask Tara Dunn



Reshoring of High-Volume IC Substrate Production

Q: *Do you think IC substrates (BGA, CSP, flip chip, etc.) will ever be produced in high volumes in the U.S.? The Asian capacities are currently full and expanding.*

A: That's a great question. First of all, I think the concept of high volume is relative, and the definition may be something different for everyone. There is quite a bit of effort ongoing at this time to bring this technology back to North America. These endeavors are exciting for the industry and important to the Department of Defense and its mission of providing security for the U.S. These "reshoring" efforts have begun with limited capacity in comparison to the overall volume in the market, but as development progresses, we might find that North American manufacturing may be more competitive than we realize, thus drawing additional production back to North America.

The Thickest Flex Layer Available

Q: *What is the maximum thickness of a single flex layer, not just for a test vehicle but a flexible circuit layer manufactured commercially?*

A: There are a lot of different ways to answer this question. There are examples of flexible circuits being manufactured with 10-ounce copper bonded to dielectric. In this case, the "body" of the flexible circuit is typically etched to a thinner copper for flexibility and leaves the contact fingers with the thicker copper.

Looking at what laminate thickness are commercially available for fabricators, Dupont provides a laminate with 0.005" dielectric, bonded on each side to four-ounce copper, with 0.003" adhesive. That is an extremely thick laminate, at 0.0222". The most common flexible laminates are much thinner, with half-ounce or one-ounce copper bonded to 0.001" or 0.002" polyimide, resulting in thicknesses of 0.0024–0.0068", depending on adhesive requirements, dielectric thicknesses, and copper weight.

Fabricator Feedback to PCB Designers

Q: *Why don't flex and rigid fabricators provide more feedback to designers, especially if it's not good design and engineering work?*

A: This is an interesting question. My initial tongue-in-cheek reaction was that fabricators are not often asked to provide feedback. In my experience, fabricators are very willing to provide feedback on PCB design, flex or rigid, and that conversation is something that I would always encourage. These conversations are always more impactful when fabricators are involved early in the design process.

Discussions about stackup and design for manufacturability concerns—especially for designs pushing the limits on multiple different fabrication parameters that require trade-offs—or for designs with concerns about flexibility and robustness of a design are critical and can have a significant impact on cost and reliability.

Unfortunately, with the rapid pace of the industry, those conversations often happen only after a design is complete and sent to the fabricator for manufacturing. At that point in the process, time deadlines often loom, and it can be time-consuming and expensive to rethink that design to improve manufacturability.

I would challenge both designers and fabricators to take a step back and find ways to better communicate about DFM issues early in the process. There is a lot of great content available, but that cannot replace conversation, or even a facility tour, as a learning tool. Reach out to your fabricators early in the design and ask their opinion.

Flex and Rigid-Flex DFM Advice

Q: *Flex designers don't seem to pay much attention to a fabricator's limitations. What would you advise new flex designers as far as DFM?*

A: Knowing your fabricator's limitations is important, whether that be for rigid PCBs or flexible circuits. And this is especially important with flexible circuit designs. There is a wide range of capabilities across the supply base. Some focus on simple flex, single-sided, double-sided, or low layer counts. Others focus on high-complexity technology, including complex rigid-flex and bookbinder technology. It is critical to really understand your fabricator's capabilities and design to those capabilities.

As important, in a general sense, is to understand that flexible circuit fabrication, while similar to rigid PCB fabrication, has subtle differences that impact things, such as minimum line width and space and hole size. Not only are the layers thinner, with considerations needed for handling and processing, but the materials themselves are less stable than traditional rigid materials, with subtle shifts in material size through processing and changing environmental conditions. These things impact registration during fabrication, and feature sizes that may be common in rigid PCB fabrication may not be the "standard" for flexible circuit designs. Communication is king.

The Future of LCP as a Flex Substrate

Q: *Will the surge in liquid crystal polymer use for cellphone antennas "trickle down" and allow LCP to be used more often as a conventional flex substrate?*

A: That is a great question. I am certainly seeing an increase in conversations about LCP materials and their benefits not only in cellphone antenna applications but also in medical applications requiring biocompatibility. As with anything cellphone related, there will be a handful of fabricators that use the materials in high volume and over time that trickles through the supply chain. In the case of LCP materials, the fact that there are specialized fabrication parameters that manufacturers need to employ when processing LCP and that the conventional flex substrate market is robust leads me to believe that while we will see an increase in demand for LCP, the material likely won't displace polyimide as the mainstream flex substrate.

Maximum Number of Flex Layers

Q: *What is the outside maximum number of flex layers that have been used in an actual product?*

A: I could answer with a number based on just my personal experience and memory, but I think it is important to include some context along with that. The key issue with the number of layers in a flexible circuit is the ability for that flex to function in a reliable manner, over time, as intended, whether that be flex-to-install or in a dynamically flexing application.

"The flex that didn't flex" is something we joke about, but it happens more often than one would think. I have seen three-layer flex circuits that were not flexible enough to be bend around the corner of the package, and I have seen 12-to-14-layer flex circuits that functioned beautifully in high-flexing environments. Key considerations to improve flexibility such as material selection, using unbonded layer construction and cross-hatch copper patterns vs. solid copper can have a significant impact on performance.

Involve your fabricator early in the design cycle; they have a lot of knowledge to draw from on how to best meet your overall flexing requirements.

Just Ask Heidi Barnes



EMC Failures

Q: *We waste a lot of time with EMC failures. It's constant. What are your thoughts on EMC?*

A: Maybe it is too simple, but if one does a great SI design, then all the energy goes from Tx to Rx and there is no radiation. It's the same with PI: if one does a great PI design, then all the energy goes into delivering power to the load and not feeding EMC resonances. The biggest culprit is often the layout of the return path, which is trivialized in schematics with a simple ground symbol that magically connects all grounds together. As EMC/EMI expert Dr. Bruce Archambeault is often heard saying, "Ground is a place for potatoes and carrots."

In electronics, we have return current paths. Obviously, it is never that simple in engineering and one always needs to make trade-offs. I find that even the simplest of EM simulations can start to provide significant insights into ways of reducing potential EMC problems from resonances and crosstalk.

'Hot' Engineering Disciplines of the Future

Q: *In the future, what EE disciplines (SI, PI, EMC, etc.) are going to be the most in demand?*

A: I am partial to power integrity (PI) because I am now 100% invested as the power integrity product owner for Keysight's PathWave PI solutions. Signal integrity (SI) is challenging, but even SI needs PI to work. PI is the foundation, and to still find so many conflicting design rules and industry arguments on best practices makes it likely that we will see a growing demand for PI engineers to define best practices and better standardize the industry.

I also like to have an ideal approach to EMC that says if one does the SI correctly so that all Tx power goes to the Rx, and if one does PI correctly and the power delivery is matched to the load, then there should not be any energy going into EMI/EMC. This is rather simplistic, but it does highlight the benefit of good PI and SI designs to reduce the need for additional hardware to mitigate EMC problems.

Attracting New Designers and Engineers

Q: *Many of my colleagues in PCB design and engineering are retiring soon. We have a few new, young EEs in our company, but not many. How can we attract more young people to this career that I love?*

A: I have high hopes that the recent investment in STEM activities for high school and elementary level students will lead to a growing interest. Also, the success of the commercialization of the space industry is very inspiring for the next generation. In terms of filling immediate needs, I still remember my most favorite things when starting work with my first job at Hewlett-Packard. They were a fully supplied electronics stock room, state-of-the-art test equipment/computers, and an engineer's machine shop. Simply put, it was having the engineering tools to be creative and think outside of the box. Just as important for attracting and retaining engineers are the people, with social activities and projects that make it easy to network across organizational boundaries.

Biggest Challenge for Today's Design Engineers

Q: *What do you consider to be the biggest challenge for PCB design engineers today?*

A: I would have to say impedance, and the fact that electrical signals with fast digital edges and low voltages are much more sensitive to this than ever before. Designers need to start thinking in terms of return paths and impedance to better understand how layout can have an adverse impact on PCB performance. The engineering trade-offs can be quite complex between performance, cost, and risk. Innovative solutions often benefit from the ability of EDA tools to do pre-layout "what-if" simulations using measurement-based models and manufacturing tolerances.

Most Rewarding Part of a Design Engineer Career

Q: *What is the most rewarding part of your job, and your career overall?*

A: Finding an elegant solution to an engineering problem and then sharing with colleagues through the publication of a technical paper. Engineering tools like PathWave ADS make it possible to look at an electronic engineering problem from the simplest rules of thumb to the complexity of full electromagnetic (EM) simulation. In the process of looking at a problem from more than one direction, it is possible to identify the critical parameters and develop a more elegant solution. Conferences like DesignCon make it possible to publish papers that not only document the engineering solution, but also provide the flexibility to go into the details of applying the solution to real-world applications.

China vs. U.S. EE Graduation Rates

Q: *Do you think China is still graduating 5-10 times more "electrical engineers" than the United States?*

A: I don't know the exact statistics, but I can say that in China, they are very proud to talk about their government leaders with technical engineering backgrounds. Engineering is considered a very well-respected career path in China. In the U.S., I think the push for STEM is having an impact at the elementary school level. I also like to think that the recent success of the commercialization of the space industry in the U.S. will inspire a surge of interest in engineering.

NASA's Silver Snoopy Award

Q: *I've never heard of the Silver Snoopy Award. How does someone win one of those?*

A: The Silver Snoopy Award is a special award given by NASA astronauts to men and women contributing to spaceflight safety and mission success. While working for NASA at Stennis Space Center in Mississippi, I had the privilege of working on hydrogen fire and gas detection systems to improve the safety of operating liquid hydrogen and liquid oxygen rocket engine technology. Growing up, I used to see one of the original Silver Snoopy Award pins on display at the ice rink in Santa Rosa, owned by Charles M. Schulz. Charles Schulz designed the Snoopy pin during the Apollo space program, and every pin flies in space before it is awarded to the Silver Snoopy recipients. It was a proud moment when I had the opportunity to let "Sparky" Schulz know that one of his local skaters had gone on to be an engineer for NASA and receive the Silver Snoopy Award.



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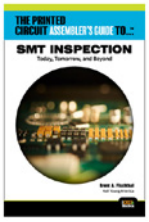


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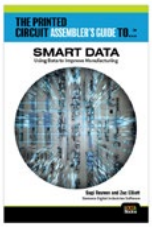
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