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## Current Trends in Signal Integrity

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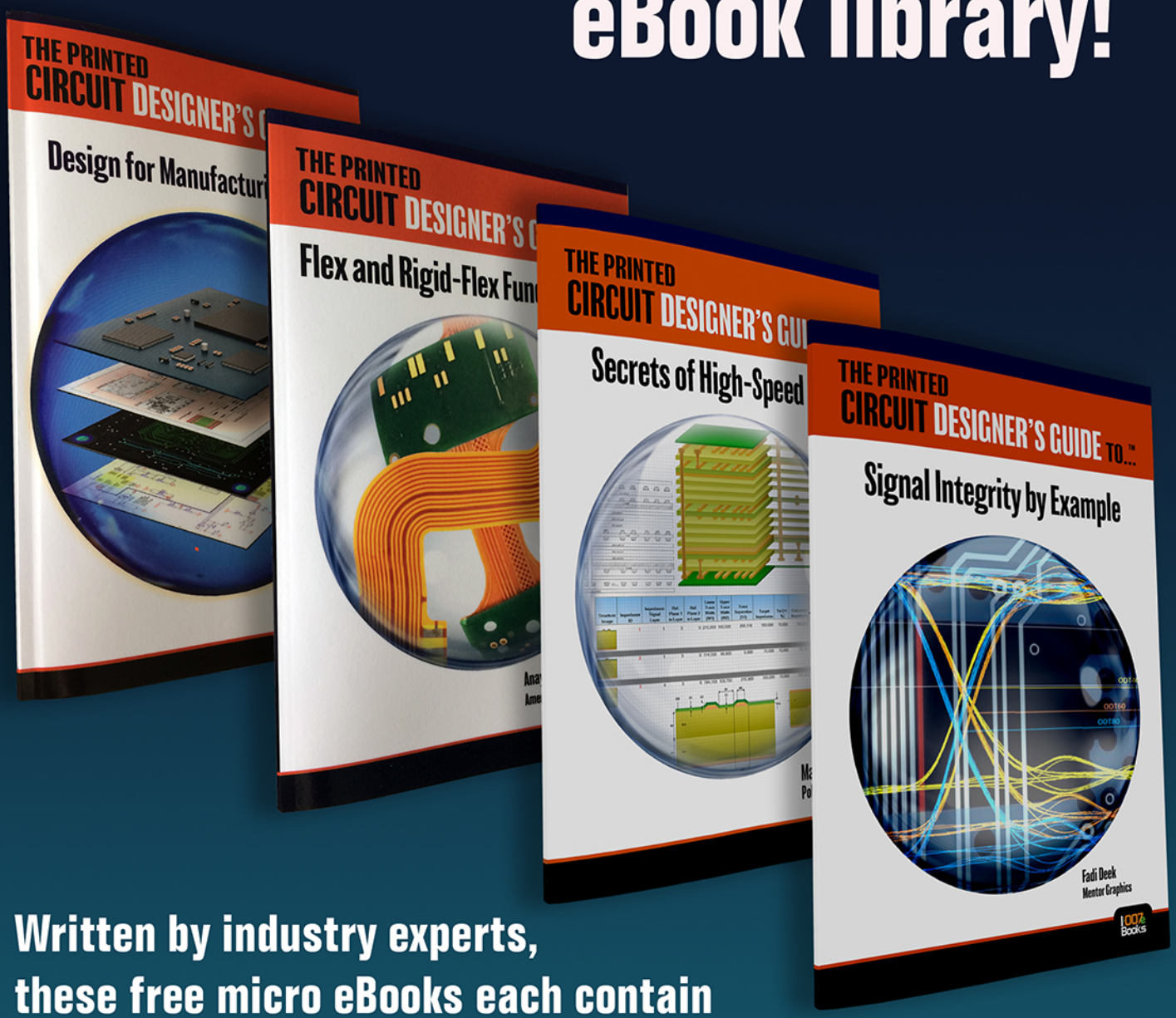


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# “If you care about signal integrity, you are sure to pick up a few nuggets of insight from this new eBook.”

**Eric Bogatin**
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This FREE micro eBook, written by signal integrity engineer Fadi Deek of Mentor, A Siemens Business, will benefit anyone interested in identifying the problems, root causes, and solutions surrounding electronic transmissions.

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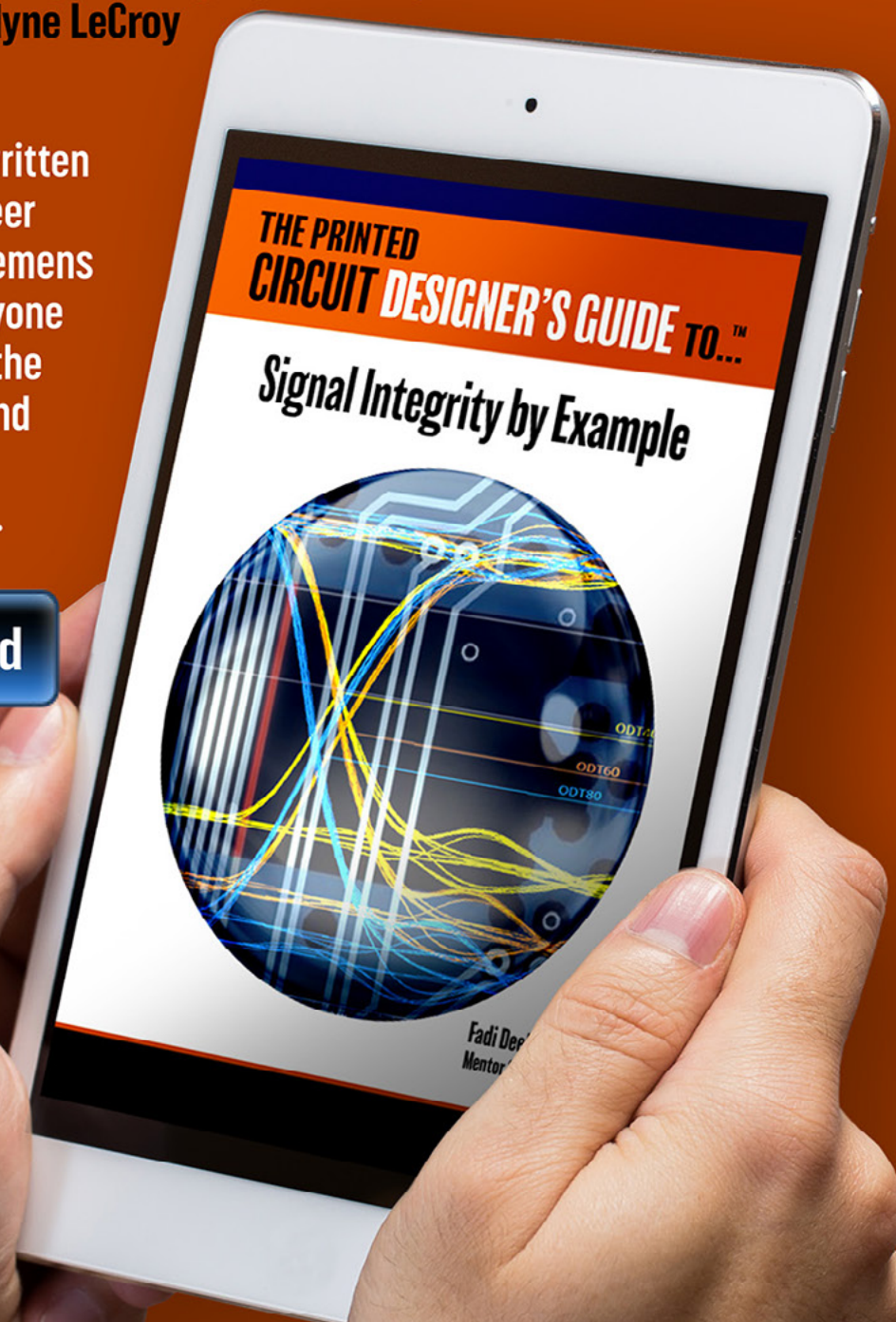


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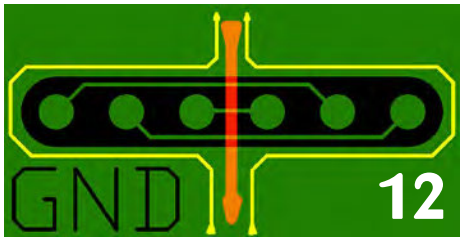




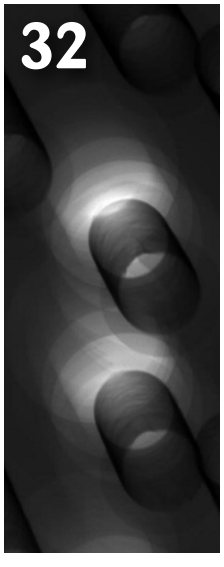


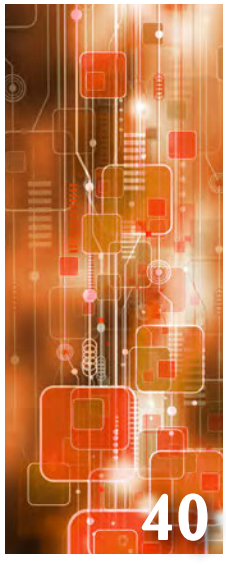


# Current Trends in Signal Integrity

If you think signal integrity is just a design problem, think again. As board features get smaller, as speeds get faster, and as more is expected from everyone in the supply chain, signal integrity should have everyone's attention. This month, our experts explain why.

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### COLUMNS



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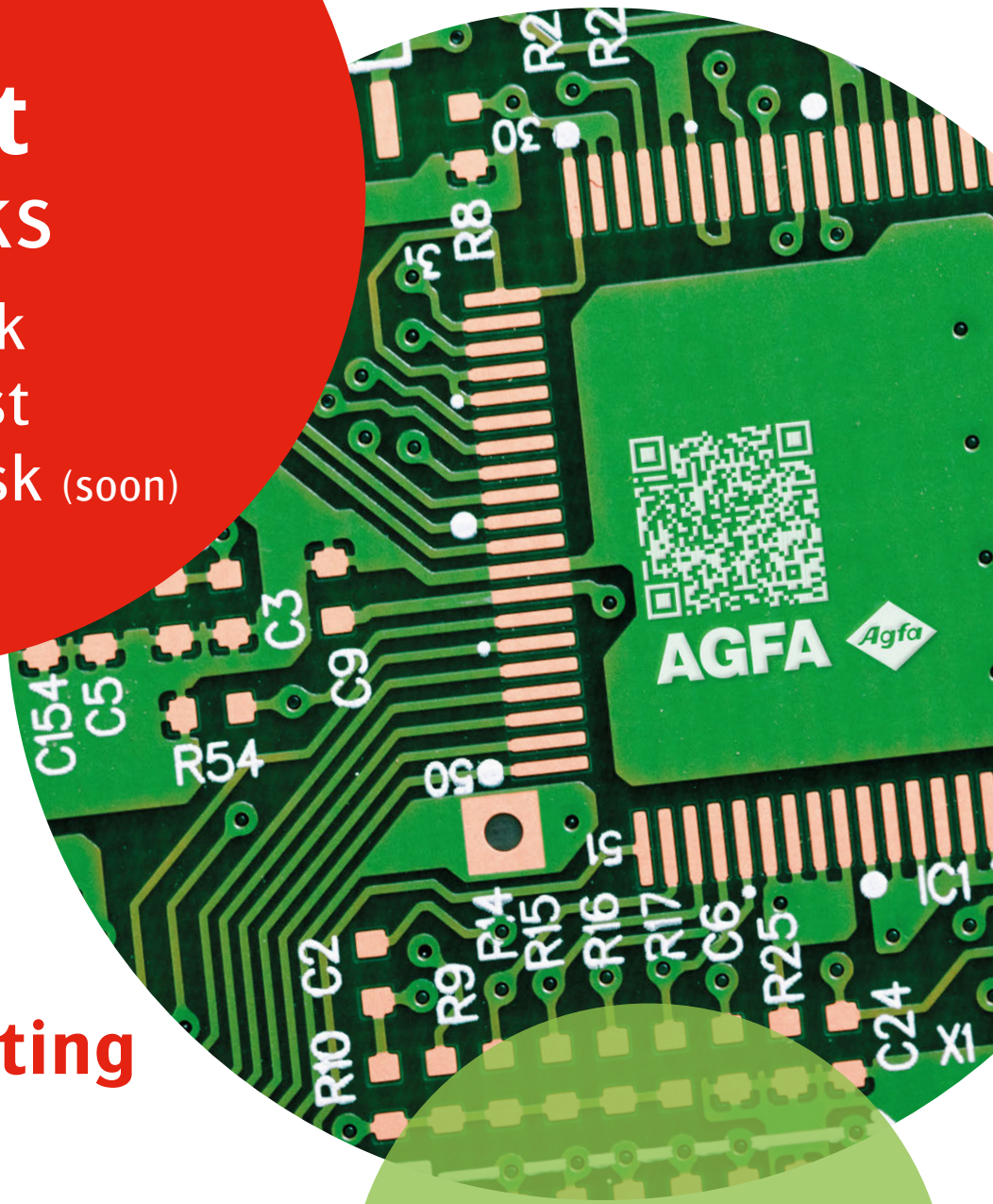


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# (Signal) Integrity for All

**by Patty Goldman**
I-CONNECT007

We are just back from the IPC fall meetings and the SMTA International conference and show, held jointly every September in Rosemont, Illinois. More than 75 IPC subcommittee meetings were there for the taking—and not just sessions related to assembly, as one might think. Plus, the SMTA conference had 2–3 technical tracks on Monday and five tracks each of the next three days. The exhibition, if not huge, was solid. Each year, the show seems to get bigger and better (though it may still be called small by international standards).

So, that aside, our topic this month is signal integrity, certainly a common one in our industry. Signal integrity is achieved by controlling impedance, so my advice is to do that. There, I'm done. Just kidding…of course I'm not done. But if you are in PCB manufacturing and you think this is just a design problem and doesn't concern you, please think again. As features on a board get smaller, as speeds get faster, and as more is expected from everyone in the supply chain, you too need to know. No sense hiding from it, so read on; this issue is for you!

To start, we introduce our newest columnist group, Elmatica, with Josse Johnsen authoring a primer on SI, covering basics that are important for both the designer and PCB manufacturer to know. Next, Viking Test's Marc Ladle uses down to earth examples to show just how complicated PCB processing can be when trying to control impedance.

We also bring you a rather detailed discussion on SI with this month's panel of experts: Mike Steinberger, SiSoft; Mark Thompson, Prototron Circuits; Yogen and Sunny Patel of Can-

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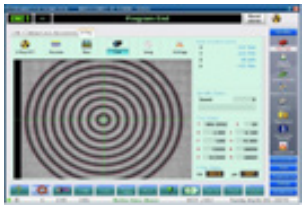

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dor Industries; and of course, Happy Holden. Learn about the challenges both designers and manufacturers face along with tips and pointers on how to deal with them. This is definitely some meaty reading.

Our next article comes from Scott Jewler of SVXR who makes a strong case for optimizing SI in the printed circuit using a new, non-destructive high-speed X-ray technology. The key words here are "non-destructive" and "high-speed."

Next, Happy Holden, known as the "father of HDI," makes the case for using HDI when designing and manufacturing PCBs that require stringently controlled impedance. Going beyond detailing the advantages and benefits, he meticulously ties together information from the SI masters with real examples to make this article a training course in itself.

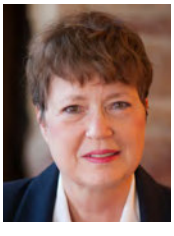
Our regular columnists round out the lineup this month. First, we have Mike Carano, RBP Chemical Technology, with Part 2 of his series on the importance of rinsing. Next, Keith Sellers, NTS-Baltimore, exhorts our readers to become experts in their fields by taking advantage of the myriad opportunities to learn: books, magazines, training courses, technical conferences, and IPC subcommittees are all ways to do this, along with IPC's certification programs.

A great follow-up to this is Steve Williams, The Right Approach Consulting, introducing his set of skills needed to become a world-class quality manager. Don't want to be a QM? These skills can be applied to just about any managerial position, but also to any life position. Check it out.

We wrap up with IPC's John Mitchell, who explains a bill recently introduced in Congress to create incentives for establishing apprenticeship programs. Recognizing the skills gaps that exist in the U.S. (not just in our industry), the bill presents a multi-pronged approach that involves tax credits, military veterans and employees nearing retirement. More details in his column.

Next month, we continue in this high-tech vein with HDI as our central topic. High-density interconnect technology was more or less "invented" right here in the U.S., but largely ignored here, taking off primarily in Asia. But, again, as we continue to cram more and more into less and less, HDI is truly coming into its own.

You know the drill: If you haven't already, subscribe now to have *The PCB Magazine* delivered to your inbox every month. You want to be at the front of the line when the next issue publishes. See you then! **PCB**



**Patricia Goldman** is managing editor of *The PCB Magazine.* To contact Goldman, click here.

# New IPC Studies Show World PCB Market up in 2016 as North American Market Shrinkage Slows

World PCB production reached an estimated $58.2 billion in 2016, up 2.2% in real terms, while North American PCB production decreased 0.1%, according to IPC's newly published "World PCB Production Report" for 2016. The North American PCB market also continued its downward trend, but at just -1.7% in 2016, based on data published this week in IPC's 2017 Annual Report on the North American PCB Industry.

The "World PCB Production Report" shows that more than half the world's PCBs based on value are now produced in China, but Taiwanese companies are the leading PCB producers, fabricating most of their PCBs off-shore. India has the fastest-growing PCB industry in Asia and has joined the top 10 PCB-producing countries in the world.

The world report highlighted that rigid PCB production, which has slowed in recent years, was up slightly in 2016, while the previously growing flex segment decreased.

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# Planning a PCB: Signal Integrity and Controlled Impedance Considerations

**by John (Josse) Steinar Johnsen**
ELMATICA

*Editor's note: We are pleased to introduce our newest column, which will be contributed each month by a team member from Elmatica.*

Knowledge and experience are the two key elements when planning a PCB. Today's PCB designers must have far more knowledge and understanding of the PCB production process than in the past. This is especially important when they plan and how they plan the stack-up, via span, routing and power distribution.

This article will focus on multilayer boards since these are the types of PCBs where we truly see the importance of planning in the day-to-day PCB life. On a double-sided board, you can of course use one layer as a ground plane, but critical traces are not easy to handle.

As a designer, you know your needs when it comes to signal integrity, electromagnetic interference (EMI) design and impedance requirements. The factors involved are:

- Number of layers
- Number of power and ground planes used
- Sequence of layers
- Space between the layers

To continue, we can say that:

- Signal layers carrying critical signals, should always be adjacent to a plane
- Power and ground planes should be as close as possible for best capacitance
- Power and ground planes can use other material with a higher Dk, for best possible capacitance
- High-speed signals should be routed on innerlayers located between planes for best possible shielding

Multiple groundings will lower the reference plane's impedance, and reduce the common mode radiation from the high-speed signals. The lowest layer-count you need to achieve all of this is probably an 8-layer board (Figure 1).

However, these points can be very challenging. There might be a maximum thickness of the PCB that cannot be ignored; many plane layers will limit the number of signal layers. It can be difficult to get the wanted signal impedances, regarding distance between layers, track widths and gaps between tracks.

Signal integrity addresses the degradation of signal quality to the point where an error occurs. EMI focuses on the corresponding specifications, test requirements and interference between nearby equipment. For signal integrity, the key factor is to keep noise levels significantly below signal levels. Our noise margins are typical in the millivolt range for digital circuits,

| Layer No. | Via | Description | Layer Name | Material Type |
|---|---|---|---|---|
| | | Soldermask | | Dielectric |
| 1 | 200 | Signal | Top | Conductive |
| | | Prepreg | | Dielectric |
| 2 | | Plane | GND | Conductive |
| | | Core | | Dielectric |
| 3 | | Signal | Inner 3 | Conductive |
| | | Prepreg | | Dielectric |
| 4 | | Plane | PWR | Conductive |
| | | Core | | Dielectric |
| 5 | | Plane | GND | Conductive |
| | | Prepreg | | Dielectric |
| 6 | | Signal | Inner 6 | Conductive |
| | | Core | | Dielectric |
| 7 | | Plane | GND | Conductive |
| | | Prepreg | | Dielectric |
| 8 | | Signal | Bottom | Conductive |
| | | Soldermask | | Dielectric |

Figure 1: Sample of an 8-layer stack-up.

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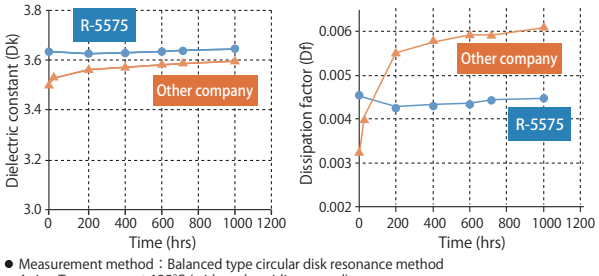


- Measurement method : Balanced type circular disk resonance method
- Aging Temperature : 125℃ (without humidity control)
- Measurement frequency : 18GHz

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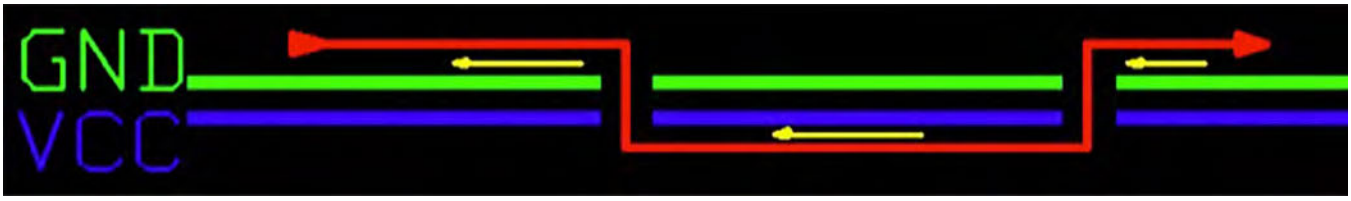


Figure 2: The return path, shown in yellow, is discontinuous if switching planes.

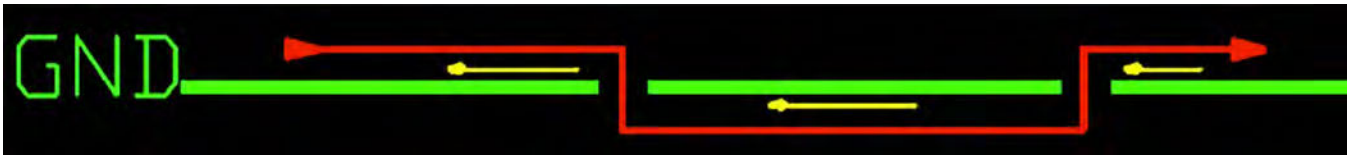


Figure 3: Return path shown in yellow. Reduced discontinuity if kept to same plane.

but for EMI, emission levels must be kept in the microvolt and microamp range.

Ground impedance is at the root of virtually all signal integrity and EMI problems. To keep a low ground impedance is mandatory for both EMI and signal integrity. This is achieved with a solid ground plane. In fact, the main problem with ground impedance is the discontinuities that occur in the signal path, and it has a major impact on characteristic impedance control.

Copper thickness is not an important factor. At high bit rates, the skin effect dominates so the signal is pushed to the copper surface, which means that additional copper thickness is irrelevant.

These days, with more and more HDI designs operating well up in the GHz frequencies, characteristic impedance control becomes more important, but also more challenging to maintain, since distances between layers are shrunk. HDI and microvias require less distance between layers, and the fact that more layers will be squeezed within a given PCB thickness.


Figure 4: Unbalanced differential pairs due to too wide openings in GND plane and/or signals routed to close to pad.

The biggest problem with maintaining impedance control is the signal path discontinuities, including the return path on ground plane. Ideally there should be a copper plane immediately underneath critical signals and the signal should refer to this ground plane without interruptions. The worst scenario (Figure 2) can be if the signal is leaving the ground plane and continues (e.g., along a voltage plane).

It is less problematic if the signal goes through the GND plane and continues on the other side of the plane (Figure 3). There is no issue with the reference GND since it is the same—just make sure that vias are kept as small and short as possible. The keep out (anti pad) diameter around the vias shall also be kept at a minimum.

There can also be cuts in the plane such as to large anti-pads (Figure 4). In this example, half of a differential pair is exposed over a miss-

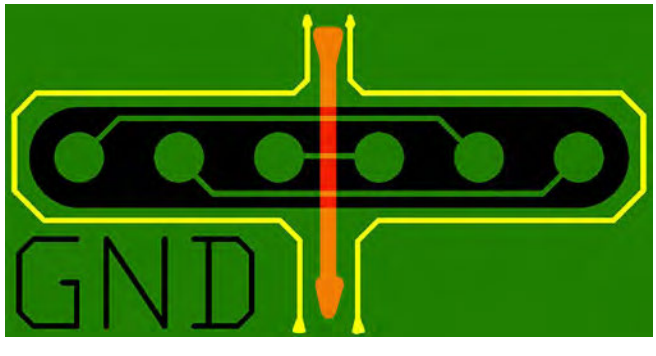


Figure 5: Disrupted return path due to cutout in the GND plane. Return path will go around the cutout.

ing plane. The result is an unbalanced current flow, delays in signal propagation delays, and increased series inductance.

Cuts in the plane (Figure 5) show a discontinuity in the signal return current path. The return path has to go all around the gap in the plane. This will raise the characteristic impedance at the gap, and the opening can end up as an antenna. The sample shows a split plane where other signals are routed in the plane opening.

**Let's Talk about Crosstalk**

Another issue for both EMI and signal integrity is crosstalk. Crosstalk is a coupling to adjacent signals, GND or PWR connection, that is unintended. Crosstalk is normally seen as a major problem with cables, but it can also occur at the PCB level. Increased space between critical lines is normally the solution. And in some cases, the space can be used for less critical lines. Increased spacing is in general very beneficial when coupling falls off with the square of the insulation distance. Increasing distance due to crosstalk, can also be an issue in the z-axis of the PCB.

When a new PCB design is to begin, designers should start communication with manufacturers at a very early stage. Start with the name/number of the PCB, then the following communication can be linked where it belongs. Do not communicate other PCBs in the same email/ticket. Unfortunately, this happens often and causes unnecessary misunderstandings and extra work.

When you as a designer need a stack-up to start routing, there is some information that you need to pass on to the engineers at the PCB manufacturer, so they have a base to start on. What you will get back is a stack-up with values on your impedance traces that you can use in your CAD software.

The strengths of PCB manufacturers have traditionally been:

- PCB material knowledge
- Lamination
- Drilling
- Plating
- Etching
- Surface treatment
- Mechanical finishing

The times have changed and electrical engineering is now part of what you get from the manufacturer. Electrical requirements such as impedance, plane capacitance, crosstalk and electrical testing is knowledge that you find in the engineering departments of the PCB manufacturers who can handle advanced PCBs. This, in combination with your own knowledge and skills is the best combination for a successful stack-up, and well working PCB.

The knowledge on how different laminates, types of glass styles, and resin content percentage work in the production process, are examples on knowledge PCB manufacturers know the best.

**Stack-up with Impedance Requirements**

Figure 6 shows a sample stack-up that reflects the drill and via span—information a manufacturer must get before setting up a final stack-up. This information tells the manufacturer that the following layers will be copper plated in addition to the etching. And that some layers also may need to be plated 2–3 times if there is a combination of mechanical and laser-drilled holes. It also informs that eventual holes shall be copper capped as well. Figure 6 also tells the total numbers of layers and where signal and plane layers are located. In addition, the follow information is needed:

- Final thickness of the PCB
- What impedances that are present on the various signal layers (single end and differential pairs) and their reference layers
- Preferred minimum track width. This is valid information for manufacturers, to give the right values back for track widths, due to HDI and or fine-pitch components used in your PCB
- If there are minimum distances between layers, due to crosstalk or other electrical reasons
- If you have preferred materials, it can be dedicated materials or materials locked to a IPC 4101/(undergroup), you should mention it
- Total size of the PCB

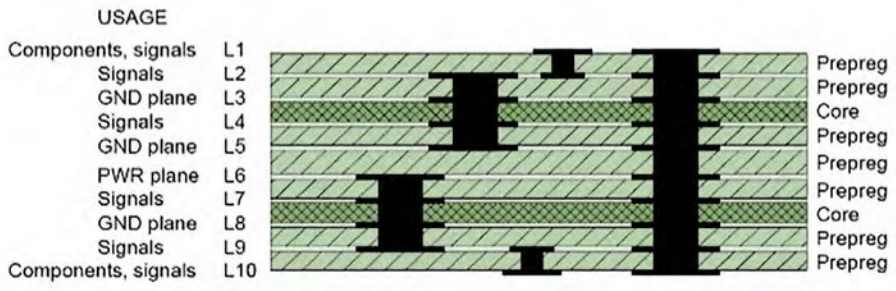


Figure 6: Example of a customer stack-up.

What you can expect back from the manufacturer is a:

- Complete stack-up, with copper and dielectric thicknesses, BOM (bill of materials)
- Track widths that you shall use on your impedance traces
- Space to use between the impedance traces (differential pairs)
- Calculation of the results above

You can now start your layout. Here's a tip: Make your impedance traces visible to the manufacturer. You can have most connections routed with, for example, 100 µm, and if there are some single-end traces using the same width, the manufacturer cannot separate these from the others. What you can do, is to set the width of the critical single end traces to a slightly higher or lower value (e.g., 99 µm or 101 µm). This change is so small that it has no influence on the production, but it will now be possible for the manufacturer to separate these traces from the others.

As a designer you should know that the stack-up you have received from your manufacturer, with values used for your routing, is not final. At the stage where your layout is ready and you want your PCB produced, there will, in most cases, be some technical issues on impedance values asked by the PCB manufacturer. These are caused, for obvious reasons, by the fact that manufacturers do not have access to your production data (Gerber, ODB++, IPC-2581…) at the stage when the stack-up is done.

When manufacturers have received your production data, they will also calculate the percentage of copper you have used on your signal and plane layers. This will influence the types and prepregs to be used, and will affect impedances.

The manufacturer will inform you via technical queries that some changes must be done for you to get your requested impedances. These changes will normally be very marginal changes on track widths, gaps or layer distances, and will in most cases be accepted without too much arguing. If there should be a change in the prepregs that will lead to a change in the resin content, this will also change the Dk value and will be taken into consideration when impedances are re-calculated.

For the designer it is most important to get requested impedances, and when it comes to these minor adjustments, I consider the manufacturer to know best what to do.

I often compose start stack-ups for designers, and I often use the ICD stack-up planner from In-Circuit Design. What we've seen used by most PCB manufacturers is the software from Polar Instruments.

My final tip to you is this: Get started. Communicate with your PCB manufacturer and do not forget to include a netlist with your PCB production data. Enjoy the wonderful world of printed circuits! **PCB**

**John Steinar Johnsen (Josse)** is Senior Technical Advisor with Elmatica.

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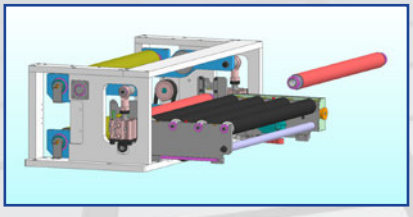

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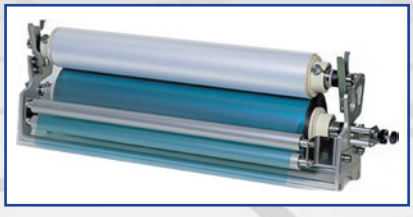

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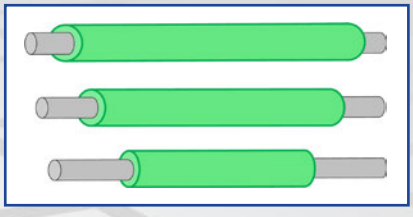

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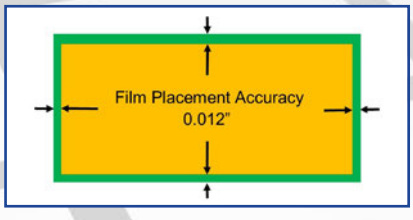


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# Fabricating for Signal Integrity

**by Marc Ladle**
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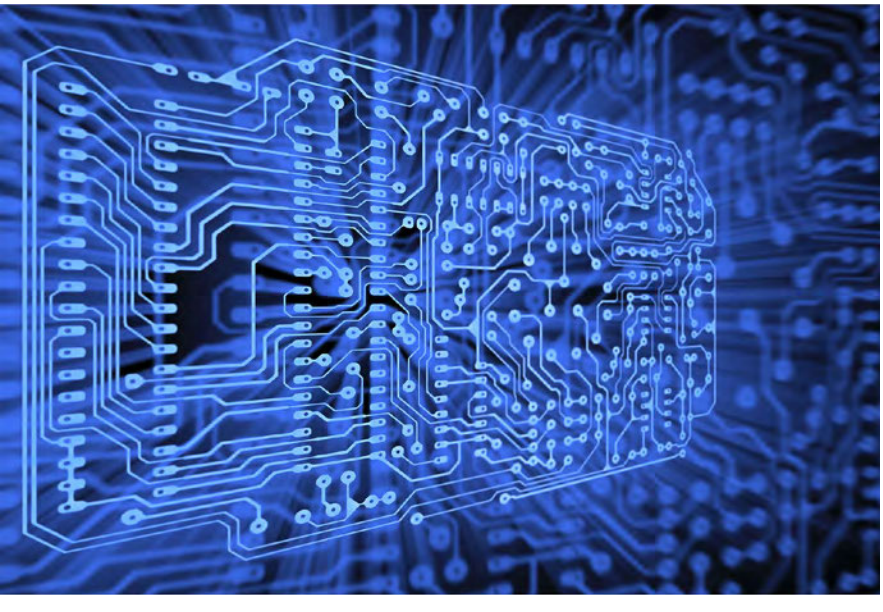
Signal integrity! In a world which is increasingly high-speed and digital, the chemical-dependent and mainly analogue-controlled world of PCB manufacturing is not always a comfortable partner.

In theory, the electronic performance of each PCB design is protected by the tolerances and material specification stated in the design package, but the further you proceed towards the limits of technical product performance, the more difficult it is to ensure you will get a perfect result.

Start with your base material. The copper thickness may be stated as 35 microns on the delivery paperwork but what is the real thickness of the copper? A lot of companies use a simple resistance-based thickness check to make sure they are using the right thickness but that will not tell you if you are starting with 35 microns or if the actual thickness is more like 33 microns. Copper is a relatively expensive commodity, and the process for foil production can be pretty accurately controlled. This means that material suppliers may use the allowed tolerance to their advantage by keeping the foil thickness closer to the lower limit of thickness.



Now let us consider a batch of 50 production panels passing through the inner layer process. Pretty early in the process you are going to have to clean the surface of the material to ensure your dry film photoresist will stick to the surface. Cleaning may be using an abrasive brush or chemical cleaning but either way you are reducing the copper thickness further.

Production processing is not a perfect science and reprocessing of material sometimes happens. Let's say the dry film had a wrinkle on the surface. In this case the material cannot be used unless the film is stripped and then the panel has to pass again through the surface cleaning process and be re-laminated with dry film. In the process, we lose a little bit of extra copper thickness which then means one of our production panels is a little different from the rest with regard to the remaining copper thickness.

The etching process then removes the unwanted copper leaving the desired line width on the PCB. Again—life is not perfect—there is always some variation, as fresh etch solution is usually dosed into the machine in pulses so the etch rate is not the same from one panel to the next. Our panel which already has a little less thickness than the others in the batch is a potential worst case as it started with less copper so would etch just a few percent faster than the others, meaning the final track width will also be slightly thinner than the other panels. Poor working practice may mean that an under-etched panel is re-processed through the etch, which removes the unwanted copper but also takes a little more of what should have remained on the track with it.

After stripping the dry film and inspecting the panels, they usually pass through a reducing oxide to roughen the copper surface in preparation for multilayer lamination. The oxide pro-

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cess takes a further skim of copper from both the height and width of the tracks.

There are some fail-safes to try to help us with the above problems. Automatic optical inspection can certainly check for over-etched panels, but in truth the capability is very limited. Nearly every machine is only able to access the width of the top surface of the track which leaves a significant open question about the shape of the sidewalls of the tracks. Undercut of the copper due to over-etching may not be apparent at inspection but it can significantly reduce the cross-sectional area of the conductor. There is also no way to be sure of the actual copper thickness remaining without a destructive microsection being taken—and there is no guarantee that every panel is the same as the next anyway.

> "The outer layer process is like the innerlayer process in so much as there are plenty of opportunities for variation—especially due to copper thickness variation through the plating process."

The outer layer process is like the innerlayer process in so much as there are plenty of opportunities for variation—especially due to copper thickness variation through the plating process.

We end up with a finished panel which potentially has quite a lot of variation in the cross-section of its conductors. All of the inspection processes have passed and been declared within tolerance but the variation is still there. For signal integrity, this variation can be quite a headache. It is possible to measure the variation with a high specification flying probe test which can test the exact resistance of every conductor, but this is a long and expensive way to test a panel. You can reduce variation by demanding than no re-processing of material is allowed at any time but there is a potential cost implication for this approach.

If your one in 50 panels is particularly unlucky it may get hit hard at every stage of the process. This worst-case scenario can lead to some disappointing results when the product is populated with components and product testing commences.

So far, all the points raised here have related only to the most basic of parameters which could affect signal integrity. Higher and higher signal speeds mean that the bar is constantly being raised with regard to reducing process variation. At the highest signal speeds, the smooth finish of the copper becomes a significant factor to ensure performance of the circuit. The so-called "skin effect" reduces the speed of the signal as the surface of the copper becomes rougher. At a couple of the normal manufacturing stages we went out of our way to roughen the surface of the copper to ensure good adhesion. The stronger the treatment of the copper, the worse the signal speed becomes. Adhesion against signal speed—two target conditions that are in significant conflict with each other.

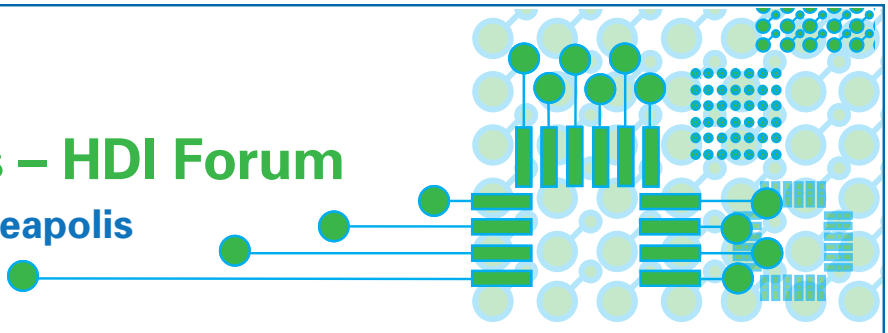
If you are a buyer or user of circuit boards, this may give you some idea of why there can be significant variation in circuit performance when you compare products from different fabricators. It is not necessarily a reflection of anyone doing anything wrong, just manufacturers working within the allowed parameters.

In adversity, there is often opportunity and I am pretty sure this is the case with high-speed signal transmission within circuit boards. Material suppliers are working hard to ensure their side of the copper has the required finish. Good fabricators will do their best to find ways to achieve the same. This market requires consistency from batch to batch to make sure that the end-product performs as required. If you can fulfill the brief your factory is likely to be busy for a little while. **PCB**

**Marc Ladle** is director at Viking Test Ltd. To contact Ladle or to read past columns, click here.

# IPC Flexible Circuits – HDI Forum

**October 17–18, 2017 • Minneapolis**



Topics of instruction and tutorials will range from flexible circuit metallization to designing a reliable and cost-effective HDI-circuit — this event promises to provide quality education and networking opportunities.

Subject matter experts from many of the industry's leading companies in this field will share their best practices, and proven methods of success, including:

- TTM Technologies
- Dow Chemical
- NSWC Crane
- Flexible Circuit Technologies
- Pioneer Circuits
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# Supply Lines
## Highlights

**MacDermid Enthone Electronics Solutions Launches MacuSpec AVF 700 Process**

MacDermid Enthone Electronics Solutions, a MacDermid Performance Solutions business, announces the release of the MacuSpec AVF 700 process, a high-performance electrolytic copper metallization for the filling of microvias in printed circuit boards.

**Ventec Shares Their Insights on the Laminate Market, Part I**

I-Connect007's Barry Matties sat down with the COO of Ventec USA/Europe, Mark Goodwin, to discuss the laminate market, the market segments behind that growth, and how Ventec has positioned itself in the thermal management space.

**Orbotech to Supply Unimicron with Industry 4.0-compliant DI, AOI and AOS PCB Production Solutions**

Orbotech Ltd. today announced a multi-million-dollar agreement with Unimicron Germany GmbH (formerly RUWEL International) for the purchase of Orbotech's direct imaging (DI), automated optical inspection (AOI) and automated optical shaping (AOS) PCB production solutions.

**High-Throw DC Acid Copper Formulation for Vertical Continuous Electroplating Processes**

The electronics industry has grown immensely over the last few decades owing to the rapid growth of consumer electronics in the modern world. New formulations are essential to fit the needs of manufacturing printed circuit boards and semiconductors.

**Insulectro Inks Deal to Distribute Dupont Electronic Inks for In-Mold Applications**

Insulectro is entering a deal to distribute DuPont conductive inks for in-mold electronics (IME).

**Laser Patterning & Metallization to Reduce Process Steps for PCB Manufacturing**

This paper details a new methodology for the plating of conductive features onto glass dielectrics. A laser is used to ablate material from a glass substrate in the desired pattern, and copper is "seeded" into these features using laser-induced forward transfer of a copper foil.

**Rogers Introduces CLTE-MW Laminates for 5G and Other Millimeter Wave Applications**

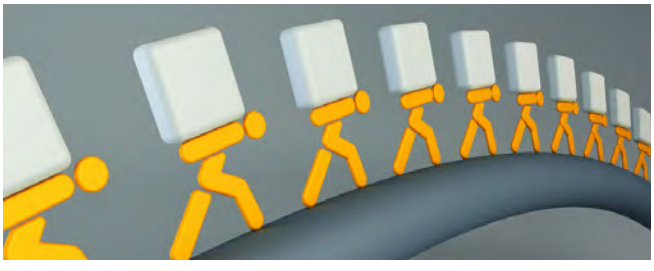
Rogers Corporation has introduced CLTE-MW laminates, a line of ceramic filled, woven glass reinforced PTFE composites. CLTE-MW laminates were developed to provide a cost-effective, high-performance material for the circuit designer. This unique laminate system is well suited for applications that have limitations in thickness due to either physical or electrical constraints.

**Isola Group Names Industry Veteran Sean Mirshafiei Global VP of Marketing**

Isola Group, the leading global and local manufacturer of copper-clad laminates and dielectric prepregs, has named industry veteran Sean Mirshafiei to a new position of global vice president of marketing. Sean is no stranger to Isola having held several positions in the company prior including director of strategic marketing and business planning, and director of high-speed digital products, among others.

**'Can Do' in CAM Outsourcing**

Time-to-market has been the mantra for every successful technology company. The best among them have strong and integrated supply chains that march to the drum of the OEMs and EMS providers that bring that technology to market. A big part of that success, especially in North America and Europe, is the ability for PCB manufacturers to turn around complex PCBs very quickly. The hallmark of PCB production in these higher-tech, higher-cost regions is flexibility and responsiveness.



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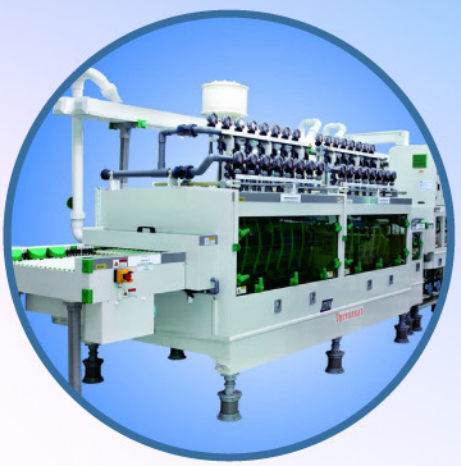

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# Experts Discussion:

## Signal Integrity and Impedance Control

**by the I-Connect007 Team**

When the content gathering for an issue on signal integrity and controlled impedance was officially underway, our I-Connect007 editorial team's first stop was an "experts discussion" with industry experts: Mike Steinberger of SiSoft, Mark Thompson of Prototron Circuits, and Yogen and Sunny Patel of Candor Industries. This teleconference call was a whirlwind at times, but we captured valuable information that we have distilled here, for our readers.

We started the conversation by asking that all important question: What are some of the challenges in signal integrity that are not being addressed right now? Mike Steinberger said that two points came immediately to mind:

"The large point is in the analysis of error-correcting code performance on high-speed serial channels. …I think that the benefits of error-correcting codes have been oversold, in that the performance analyses for error-correcting codes have been based on assumptions that are appropriate for radio channels, like where you have a lot of added noise—so a satellite channel or something like that. Therefore, the errors are completely uncorrelated. The fact of the matter is that on high-speed serial channels the errors are more correlated than that…I did some simulations and was able demonstrate that the correlation of errors is due to the inter-symbol interference. It's a very practical problem from a simulation perspective, but people simply haven't been doing that analysis. I predict that eventually error-correcting codes aren't going to give people quite the performance boost they expected.

"A smaller thing, but also important, has to do with what happens when you have a cutout in a reference plane. Suppose you have a transmission line that's going over a ground plane, for example. It gets to a certain point and there's a cutout in the ground plane. What happens when the transmission line hits that discontinuity? There are return currents flowing in the reference plane and those currents have to go someplace. Well, now, the return currents aren't going to flow all the way around this discontinuity to meet up at the other side. It turns out what the return currents do is

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BY TAIYO

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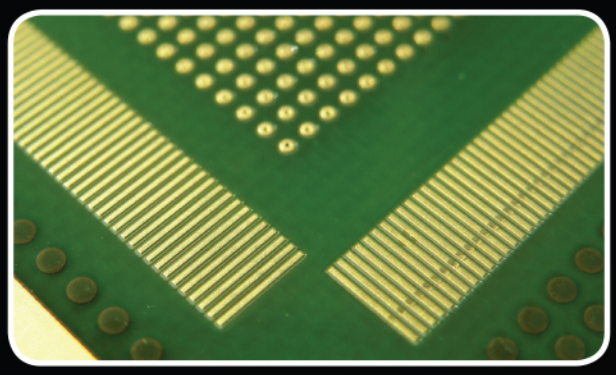

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transition to whatever the closest plane is, regardless of whether you have a return via. So you don't need ground vias to have this transition of the return current occur, and it turns out that there is a very simple formula for what amounts to an inductance that the return current goes through when it transitions from one reference plane to another. This is a piece of knowledge that all signal integrity engineers should understand, and basically none of them do…You get it from closed-form equations.

"Those are two immediate topics that I think need to be addressed, and the other thing we had better start thinking about is that we may be approaching a brick wall when it comes to throughput on serial channels. I'm going to take another chance here and say that there is going to come a limit, and we may be starting to get close to that limit."

Mark Thompson had further thoughts on this:

"We've been spending so much time over the last 10 years beating up the material manufacturers from the other side saying, 'Look, we need specific dielectric constants. We need specific loss tangents.' Now we're at a time in the existence of electronics and circuit boards that we're beating up the copper foil manufacturers for surface roughness because we're literally at a stage where 25 gig is the key, and at that stage any surface tooth or surface roughness is an issue. It's strange that we've gone from a situation where we beat up material manufacturers to the point where we're beating up copper manufacturers to get surface roughness down to a minimum."

According to Steinberger, Rogers has observed that when they measured transmission losses for two different kinds of copper—rolled annealed and electrodeposited—they found that the roughness models we've been using modeled the electrodeposited copper quite well but overpredicted the losses for the rolled annealed copper—by a lot. He added this:

"I find this fascinating because I've never been satisfied with the modeling of conductor losses. I see these bewildering models of conductor roughness and I ask, 'Where is the underlying physics? I'm not really seeing it.' I learned a theory that says, 'You've got a very lossy dielectric layer next to your electrodeposited copper. That's why you're getting the transmission losses. Not specifically because of the actual physical shape of the copper surface itself.' Maybe people will start asking you for rolled copper instead of electrodeposited copper."

Thompson noted that some of their customers have asked for RA copper, as opposed to the electrodeposited. He also commented, "Remember when people were asking for things like an 11-degree offset on a panel to minimize having to deal with having a structure sitting over the top of a glass knuckle or weave in the material, or even things like a skin effect due to differential pairs that were dipped in deep gold that didn't have any solder mask over the top of them. It's not as prevalent as it was in the last ten years."

According to Steinberger, that could be because "people end up routing at different angles anyway so you don't have these really long straight lines—or you shouldn't have these long straight lines—that they had on the test boards where they were measuring these effects to begin with. I never was happy with that whole discussion of weave effect. One reason was simply the emotional tone that got tied to the whole subject and the other is that people pointed to these weave effects, particularly the skew, which would be induced on a differential pair and talked about how you had to keep that differential skew down. But you can accept a certain amount of skew. You get a little bit of degradation but as long as you keep the skew within, say, an eighth of a wavelength at the maximum frequency of interest, the effects can be minimal."


Mark Thompson

Sunny Patel added his perspective at this point:

"We make boards for different technologies, and we can control the impedance to nearly

2%. We can talk about the challenges with keeping those tolerances that tight, like how the dielectric thickness and the etching characteristics in plating are really the key parts of the fabrication process."

Yogen Patel added, "We know that most manufacturers control impedance close to 10% most of the time. To control to under 5%, they charge so much extra money. There are three main differences between the conventional process as we call it and our process. First, our press is resistive-heating so the outer layer copper becomes a heater, and that's why we don't have to press at 350 PSI—we use 230 PSI—so the dielectric is very consistent across the whole panel. And then we drill, clean the holes, and panel plate copper over the whole board, which is the second difference. This makes for very consistent coper thickness over the whole panel and in the hole as well. And the third major difference is our positive-acting electrodeposited photoresist, where the areas exposed to UV light develop off. Then we etch in cupric chloride. In this way, we get very uniform conductors, and that's how we get controlled impedance to close to 2%."

Sunny Patel

Continuing, Sunny added, "The main issue on the board fabrication side is consistent lamination, making sure that the board shop has a good, consistent way of measuring at different weaves and resin contents. If a PCB manufacturer is pulse plating, the consistency will be pretty good, but that's generally one of the areas where most will have difficulty—with copper plating and copper etching as well. So, people with more direct imaging and pulse plating technology, or our way of doing things, will get you finer impedance characteristics. But a lot of it comes back to the engineers themselves, discussing stackups and what they want in the end with their PCB supplier—having that thorough conversation with the engineer on the board side to ensure that what they want is what they're going to get with the stackup. Those are the two main things: The process has to be controlled and consistent, and there has to be a clear communication with the design engineers."

Mark Thompson had more to say about interaction with the design engineer:

"I agree with you guys regarding the negotiation process. If a customer approaches you before they have a design ready, and their engineer has just told them, 'I have 8-, 10-, and 12-layer boards, and I need to get a slew of impedances from you, and a dielectric stackup with effective dielectric constants for each of the subsections,' there are several questions that must be asked at that time. A lot of us come up with an impedance checklist that asks all those basics, such as: What's the material type? What's the copper weight? Where will the impedances reside? What are the thresholds in tolerances (e.g., 100 ohms, 120 ohms, 75 ohms)? And what are the intolerances associated with it (2%, 5%, 10%, etc.)? At a stage where there has been no layout done and no actual artwork exists, it's difficult from a fabrication side to crawl into the customer's head and picture what it is he's trying to accomplish."

"But if you're dealing with a fabricator that has not dealt with coplanar waveguides properly, they'll come back and say, 'Cosmetically, we want to route this thing out and don't want to see any burring, so we're going to hack back that launch pipe three or four thousandths,' which is doing a huge detriment to you as the end user. Obviously, in a coplanar waveguide, the launch needs to reside right at the part edge, and the end-user is well aware that the exposed copper there is really what you want to see. You really want to see it actually meeting with the Z-axis and you don't want to trim it back in any way."

Thompson then shared an experience in which a material manufacturer shipped in very consistent material up to a point and then suddenly all the impedances were off; it was linear and all in one direction. After cross-sectioning, they discovered that the various laminate materials were all ~1 mil thicker than previously

predicted. They learned that a change had been made in the supplier's manufacturing process at one location which resulted in a slightly different dielectric thickness.

"That was a problem for us, because they were sending prepreg and core materials from two sources. How could we possibly predict impedances for a customer when we couldn't even predict the dielectric impedances of the prepregs that were being used?"

Thompson mentioned a couple of other challenges, such as when a customer makes a change but the revision does not provide for a reference plane—"they've inadvertently placed a bunch of differential pairs over split sections, and you don't have a proper reference plane." He also mentioned that some things, such as lengths cannot be controlled; lengths of less than 0.300 mils are very difficult to control.

Getting to the fab side of things, our panel discussed the challenges specifically for manufacturing including variation in the etching and plating areas, as well as techniques to minimize any signal losses in a Class 3 mil/aero world. According to Thompson, blind, buried or epoxy-filled vias may require an additional wrap plate which could affect impedances.

At this point, Steinberger expressed concern, referring to a time, 10–15 years ago, when non-functional pads were removed, but today, the dense board geometries mean this can be risky.

"I start to wonder more about pad sizes, backdrill precision, and the fact that I can't get big enough anti-pads on my vias to get the impedance I want… From my end of it, I'd like to remove all the pads. If I could get away with a pad diameter equal to the drill diameter at my routing layer, where I did want to connect to the trace, I'd do it."

Sunny also had thoughts on this.

"Technology in general has yet to catch up to what we require. The new types of lay-up, back straights, calculations, algorithms—are all trying to get back to what you're saying, to remove those non-functional pads and get that alignment to where we need it to be for perfect manufacturing. We think that probably helps with the impedance control side of things, though there is more testing to be done."

Yogen added, "But by using the positive-acting electrodeposited photoresist, we can consistently make landless vias, so you don't need a pad. Also, you mentioned wrap plating, which you wouldn't need. Once you have proper plating in the hole and on the surface, why would you need a wrap? We should concentrate on cap plating."

Steinberger then raised a question: "Is there any conversation about eliminating the via stubs for extremely high-frequency signals? For example, are people going to multiple laminations so that they can keep vias confined to sub-laminates, or are designers driving you to get the absolute minimum via stub length on a back-drilled via, stuff like that? Part of the reason for my question in general is—at least in the design spaces I do happen to have experience in—it's all about the vias."

In response, Yogen mentioned one of his customers, who had asked for back-drilling right to the layer, leaving very minimum stub, with Sunny adding that they still have the sub-drilling customers at the same time, which results in a "mixed bag." Sunny feels that there is no clear direction as to which way is more popular on a design side, but stated that sub-laminate drilling is more expensive than back-drilling. Thompson agreed that having to do either blind, buried, and/or back-drilled vias will create far costlier scenarios.

Yogen Patel

Continuing the subject of vias, Steinberger said, "The other thing that people aren't aware of is that, if you have even a relatively small back-drill stub, there is a fringing capacitance at the end of that stub which is quite significant compared with the total capacitance of the stub as transmission line. You really have to back-drill the stub to something smaller than the pad diameter in order to start really

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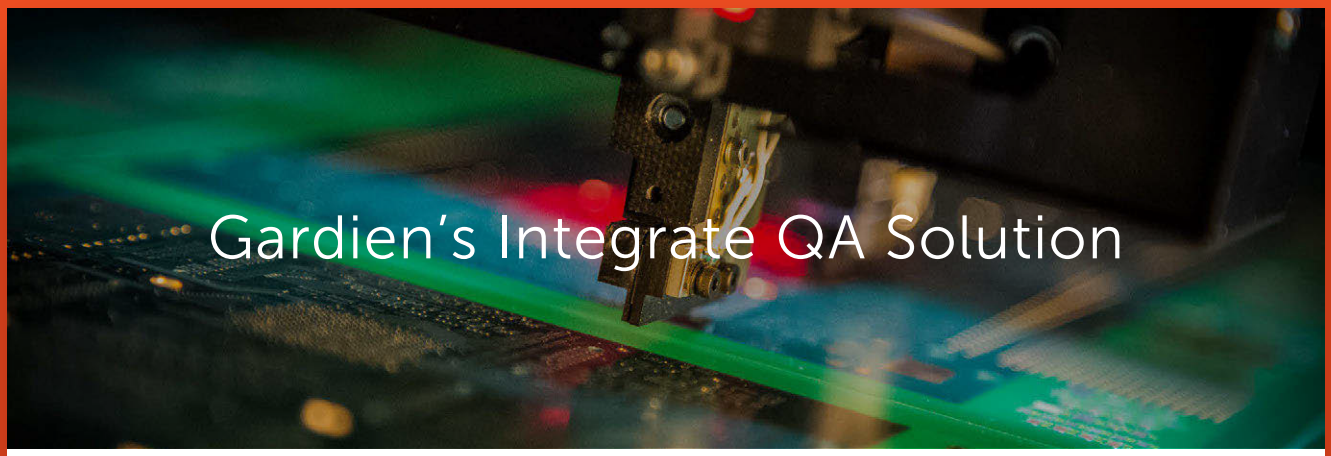

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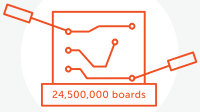


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eating into that fringing capacitance. That's something people don't generally think about and I wonder how many people have been able to see a characterization. It's enough to get your attention."


Mike Steinberger

Yogen said, "Companies have to start using the landless via, like what we produce. We invented our process in 1995 and have been using it for the last 20+ years. With the positive-acting electrophoretic photoresist, whatever pad size you put that's what comes out, so if you have 6 mil holes then make the pads 7 mils; you get extremely reliable landless vias, and now with direct imaging technology you can get even closer."

At this point, Happy Holden referenced an article on landless vias that he wrote last year.

"There are four different ways of doing it, one of which is the positive electrophoretic resist. But there are three other ways: the direct imaging machines, the Hewlett-Packard method that they got from the Japanese (which doesn't require any change in imaging registration), and then there's the Russian method. Anybody can use the Hewlett-Packard and Russian methods; they are free and no change of equipment or process is required—just a change in artwork. I've made more landless vias than everyone in the world put together, but the article mentions all four methods."

When Steinberger asked why more companies don't make landless vias, Holden's response referred to IPC specs, which require a minimum pad size to surround any via or hole.

Holden: "Landless vias were never adopted by the IPC, though we (HP) have data that shows landless vias are 10-times more reliable than vias with lands. The landless via and its reliability blows a hole in Class 1, 2, and 3 [of the IPC specs]. HP did extensive testing: on different hole diameters, different thickness of boards and different sizes of vias, and we found out that our Japanese partners apparently knew a lot more than we did, and they were less subject to influence from the IPC. You needed a pad 50 years ago because we used to crimp actual leaded components, not to the whole barrel but to the pad, and because we've been doing it for 60 years, the industry thinks we have to do it forever, even though it's detrimental to both reliability, density, and signal integrity. Hewlett-Packard used them exclusively once we discovered the secret, and nobody bothered to look at our boards closely enough to realize there weren't any lands on those vias. They're covered with solder mask, so you don't really see it."

Yogen added, "We have data on 6-layer landless vias that pass 1,000 IST cycles; the IST person says it's much better, because there's no pad to anchor it and then crack. Normally the pad will only anchor to the laminate and then crack at the knee of the hole. But if you've got no pads, then you've got no corners to crack."

Steinberger mentioned that he intends to contact a few colleagues, who he said, "are actively designing a system at 28 gigabits and starting to plan for 56 gigabits" and pick their brains about landless vias.

Holden concluded this portion of the conversation by reminding us of days gone by: "Hewlett-Packard, in my day, was operating at 150 GHz for microwave test equipment, and the test equipment had to be nearly 8 to 10 times better than what we were measuring; even back in the '90s and the 2000s, we were way over 150 GHz. So, making very sensitive test equipment, you do a lot of testing, and you find out a lot of myths aren't correct, and in fact they're detrimental and not being controlled by military standards or things like that."

This conversation next ventured into design territory, which we will excerpt in the October issue of *The PCB Design Magazine*. **PCB**

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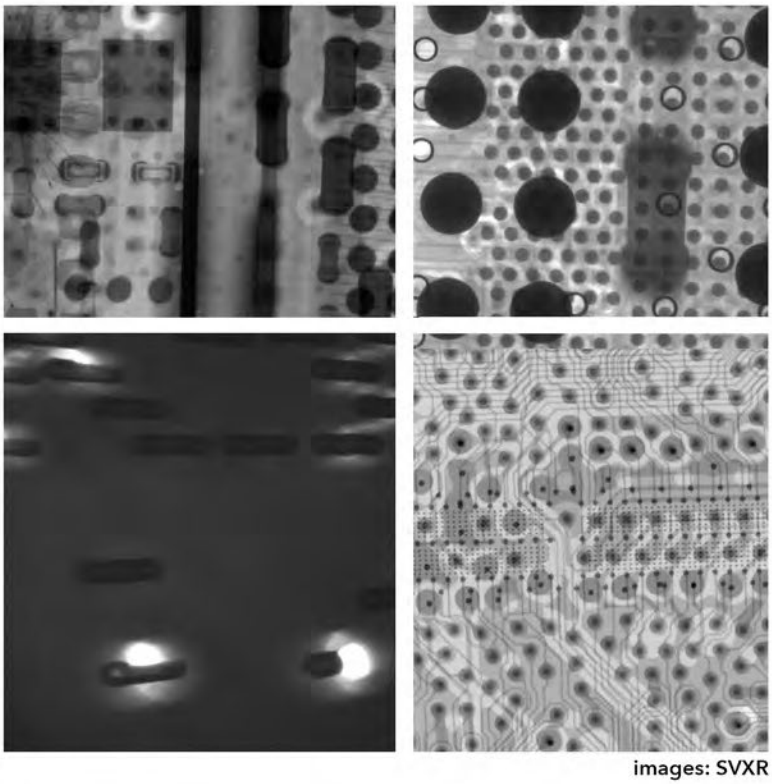
# PCB Signal Integrity Optimization Using X-ray Metrology



images: SVXR

**by Scott Jewler**
SILICON VALLEY X-RAY

## Murphy's Law

It happens again. A new backbone router/switch build or a line card upgrade is approaching completion when something goes wrong. The system won't operate at the targeted data rate. Deadlines are looming and the root cause of the problem is buried somewhere in a big rack of electronic components. The integrated circuits were all speed tested prior to printed circuit board assembly. There must be a problem in the system assembly, but where?

For some time, control of printed circuit board manufacturing to specification has relied primarily on coupon tests. These are time-consuming and often poorly represent the live portion of a panel, much less a population of panels. Modifications to designs, variations in line and space widths, and misalignment of layers can occur without the supplier being aware of the impact these changes have on the system's performance. Electrical test methodologies for bare boards are difficult to maintain, expensive, and provide limited information. Engineers are left to commit large amounts of money to board builds and cloud server manufacturing and hope the PCBs perform per design.

## The challenge is getting harder

As the industry moves rapidly to full deployment of 28 Gbps backplanes, many cloud hardware and PCB manufacturers are just beginning to regain confidence that what they build will work as intended. But 56 Gbps backplanes are just around the corner, or already in the driveway for some companies. And line cards are not far behind. These faster data rates require even tighter design compliance and PCB process control.

Certainly, much of this battle will be fought on the design side. Single layer routing, sacrificial vias, and other techniques can mask PCB process variation. But is this the most desirable or cost-effective solution? The time is right for a new generation of metrology tools that will enable PCB manufacturers to build better products and for network designers to unleash the performance of their products without worrying about variances in as-built boards.

## The Back-Drill Dilemma

Via stub length for high speed nets has been an industry concern for some time. Back-drilling to shorten the length of the via stub extending beyond the internal signal layer is a relatively cheap and effective solution and has been

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widely deployed for nets up to 28 Gbps. Stubs can typically be terminated within 12 mils of the target signal layer pad, using cross-sectioning of test coupons to check a few of the resulting stub lengths after back-drill.

However, some manufacturers are reporting the need to control via stubs to six mils maximum for 56 Gbps nets. Are backplanes being shipped today able to operate at these higher speeds? Net-by-net electrical testing using time-domain reflectometry (TDR) provides some level of compliance testing but is it sufficient or practical? Figure 1 shows a cross-section view of a typical back-drilled via stub. While back-drill accuracy can be measured in this way, it is certainly insufficient to meet these emerging requirements for precision.

## Other Challenges

While stub lengths are a major culprit in the failure of high speed PCBs, they are not the only problem. Stub drilling can be misaligned resulting in slivers in the via. Coupon tests in the corner of a board are unlikely to provide any useful information about this kind of defect. Even with good stub length control, other things can go wrong. The as-built net impedance may just not match the design value. Has the design been modified for manufacturability? Is the variation in line width and space greater than intended? Countless hours of engineering time and weeks and months of new product launches have been lost searching for these kinds of variations. And this challenge will only increase data rates are accelerated.

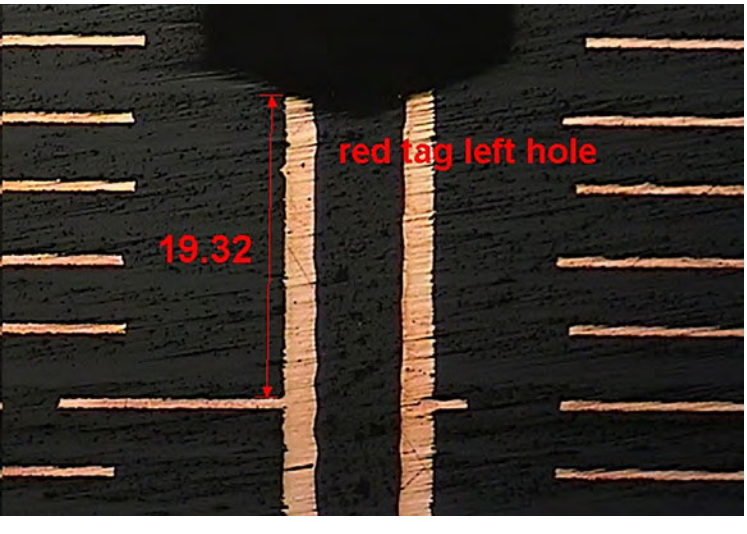


Figure 1: A back-drilled via view after destructive cross sectioning.

## What's next?

A look into other parts of the electronics ecosystem illuminates the direction that board making must go to meet the needs of the most demanding customers. The semiconductor industry faced similar problems some time ago. Existing line monitors and controls failed to detect variation that led to device failures. KLA and other manufacturers introduced new defect detection and metrology tools. These tools didn't go into a measurement lab outside of the manufacturing area, they went directly into the line and were integrated into the process routing. By integrating real-time metrology into manufacturing, semiconductor makers have been able to pack more and more circuitry into the same space while increasing operating speeds and reduction power consumption.

## Metrology in PCB Manufacturing

Even if net-by-net electrical testing was more cost-effective, at best it is a screening tool to catch non-compliant boards before they are populated with integrated circuits. Drill surface detection helps but as board layers increase, variation in the position of signal layers in the full board stack become greater and greater.

The structure of PCBs and the measurements that are required to drive improved process control clearly point towards a transmissive metrology solution that can look through a board stack and detect non-compliant stub lengths or slivers from misalignment. But what about accurate pre-mapping of actual signal layer position across the entire area of a high-speed board? Would not this information allow for significantly more accurate back-drilling?

## High Speed X-ray Metrology

X-ray tools have been used in PCB assembly for a long time. These systems are extremely fast but do not provide sufficient resolution to drive the improvements described above. High resolution X-ray systems are being installed by some PCB manufacturers for failure analysis,

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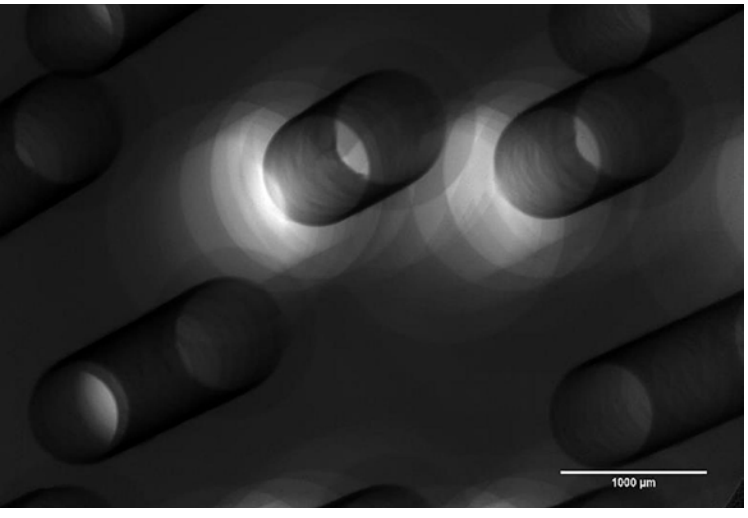


Figure 2: X-ray of multilayer PCB with wide dynamic enabling detection of individual signal layers.

but these tools are much too slow to provide useful data on the thousands of high-speed nets on a single board, not to mention a line producing hundreds of boards a day. But a new X-ray technology has entered the market that provides both the speed and resolution. And by integrating advanced image analysis and machine learning software with this new high-speed X-ray solution, the era of high-speed X-ray is upon us. A tool with these capabilities is currently under development with commercial release anticipated in the first quarter of 2018.

### What does this mean for PCB manufacturers?

1. Stub compliance. No more shipping boards with only coupon test data. 100% of the high-speed net via stubs can be quickly and accurately measured prior to shipment.

2. No more slivers from back-drill misalignment. Slivers are a killer and can occur randomly across a board. As layer counts increase, back-drill alignment becomes tougher. At the same time, denser designs limit the drill size that can be used for back-drilling, taking away even more design margin.

3. 56 Gbps and higher speed boards are no longer stub length limited. State-of-the-art for stub length is about seven mils maximum today. It is crucially important that the PCB industry move to shorter stub length technology. This can only be achieved by contour mapping of signal layers as laminated. High-speed X-ray metrology is the only method available to map the signal layer position in a board stack and feed this information into the drill recipe to individually target the drill depth for each individual net.

### What about their customers?

1. Time to market. High-speed X-ray is the only means of confirming that the dimensions on the finished board match those in the design. New product introductions (NPI) can quickly identify the causes of any performance issues on a single cycle.

2. More design margin available. Instead of using design margin to accommodate poorly manufactured boards, designers can instead optimize for cost and performance.

3. Credibility in the field. When a manufacturer sells a router or switch that is field upgradable, they need to know that the backplane can perform at higher speeds than as originally shipped. Line card swaps that turn into forklift box exchanges are a terrible outcome for everyone that can be avoided by tightening PCB manufacture process control and ensuring compliance.

### Conclusion

The electronics industry is characterized by continuous improvements in size and performance. As the industry moves forward, inflection points arise where doing things the same way can no longer achieve acceptable results. We are at that point in high-speed networking applications now and the quantity of boards that need to meet these tighter specifications is only going to grow. High-speed X-ray metrology allows contour mapping of as-built signal layers for tighter targeting and compliance testing of stubs and other features for conformance to design. **PCB**

**Scott Jewler** is co-founder of SVXR, an X-ray metrology company bringing new and innovative technology to the printed circuit board industry. To contact Jewler, click here.

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# Electronics Industry News
## Market Highlights

**Insect Eyes Inspire New Solar Cell Design**
Packing tiny solar cells together, like micro-lenses in the compound eye of an insect, could pave the way to a new generation of advanced photovoltaics, say Stanford University scientists.

**Scientists Move Graphene Closer to Transistor Applications**
Scientists at the U.S. Department of Energy's Ames Laboratory successfully manipulated the electronic structure of graphene, which may enable the fabrication of graphene transistors that are faster and more reliable than existing silicon-based transistors.

**Scientists Create World's First 'Molecular Robot' Capable of Building Molecules**
Scientists at the University of Manchester have created the world's first 'molecular robot' that is capable of performing basic tasks including building other molecules.

**Convergence of Big Data, IoT and AI to Drive Next Generation Applications**
Disruptive technology innovations in the information and communication technology (ICT) space, such as artificial intelligence (AI), Internet of Things (IoT), self-service visualization and structured query language (SQL), have deeply permeated various applications and markets.

**Medical IoT Enabled by Convergence of Sensor Technology and Connectivity**
Healthcare is facing one of its major turning points in decades. After penetrating the consumer market, the digital revolution and its related IoT concept is rapidly changing health models.

**A New Way to Print Electrical Circuits**
Within 15 minutes of meeting Mark Hersam, PhD, a renowned nanotechnology expert and professor of materials science and engineering at Northwestern University, Ethan Secor knew he wanted to work with him. Secor, a fifth-year materials science and engineering PhD candidate, didn't have a project in mind at the time, but when Hersam had an opening in his research group, he jumped right in—and hasn't looked back.

**Highly Flexible, Wearable Displays**
Engineers have created wearable displays for various applications including fashion, IT, and healthcare. Integrating OLED (organic light-emitting diode) into fabrics, the team developed some of the most highly flexible and reliable technology for wearable displays in the world.

**Thin, Flexible Device for Efficient Cooling**
Engineers and scientists from the UCLA Henry Samueli School of Engineering and Applied Science and SRI International, a nonprofit research and development organization based in Menlo Park, California, have created a thin flexible device that could keep smartphones and laptop computers cool and prevent overheating.

**Flexible Hybrid Electronics and Sensors Impacting the Automotive Industry**
FlexTech, a SEMI strategic association partner, will host a one-day Flexible Hybrid Electronics and Sensors Automotive Industry workshop in Detroit, Michigan on September 13, 2017 to explore how FHE adds functionality, decreases weight and impacts design.

**Nanocarbon Materials are Challenging Silicon, from Transparent Electronics to Bendable 3D Displays**
The superior characteristics of nanocarbon make it an extremely promising material for numerous current and future applications.

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> *-Thomas Hofmann, CEO/Owner*

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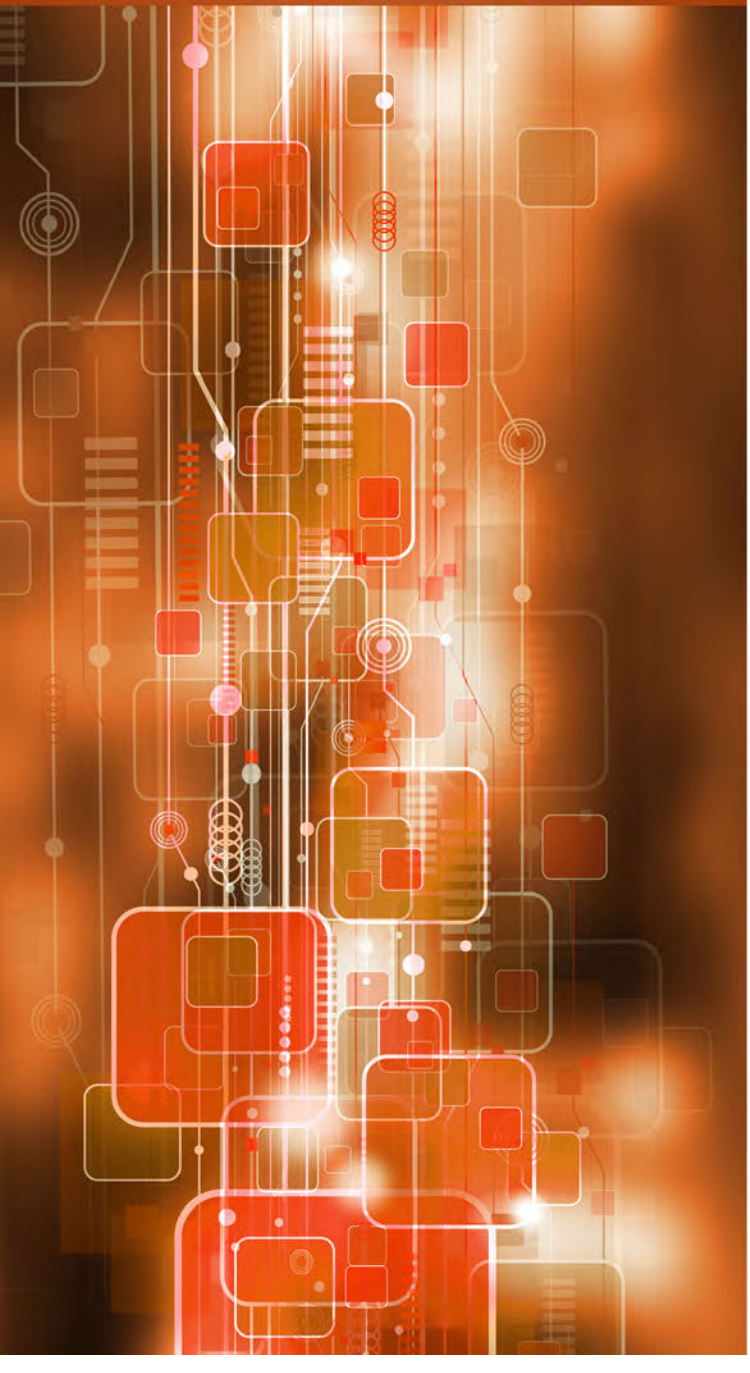
# HDI's Beneficial Influence on High-Frequency Signal Integrity



**by Happy Holden**
I-CONNECT007

## Introducing the Benefits of Microvias

The increasingly widespread use of fine-pitch ball-grid array (BGA), chip scale packaging (CSP), and other evolving technology form-factors means that new fabrication techniques must be used to create printed circuit boards (PCBs). In addition, extremely fast clock speeds and high signal bandwidths challenge systems designers to find better ways to overcome the negative effects of noise, radio frequency interference (RFI) and electro-magnetic interference (EMI) have on their product's performance. Finally, increasingly restrictive cost targets are compounding problems associated with today's smaller, denser, lighter, and faster systems.

Staying competitive and delivering the products people want means seeking out and embracing the best available technologies and design methodologies. The use of PCBs incorporating microvia circuit interconnects is currently one of the most viable solutions on the market (Figure 1). Adopting microvia technology means that products can use the newest, smallest, and fastest devices, meet stringent RFI/EMI requirements, and keep pace with downward-spiraling cost targets.

## What are Microvia Technologies?

Microvias are vias of 6-mils (150 microns) diameter or less. Their most typical use today is in blind and buried vias used to create interconnections through one dielectric layer within a PCB. Microvias are commonly used in blind via constructions where the outer layers of a multilayer PCB are connected to the next adjacent signal layer. Used in all forms of electronic products, they effectively allow for the cost effective fabrication of high-density assemblies. The IPC has selected high-density interconnection structures (HDIS) as the term to refer to these various microvia technologies. This definition is by no means universal. The Japanese refer to any via drilled by lasers in a thin dielectric as a microvia.

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**Why use Microvias in PCBs?**

From a physical and electrical standpoint, microvias offer several distinct advantages over their mechanically created counterparts. Systems with higher circuit densities and better electrical performance can be created using the smallest and most advanced components available. As a result, smaller, lighter, and more robust products can be built[1].

The major benefits of using microvias are:

- Lower costs through board size reduction (easily up to 40%) and layer elimination (up to 33%)
- Product size reduction: lower substrate weight, thickness, and volume
- Increased wiring density: closer component spacing with more connections per component, which permits higher density at a lower cost. At higher densities, HDI costs less per connection
- Improved reliability: The thin nature and 1:1 aspect ratio of microvias deliver increased reliability over larger drilled through-holes.
- Improved electrical performance (signal integrity): HDI has one-tenth the parasitic inductance, and capacitance of through-holes, fewer stubs, less reflections, less ground bounce, and better noise margins.
- Lower RFI/EMI: Since ground planes are closer to or on the surface and distributed capacitance is available, RFI/EMI is significantly reduced.
- Improved thermal efficiency: The thin dielectrics and higher Tg of HDI improve thermal performance.
- Greater design efficiency: Microvias allow ease of part placement on both sides of an assembly as well as improved component escape routing (via-in-pad).
- Faster time-to-market: 100% completion by HDI auto-routers because of placement and easier innerlayer free space routing.

***Lower PCB Costs***

HDI boards can usually provide higher density (increasing past eight layers) at a lower cost. When complex blind and buried vias are produced by sequential lamination, a simpler HDI board will usually cost less.

***Product Size Reduction***

Routability area gains increase the potential for a PCB layer count reduction in the design, and for a physically smaller form factor gained through increased circuit density. This allows for better component placement, improved layout options, and better electrical performance. This will be illustrated in the case study provided later.

***Increased Circuit Density***

Because microvias can be incorporated within the pad structure, there is a major reduction in fanout. Further, microvias provide not only additional gains in routable areas, but also improved cost-effectiveness during manufacture. Greater via density per given area provides a greater number of routing tracks per the same area. The benefits of this are twofold—designers can place components in much closer proximity to each other while achieving a corresponding increase in trace routable area.

***Improved Reliability***

The thin nature and 1:1 aspect ratio of microvias deliver increased reliability over larger drilled through-holes. HDI boards have long been used in European military, transportation, and spacecraft. The data is available from IPC's ITRI on reliability testing of HDI multilayers.

***Improved Electrical Performance/ Signal Integrity***

Due to the physical structure of microvias, there is a reduction in switching noise. This is attributable to the decreased inductance and capacitance of the via as its physical size becomes smaller and shorter. A microvia will have nearly one-tenth the electrical parasitics of a through-hole. Another advantage of using microvia technology for creating interconnects is a reduction in circuit noise, signal reflections and crosstalk between traces. Miniaturization offers the opportunity for smaller current loops on critical nets. The corresponding increase in routability area also allows designers to place traces further apart to reduce crosstalk. More on this later in the article.

***Lower RFI/EMI***

In the realm of RFI/EMI, combining the increased routability area with the microvias' physical via-in-pad implementation allows designers to place more ground plane around components. By doing this, the size of ground return loops decreases and improved RFI/EMI performance is realized. Thin dielectrics characteristic of HDI along with PWR/GND pairs also reduce EMI and radiations. More on this later in the article.

***Improved Thermal Efficiency***

The thin dielectric and higher Tg of HDIS materials improved thermal performance. Many complex enhanced tape BGAs are made of thin, laser-drilled polyimide film.

***Greater Design Efficiency***

Microvias allow ease of part placement on both sides of an assembly and improved component escape routing (via-in-pad or swing-vias), leading to easier inner layer free space routing and 100% completion by HDI auto-routers. New fine-pitch parts can easily be utilized.

***Faster Time-to-Market***

Microvia placement on both sides of an assembly makes placement and routing faster. Either manual or auto-routing, the blind/buried via stackup provides 2–4x greater routing density per signal layer, making routing easier and faster.

These benefits are highlighted in Figure 1[1].

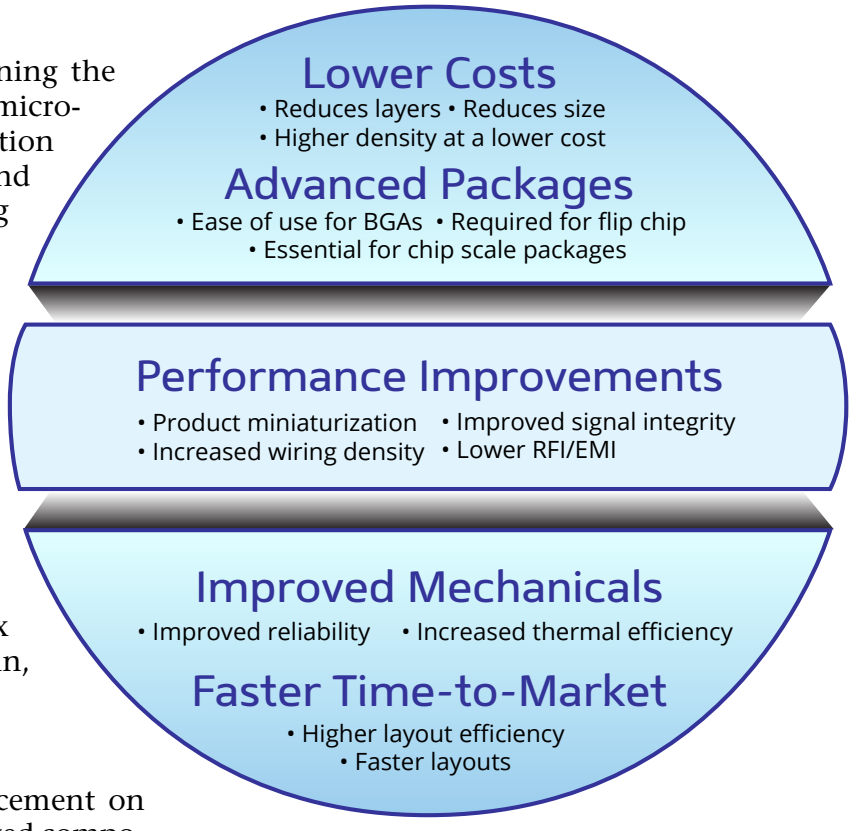


Figure 1: Five major areas of HDI benefits.

**Details on Signal Integrity and HDI Electrical Performance**

The information in this section has been presented by experts such as Dr. Eric Bogatin[2,3] and Dr. Paul Franzon of NC State University[4]. (For further information, use the link to Dr. Bogatin's papers shown in references 2 and 3.)

Signal integrity improvements are certainly available to all who take the time to respect Mother Nature. HDI's contribution comes mainly

| HDI Features | Signal Quality | Cross Talk | Switching Noise | EMI |
|---|---|---|---|---|
| Short interconnect lengths | X | X | | |
| Low dielectric constant | X | X | | |
| Small vias and small features | X | | X | |
| Vias in pads | | | X | |
| Fine lines and thin dielectric | | X | X | X |
| Support for fine-pitch components | | | X | X |

Table 1: HDI features and the SI problems they help solve[2,3].

from the adage "Smaller and closer is better!" That is, HDI's main contribution is miniaturization! The signal integrity improvements for HDI come from three phenomena: noise reduction, EMI radiation reduction, and improved signal propagation and lower attenuation.

***Noise Reduction***

Four categories of noise describe the various effects (Table 1)[2].

1. Signal quality of one net and its return path (ringing due to reflections)
2. Crosstalk between two or more nets (noise pulses due to switching on neighboring lines)
3. Switching noise (noise on power and ground lines/planes)
4. EMI

Each of these four categories has specific causes (Figure 2). By identifying the cause in each category of problems, design- and technology-based solutions can be identified and implemented[3].

Noise can come from many sources in the board layout, such as:

- ✔ Changes in trace width
- ✔ Plane splits
- ✔ Cutouts in power/ground planes
- ✔ Via antipads (the opening in a power or ground plane for a drilled hole so it doesn't make contact)
- ✔ Insufficient plane capabilities
- ✔ Excessive stubs, branched or bifurcated traces
- ✔ Component lead frames
- ✔ Improper impedance matching and termination networks
- ✔ Coupling between signals
- ✔ Varying loads and logic families

**Signal Quality of One Net and its Return Path**

HDI is a fabrication technology of miniaturization that has two main benefits: a smaller substrate and improved SI. The smaller substrate is due to the shorter interconnect length, smaller vias, and thinner dielectrics of lower dielectric constant materials. These things also improve the signal integrity.

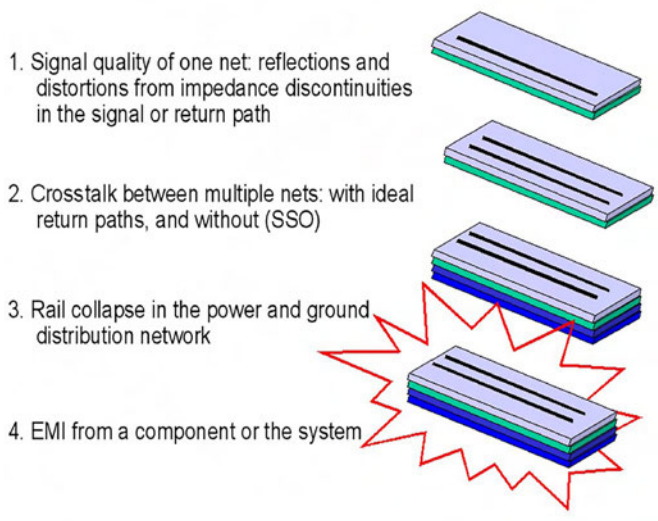


Figure 2: Four categories of SI problems (Source: Eric Bogatin[3]).

With HDI, devices can be brought so close together (both from a surface point of view and using the secondary or backside of the interconnect) that the signal may not need to be terminated. "Interconnects with a time delay shorter than about 20% of the rise time of the signal may not need to be terminated[2]." The interconnect length is given by:

$$\text{LENGTH}_{\text{short}} < 20\% \times \tau \times 12 \text{ in/nsec} \div \sqrt{[\varepsilon r]}$$

Where: $\tau$ = signal rise time in nsec, and
$\varepsilon r$ = dielectric constant of the material[2].

For a rise time of 1 nsec for FR-4, this is only 1.14 inches.

The signal return path is just as important as the signal path, and exists whether you provided for it or not. The signal return path contributes to the inductance, capacitance, and resistance experienced by the signal. The signal return current will seek the path of minimum energy, which has the least impedance. For low frequencies, this path will have the least resistance; for high frequencies, the path will minimize the current loop. At higher frequencies, inductance dominates over resistance, so the return path follows the signal path even though it meets higher resistance.

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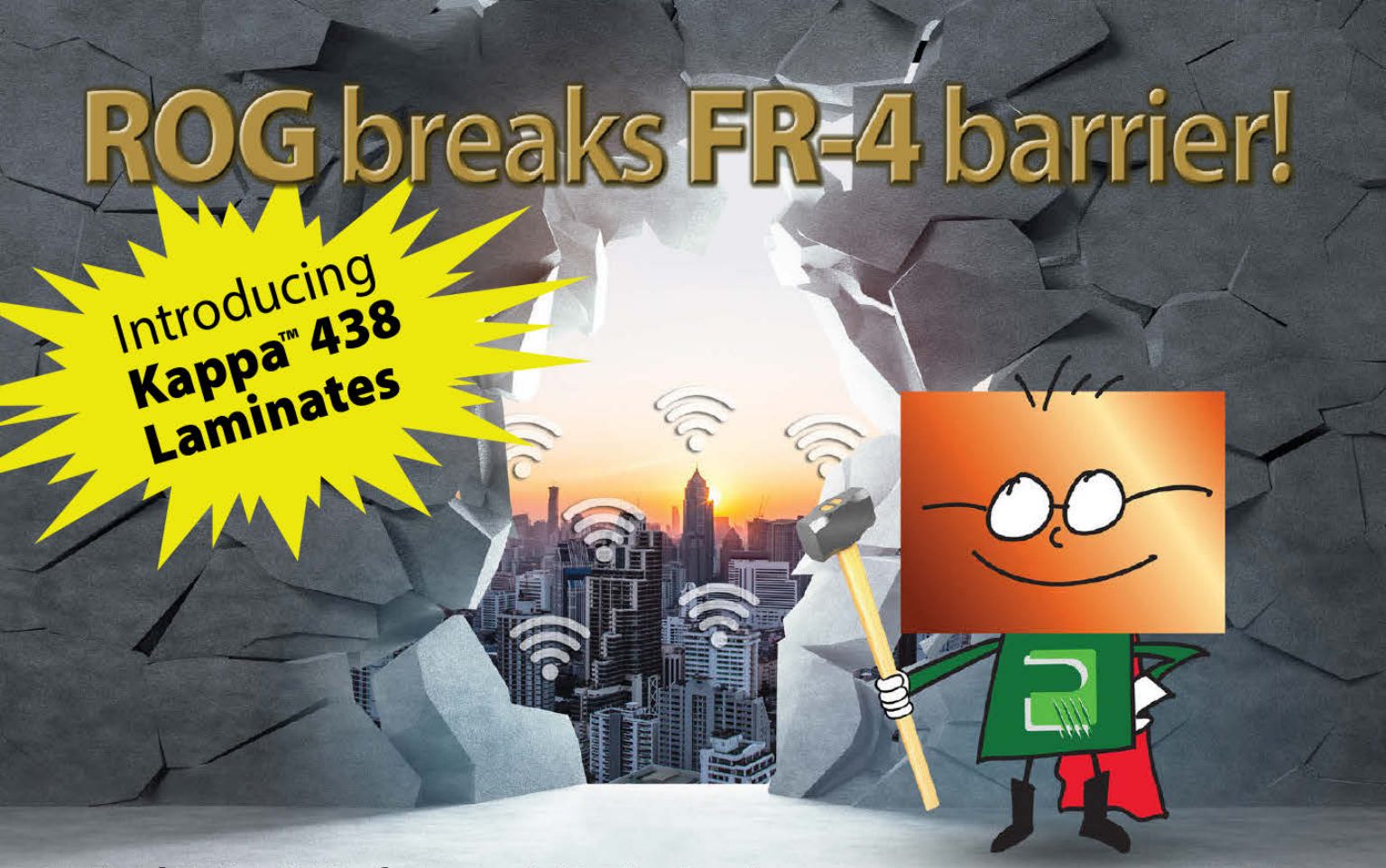

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Demand for wireless data is growing exponentially, driving a need for substantially higher levels of mobile network capacity and performance. This demand will grow further in support of the upcoming 5G IoT ecosystem where billions of devices will be communicating with each other, and connectivity is immediate and uninterrupted. FR-4 was historically a material choice for many less demanding RF applications, but changes in the wireless infrastructure related to growing performance requirements, especially in small cells and carrier-grade WiFi/Licensed Assisted Access (LAA), have resulted in instances where the properties of FR-4 are lacking, and RF performance and consistency is compromised. There's no longer a need to sacrifice your PCB performance.



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| Typical HDI Materials | Dielectric Constant* | Dissipation Factor* | Relative Costs |
|---|---|---|---|
| Liquid Epoxy Resin (thermal ink) | 3.1-3.48 | .018-.021 | 0.8 |
| NanYa CCL FR-4 Tetra-functional | 4.4 | 0.01-.016 | 1.0 |
| NanYa CCL FR-4 NP170 | 4.3 | 0.01-.016 | 1.11 |
| Resin Coated Foil | 3.1-3.5 | 0.018-.021 | 1.26 |
| Aiinomoto Dielectric Film | 3.6 | 0.037 | 1.36 |
| Isola FR406 FR-4(170) | 4.6-4.3 | 0.023-.014 | 2.09 |
| Typical Photoimageable Dielectric | 3.9-4.1 | 0.025-.020 | 2.5 |
| Nelco-4000-6 FR-4 ( 180 C ) | 4.4 | 0.012 | 4.19 |
| Isola FR408 (low Dk & loss) | 3.8 | 0.010 | 3.08 |
| Nelco - 4000-13 (low Dk & loss) | 3.9-3.7 | 0.009 | 4.19 |
| GE Getek (low Dk & loss) | 3.8-4.2 | 0.013 | 4.84 |
| Rogers R04003 (low Dk & loss) | 3.4 | 0.0027 | 15.2 |
| Rogers R04350 (low Dk & loss) | 3.5 | 0.004 | 15.62 |
| * At 1 MHz and 25 C, characteristics change with frequency, temp. and humidity | | | |

**Table 2.** Typical HDI materials employed in Asia with costs normalized to FR-4

Table 2: HDI materials and their electrical characteristics.

The low dielectric constant results from the use of many new HDI materials. Many of these materials are not glass-reinforced and thus have lower dielectric constants than glass-reinforced laminates. Many of the dielectrics are liquid such as the high-Tg epoxy or polyimide, or the photodielectric resins (PDR). Some materials are thin, vacuum-laminated dielectrics with high thermo-plastics contents. However, all materials are uniformly thin—this contributes to reductions in wiring delays and reduction in noise. Several of these new materials and their electrical characteristics are shown in Table 2. The relative cost is based on high-volume usage in Asia, including dealer markups.

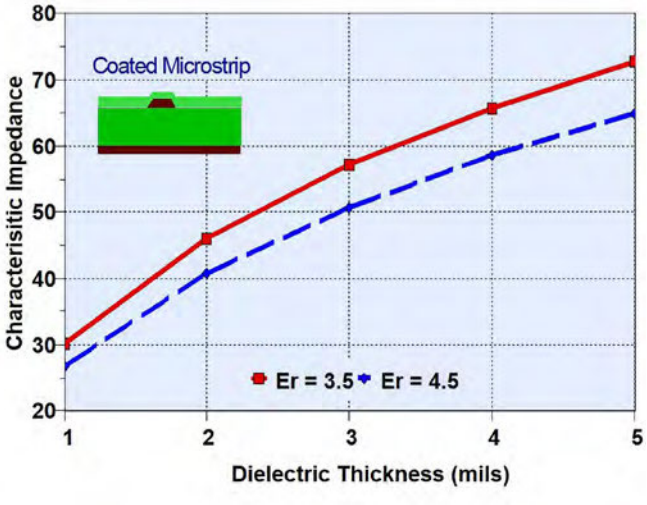


Figure 3: Characteristic impedance of lower dielectric constant materials.

Figure 3 shows the characteristic impedance for a fine-line HDI microstrip (3-mil trace) with two dielectrics of Dk equal to 3.5 and 4.5. The lower Dk allows the dielectric thickness to be nearly one to one-half mil thinner.

## Crosstalk between Two or More Nets

HDI miniaturization provides shorter interconnect lengths, and if the lower dielectric constant material is used, then cross talk in HDI substrates is reduced. Bogatin provides the following example: "A typical line width in HDI technology is 3 mils (75 microns). Figure 3 shows the characteristic impedances of 3-mil traces for various dielectric thicknesses. The dielectric thickness will be less for a lower dielectric constant. This means a lower dielectric constant material system will either result in less crosstalk for the same spacing, or the traces can be moved closer together and have the same amount of crosstalk"[3].

Bogatin continues, "The variation in the near-end cross talk coefficient with separation for two, 50-ohm microstrip traces is shown (Figure 4). In the two cases studied, the line-width was 3 mils, and the dielectric thickness was adjusted so that for the two different dielectric constants, the line impedance was the same. From these curves, it can be seen that if the routing pitch is cross talk constrained, just the lower dielectric constant of the HDI material system may allow a board to shrink up to 28%. For coupled lengths less than the saturation length, the magnitude of the near-end voltage noise will scale with length. The saturation length will depend on the rise time. For a rise time of one nanosecond, the saturation length with an effective dielectric constant of 2.5 is about 7.6 inches, which would include many of the traces in a small card application. The relative cou-

pled near-end noise would be given by the following equation:"[2]

$$\frac{V_{noise}}{V_{signal}} = \frac{len_{coupled}}{len_{sat}} K_b = \frac{len_{coupled}\sqrt{\varepsilon r}}{\tau\ 12\ in/nsec} K_b$$

Crosstalk in HDI substrates is reduced by the shorter coupled lengths and by the lower dielectric constant by as much as 50%. Shorter trace lengths will radiate less, and traces with thinner dielectric will radiate less. The example in Figure 5 shows that the shorter the coupled length, the less the mutual inductance (Lm), and the thinner the traces, the less the mutual capacitance (Cm). Moreover, the thinner the distance to the reference plane, the lower the near-end crosstalk will be, or the same cross talk for a longer coupled length. With length reductions of 2x and dielectric thickness reductions of 2x over conventional boards, the radiated field from HDI signal loops might be reduced by as much as 4x, which is 12 dB.

## Simultaneous Switching Noise and Voltage Rails

The actual circuit performance varies with the rise-time of signals. Because most of these larger/higher-performance HDI boards deal with high-speed computer busses and telecom signals, they are very sensitive to noise and signal reflections. Simultaneous switching noise (SSN) is the most difficult type of noise to control. Switching noise originates from the instantaneous demand for current as devices turn on and off. Any drop in the power supply voltage will adversely affect components, the power distribution in the board, and how devices are connected to ground. Keeping the inductance of the power and ground distribution low and the inductance to the ground connections low reduces this type of switching noise or 'ground bounce.' Conceptually, that reduction looks like the following equation:

$$\Delta V = N_{switching}\ L_{effective}\ \frac{di}{dt}$$

To manage simultaneous switching noise (SSN), the focus needs to be on:

1) minimizing di/dt;
2) good selection of decoupling capacitance;
3) careful induction management.

Reducing $L_{effective}$ can be helped by HDI techniques. The use of area array packages instead of peripheral leaded packages is one way. Watching how ground is assigned on peripheral leaded packages is another. Increasing the number of power/ground leads to packages and using a power/ground plane in the package (even a floating plane) helps. However, the major issue is board layout. Nearly 70% of BGA and QFP inductance is due to breakout routing on the PCB or the ground return path. The choice of mi-

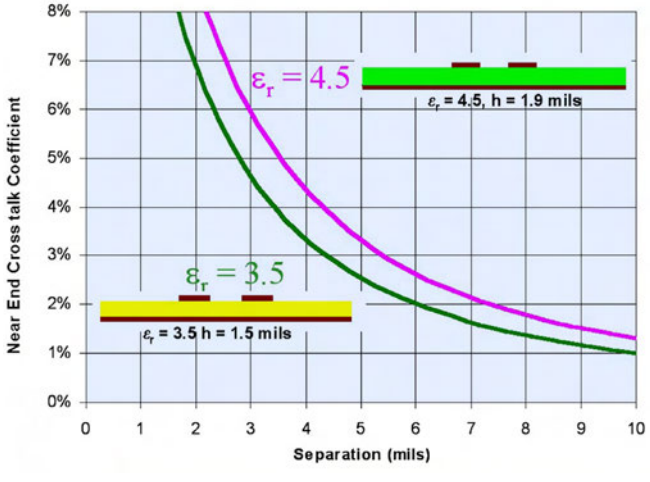


Figure 4: Near-end crosstalk coefficient (Source: Eric Bogatin[3]).

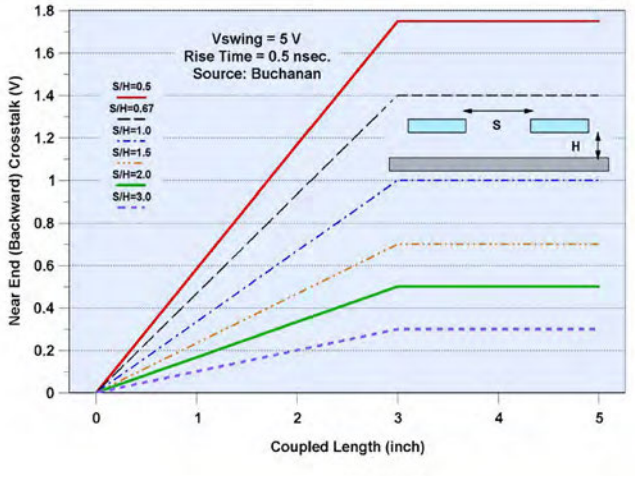


Figure 5: Crosstalk vs. length (Source: Buchanan[6]).

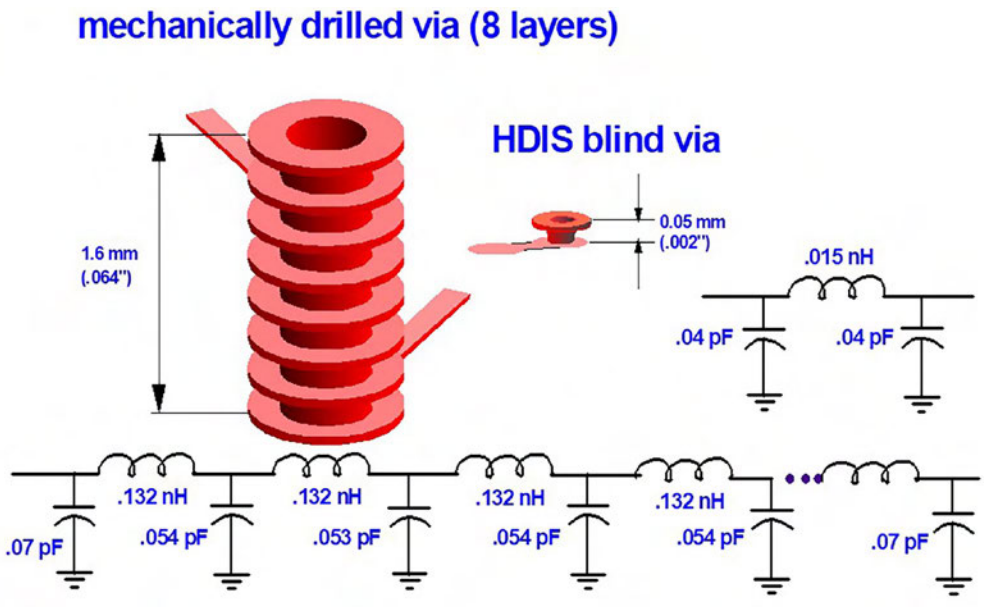


Figure 6: Via comparison.

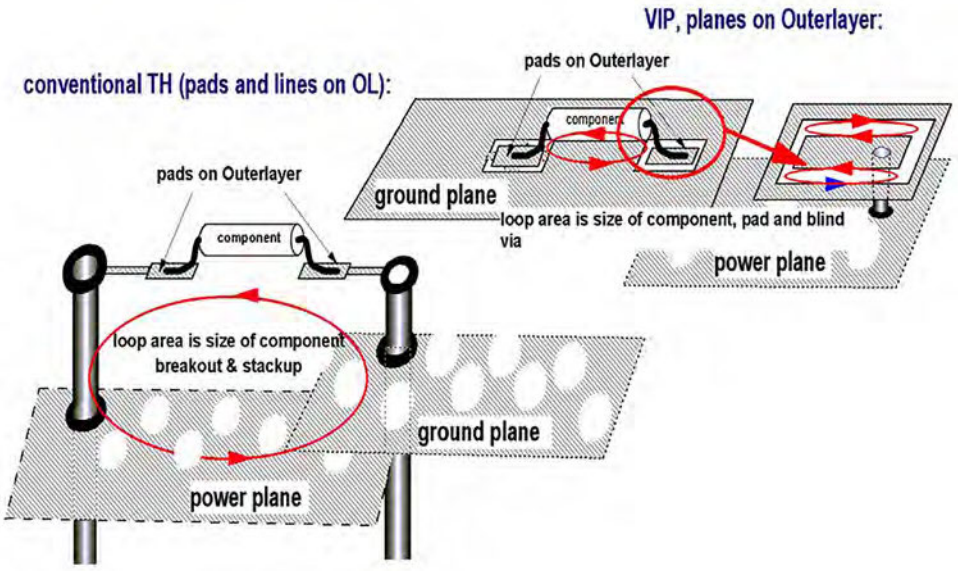


Figure 7: Loop difference.

crovias now provides an advantage. Looking at the simple lumped models of PCB vias in Figure 6 shows that the smaller microvia has nearly 1/10th the inductance and capacitance of a through-hole via.

### *Via-in-Pad and Short Via Lengths*

Bogatin's article provides the partial self-inductance of a microvia 2 mils deep and 1 mil in diameter as less than 10 pH (where pH = picoHenrys), while a drilled via, 10 mils in diameter and 32 mils deep has a partial self-inductance of almost 200 pH[2]. This is significant for higher frequency designs. Bogatin goes on to point out that at 300 MHz, the impedance of an HDI microvia is only 18 milliohms compared to the through-hole via which is 400 milliohms.

The via-in-pad reduction of inductance is even more dramatic. One of the largest sources of inductance to devices and decoupling ca-

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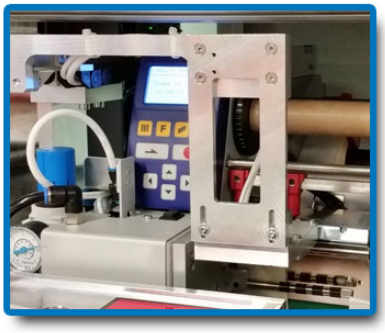

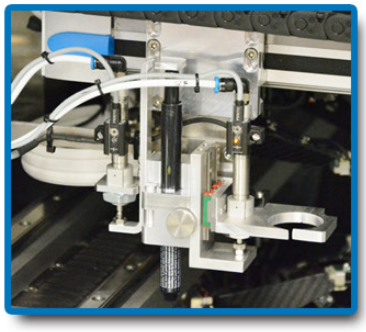

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pacitors is the trace-via combination to power and ground. By placing the microvia in the SMT pad, this inductance is decreased to practically nothing. This is compared to a conventional trace to a through-hole that at 20 mils would be as much as 500pH to the loop inductance. This loop difference is shown in Figure 7.

Using a via-in-pad microvia and a surface ground plane, there is essentially no inductance to ground, and if power is used as the second layer under the microvia, only a minimum inductance to power. The close nature of this power/ground combination will lower loop inductance and provide a significant amount of decoupling capacitance. A final advantage is the reduction of part spacing and a shortening of all the signal tracks. Figure 8a and Figure 8b show high-speed controlled impedance multilayer redesigned with only the use of microvias-in-pads[5]. No parts were changed and current assembly minimum spacing was observed. The advantages from a cost and size point-of-view is nearly 40% lower cost, from 12 layers to eight layers, and 40% smaller in size, allowing more up on a fabrication panel. The signal integrity was improved significantly.

Note that Figure 8a shows a 12-layer, controlled impedance multilayer that was redesigned employing only microvia-in-SMT pads. The original through-hole version is shown on the left side of the figure, and the microvia version requiring only eight layers is shown on the right side. Also note that Figure 8b shows the secondary side of the redesigned multiplayer, illustrating the advantage of blind vias and the via-in-pads design concept.

***Power/Ground Distribution***

Keeping the inductance of the power and ground distribution low is a major objective if fast rise-time circuits are going to be used. Two factors that contribute to the inductance of the power and ground interconnect are the physical length of the path and the separation between the actual power and ground planes.

Again, Bogatin's advice[3] is, "The use of very thin dielectric layers between the power and ground planes contributes to a very low loop inductance for the power and ground currents. For two rectangular conductor sheets, separated by a dielectric thickness, h, the loop inductance for current to go down one surface and return back on the other is given by:

$$L_{loop} = \mu_0 h \left(\frac{len}{W}\right) = h \times \left(\frac{len}{W}\right) \times 33pH/mil$$

"Where *len* is the length of the current path and *W* is the width. The loop inductance decreases as the spacing between the power and

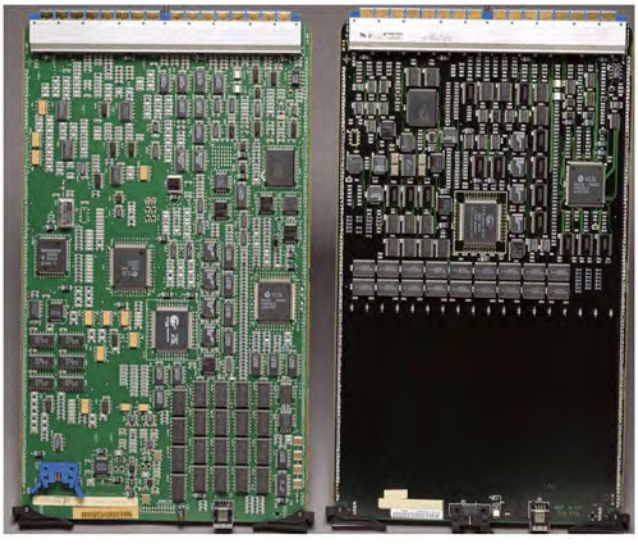

Figure 8a: Redesigned multilayer (component side).

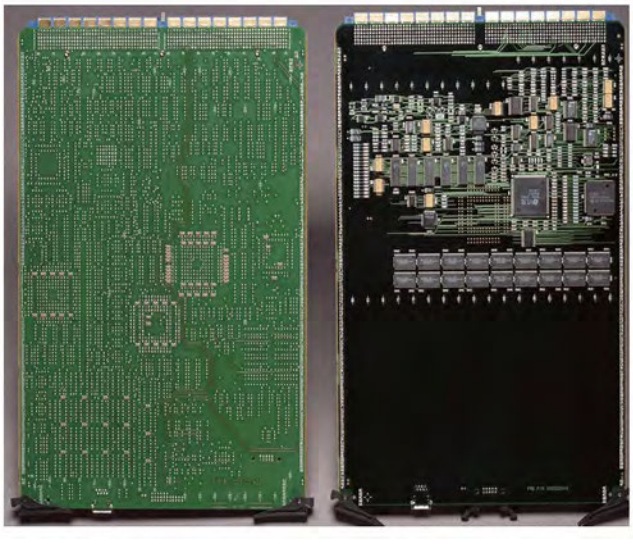

Figure 8b: Redesigned multilayer (circuit side).

ground planes drop.

"When the dielectric thickness is 1 mil, there can be as low as 33 pH/square of loop inductance. When the current travels in conductors that are shaped like a square and have the same length as width, the loop inductance is independent of the size of the square. This represents a rough approximation to the typical interconnect inductance in the power and ground planes. Between the decoupling capacitor pads and the chip attach pads, the connecting loop inductance can be about one square's worth. Thin HDI layers can keep the power and ground inductance very low[3]".

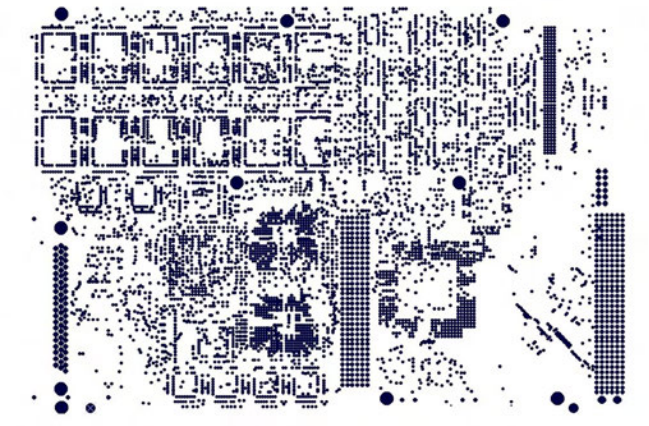

Figure 9a: Innerlayer plane ground plane relief.

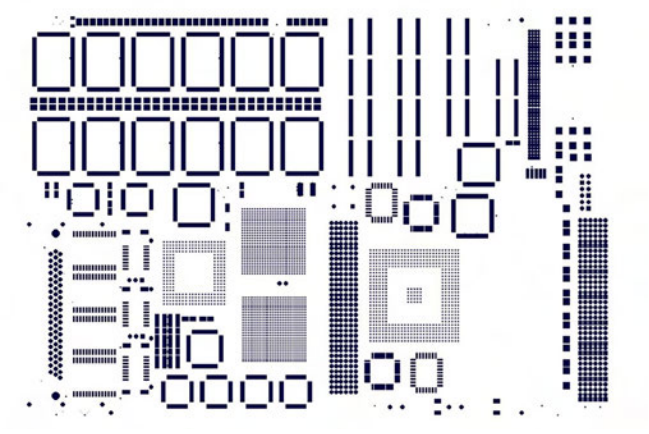

Figure 9b: Primary side ground plane relief (with the ground removed for clarity).

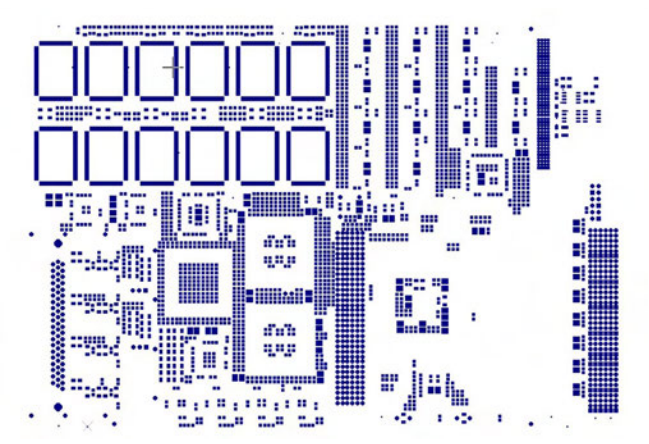

Figure 9c: Secondary side ground plane relief (with the ground removed for clarity).

**Signal Propagation and Interconnect Delay**

Higher via density, microvias (smaller vias), and via-in-pads allow components to be placed closer together, reducing wiring delays by a factor of up to 50%. Signals propagating through a transmission line have a characteristic velocity that is primarily determined by the square root of the effective dielectric constant of the surrounding medium. The reciprocal of this velocity is the signal propagation delay per unit of conductor length. This is for a classical microstrip topology, but if the conductor is located between two reference planes, then it is proportional to the square root of the material's dielectric constant:

$$\text{Propagation Delay}(ns/in) = 0.847\sqrt{\varepsilon}$$

Where: $\varepsilon$ = dielectric constant of substrate

Interconnects with a time delay shorter than about 20% of the rise time of the signal may not need to be terminated.

**EMI Radiation**

***Ground Return Path***

Voltage and current waves are supported by propagating electric and magnetic fields. The ideal return path is continuous and uniform. This is usually not the case in high-speed dense circuit boards. The more the return path is nonideal (with discontinuities), the more it produces ground loops. The ground loop of the conventional through-hole with innerlayer power and ground was discussed earlier and is shown in Figures 7 and 10. The characteristic of continuous and uniform is illustrated in Figures 9a, 9b, and 9c.

In Figure 9a, the ground planes of a high-speed dense multilayer are shown. For this 9.2-inch by 6.3-inch 18-layer board, 8.46 square inches of copper is etched away to make room for the through-holes. Figure 9b is the 10-layer HDI multilayer that replaced the original 18-layer multilayer. The surface ground plane (primary side, Figure 9b) has only 6.63 square inches removed and the secondary side (Figure 9c) has only 6.35 square inches removed. This is 21.6% and 24.9%, respectively, less discontinuities for the return path. In addition, you can see that at the fine-pitch BGA devices, the ground copper goes substantially all the way into the center ground pins.

The return signal may encounter breaks in the ground plane, which are a known source of noise, but many do not recognize that large through-hole antipads on the PWR/GND planes under finer pitch BGAs can also cause ground loops that will create noise. When generated under the BGA, ground loops are very difficult to locate. This situation is depicted in Figure 10.

## Details on Improved RFI and EMI

At 1.00 mm pitch BGAs, which are 0.040" center to center, the copper left between the antipads of a 0.013" dia. PTH is 0.007" or less. When you drop to 0.8 mm pitch devices (0.032"), a 0.013" diameter TH would wipe out all the copper. Dropping to 0.008" diameter drilled holes will provide only 0.004" of copper between the antipads. This ideal situation does not take into consideration drill accuracy and the difficulties in metallizing such a small hole. On higher I/O BGAs, only one trace can be routed out between the adjacent holes. There will be a number of signal aberrations because the reference planes will be too small. At 0.65 mm pitch (0.032"), not only do you have to use HDI, but the microvias may have to be stacked.

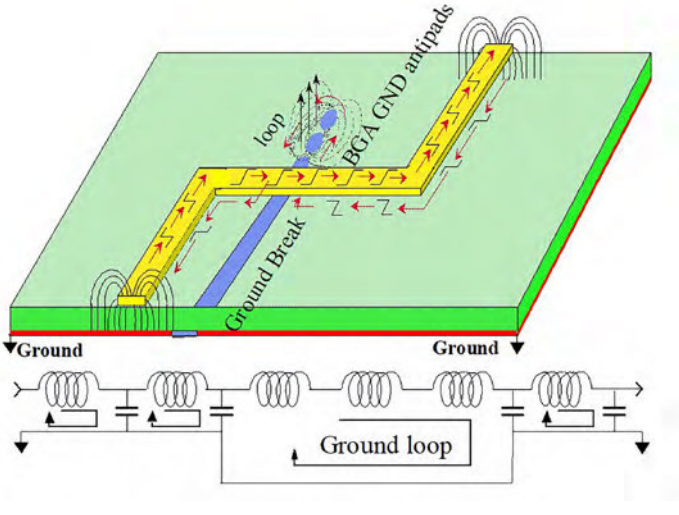


Figure 10: Ground loops. (Source: Steve Bird[7])

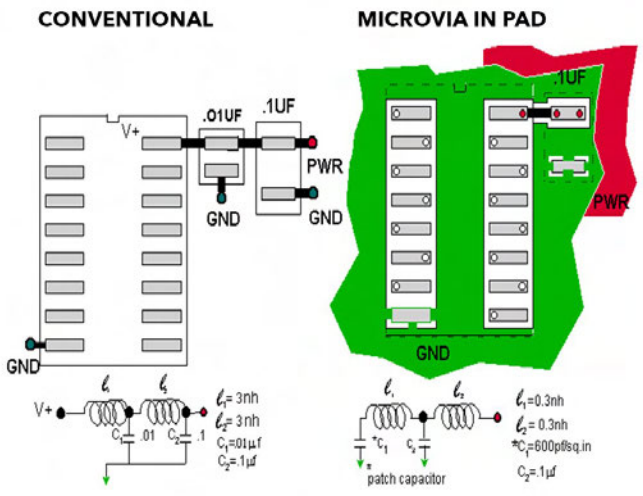


Figure 11: A comparison of conventional decoupling capacitor versus the HDI approach where GRN is flooded on the surface and PWR is layer two. (Source: Steve Bird[8])

The 22% and 25 % greater ground return area on moving GRN to the SMT layers not only reduces noise, but the two grounds on the outer layers can serve as a Faraday Cage to minimize radiated emissions.

## Decoupling

The energy storage capability of a multilayer can be significantly enhanced by HDI. Figure 11 compares the normal decoupling with an improved HDI structure. The normal through-hole multilayer is simulated in Figures 12a through 12d. The inductance of the TH vias contributes to the reduced effect of the capacitors as frequency goes up. As shown in Figures 12c and 12d, the through-holes act as excessive stubs affecting impedance, phasing, and signal reflections. The vias represent nearly 3 nH each.

Bogatin points out that "Even by using heroic efforts to get the inductance of the power and ground distribution of the substrate as

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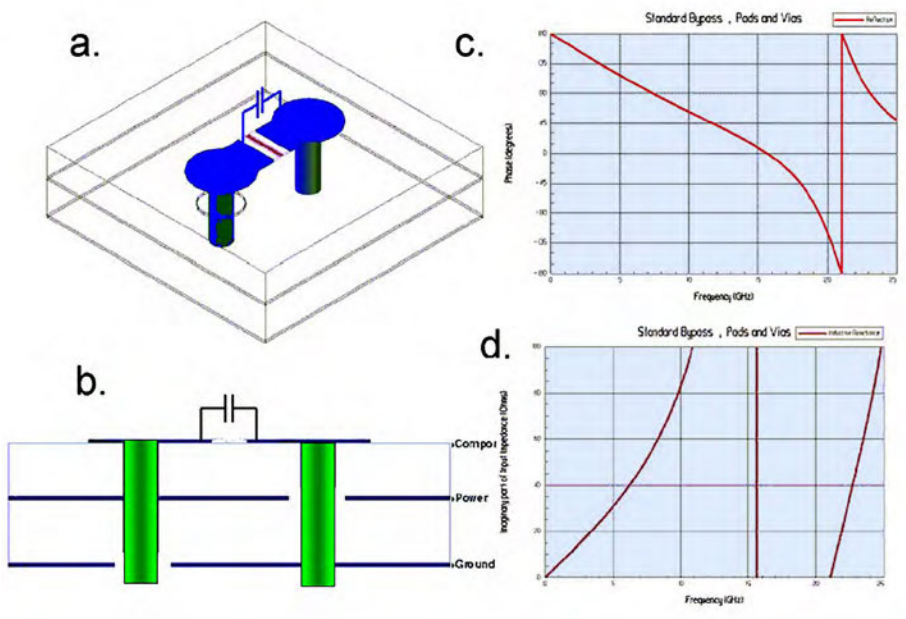


Figure 12: Simulations of TH vias on a bypass capacitor taking into account pads, traces, and vias (a, b). Results of the simulation showing (c) phase and (d) impedance. (Courtesy: C. Grasso, ANSOFT)

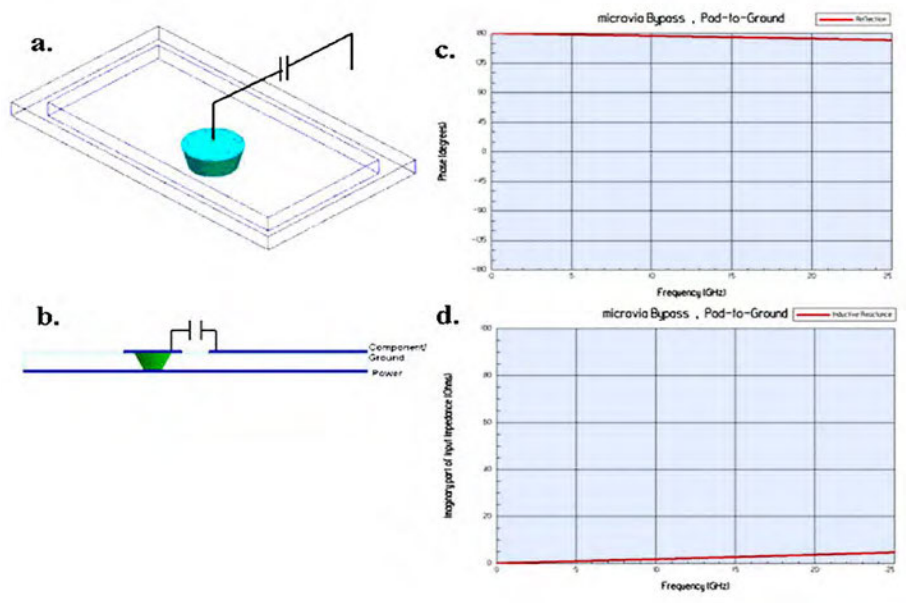


Figure 13: Simulations of a microvia bypass capacitor taking into account pads, traces, and vias (a, b). Results of the simulation showing (c) phase and (d) impedance. (Courtesy: C. Grasso, ANSOFT)

low as possible, the inductance of wire bonds can swamp any gain. With a partial self-inductance of a wire bond of roughly 1 nH/mm, and typical wire bonds on the order of 1 mm long, the inductance of one bond can be 1 nH. To reach the 10-pH range, a minimum of 200 wire bonds would be needed just for power and ground. Microvias on an 8-mil (200 micron) pitch can provide the connections for most high pin count flip chips [or BGAs]. With a solder ball length of only 5 mils (0.15 mm), the chip attach inductance can be reduced over an order of magnitude from wire bonding"[2].

The HDI structure in Figure 11 has ground on the outside with power as layer two. Microvias connect the power land to the power plane. These vias are only 40 pico-henrys, while the ground connections have no inductance or capacitance. Figures 13a and 13b are the microvia-decoupling capacitance simulation. Notice that the response in Figures 13c and 13d are almost flat. They are almost invisible to the circuit and do not affect the energy storage capability.

## Radiation

When resonances are present in a PDN, the energy usually escapes out of the end of the boards, or some components can even act as antennas and cause electromagnetic interference (EMI). As frequencies go up, this radiation becomes a bigger issue. It has been demonstrated that less noise in the PDN results in less EMI. Taking the 14-layer PCB as an example (from Ch5-HDI Handbook), we measured the radia-

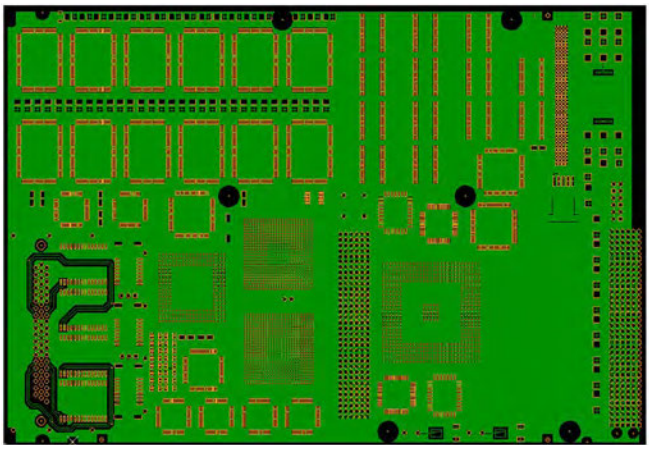

Figure 14a: Component (side A) of the 10-layer HDI multilayer redesigned from an 18-layer through-hole multilayer.

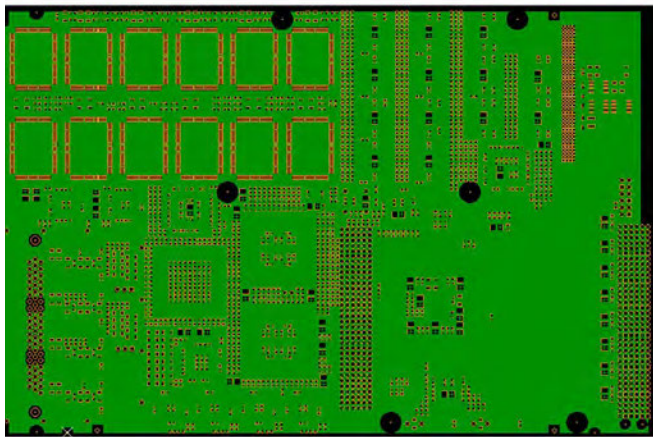

Figure 14b: Solder (side B) of the 10-layer HDI multilayer redesigned from an 18-layer through-hole multilayer.

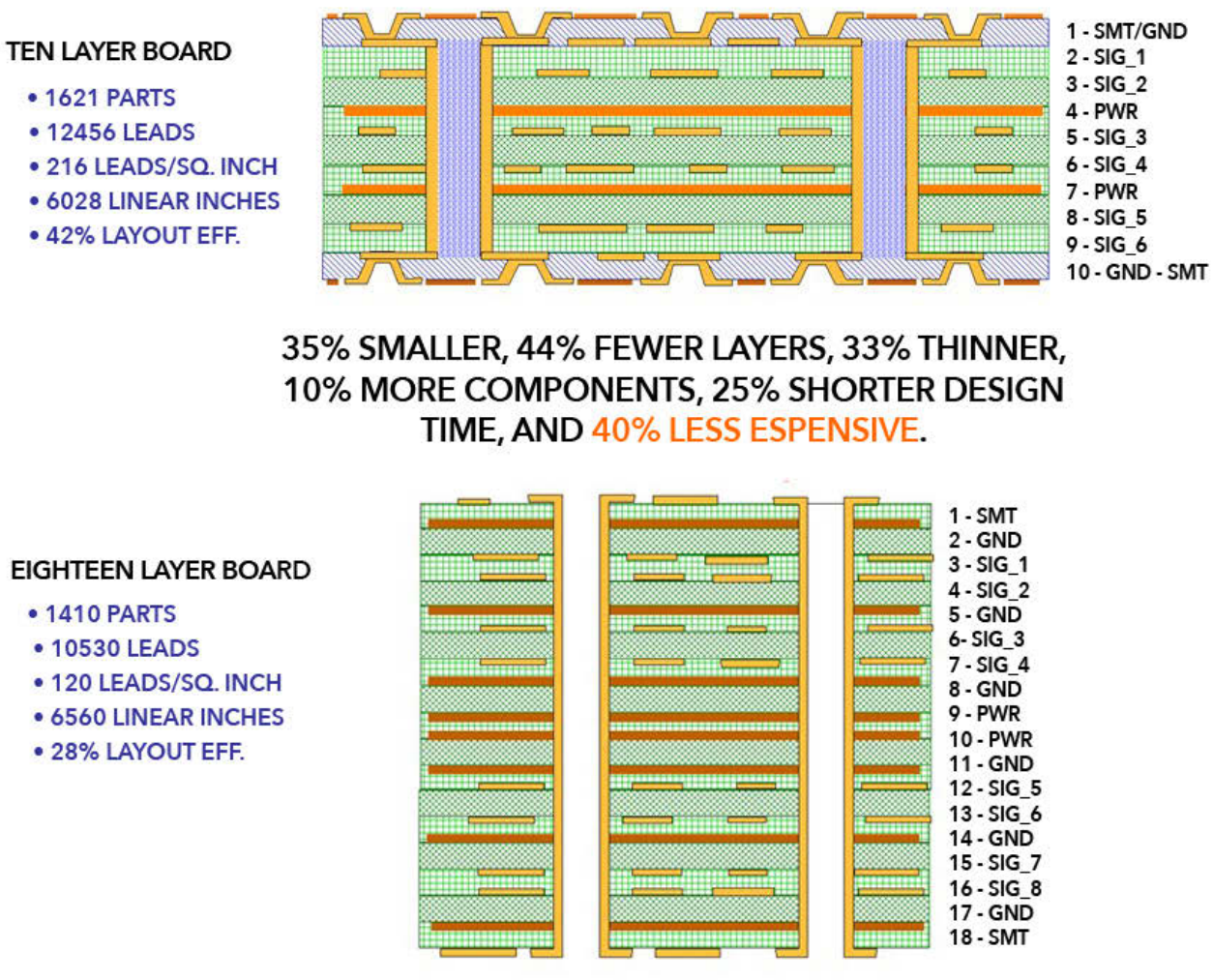


Figure 15: Cross-sections of the before and after versions of the high-performance, high-frequency multilayer board.

tion coming off the board from 1 to 7 GHz. The FCC requires testing to five-times clock frequency. Thinner dielectrics result in lower EMI. The higher $D_k$ material (in this case $D_k$ of 10 compared to 4.4 for the other material) had the lowest EMI on average, but did shift the EMI distribution. This improvement in EMI was shown by Sun Microsystems in one of their server design case study.

## Case Study of Cost, Size, Thickness and Design Time Reduction

The board illustrated in Figures 9a, 9b, and 9c not only benefited from SI improvement, but the HDI microvia version was 43% less expensive and took 30% less time to design than the through-hole version. The original board was 11.75" x 8.75", included 18 layers, and was all through-hole. The upgraded, high-speed version used two new BGAs, each with 676 pins at a 1.00 mm pitch. A microvia change was indicated. After analysis with pre-design software, the HDI version could be designed with only six signal layers for a total of 10 layers. Figures 14a and 14b show the finished design. Utilizing all via-in-SMT pad design and surface ground planes with buried vias, the board was reduced by 35% to 9.2" x 6.3". The before and after characteristics of the two designs are detailed in Figure 15.

## Conclusion

Blame it on Maxwell's equations, but SI is getting more important and… more difficult. HDI provides small geometries and dielectrics. Providing you take advantage of the other benefits of HDI, like lower costs and higher densities, SI will benefit as well. All of the problems listed get worse as signal rise times decrease. With current IC geometries shrinking, decreasing signal rise time is assured. Unfortunately, the amount of time available to solve these problems is also shrinking. The successful company will be the one that masters signal integrity problems, HDI, price reductions, and the shorter time-to-market. **PCB**

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**Happy Holden** has worked in printed circuit technology since 1970 with Hewlett-Packard, NanYa/Westwood, Merix, Foxconn and Gentex. He is currently a contributing editor with I-Connect007. To read past columns or to contact Holden, click here.

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RBP CHEMICAL TECHNOLOGY

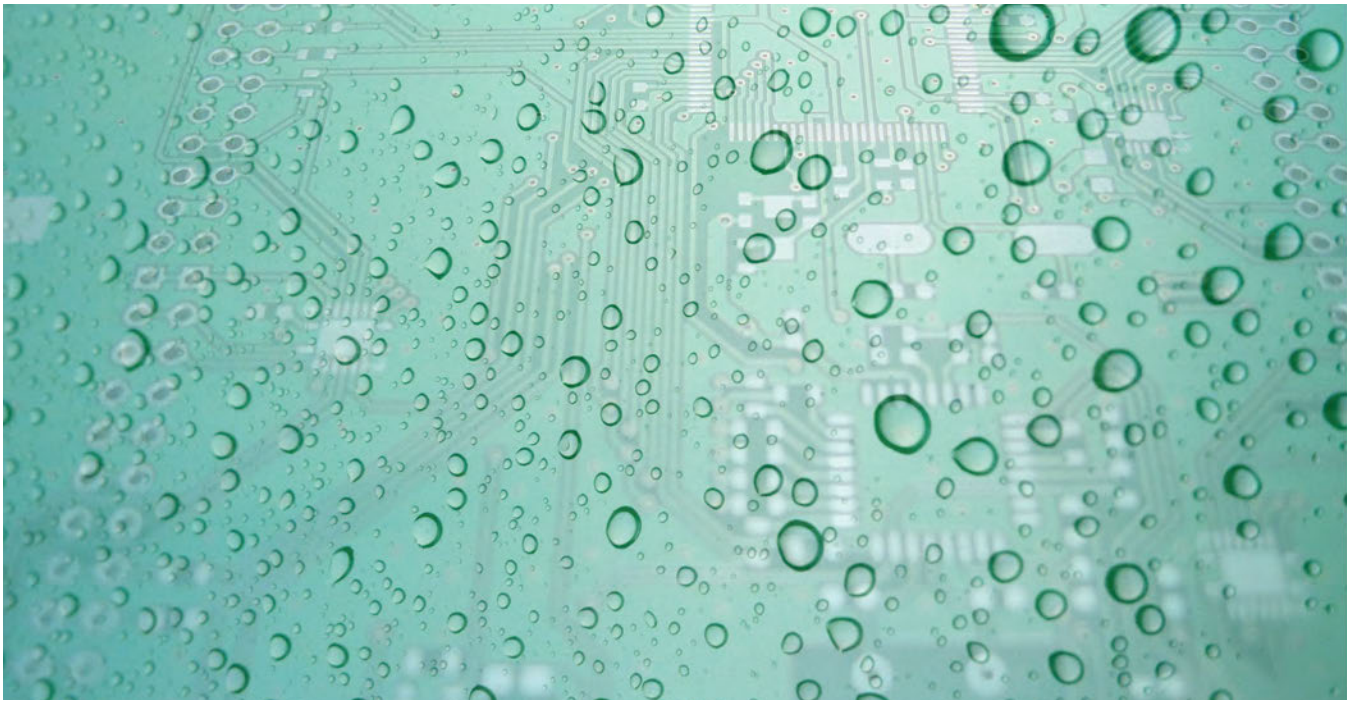
## Introduction

In Part 1 of this series on the importance of rinsing, the author presented an overview of the critical aspects of rinsing as it applies to the overall quality of a printed circuit board, with considerable space devoted to water conservation. Thus, we now turn to how one can improve rinsing effectiveness without increasing water consumption and, by default, significant waste treatment costs.

## Rinsing Protocols

The preferred rinsing method of design engineers is counterflow, or cascade rinsing. Still another theory widely held throughout our industry reasons that, if work is left in a rinse tank for longer periods of time, better rinsing will be the result. First, let's explore the idea of leaving the circuit boards in the rinse for a longer period.

When a rack of PCBs is immersed in a rinse tank, the residual surface contamination is reduced to a practical minimum within 30 seconds as the solution carried in on the surface of the work disperses into the rinse waters. A typical rinse tank—100 gallons with a water flow of five gallons per minute—would decrease the concentration of the solution contaminants at a rate of only 5% for each minute that it remains in the rinse tank. Leaving the work in any longer would have virtually no effect. This demonstrates that rinsing time in a rinse station is a non-linear relationship with respect to removing contamination from the surface of the parts. Yes, this is counter intuitive. We often think that if two minutes in the rinse removes 50% of the residues, then doubling the time in the rinse will remove 100%! This is not the case. Basically, the law of diminishing returns applies. There are many factors in play here in-



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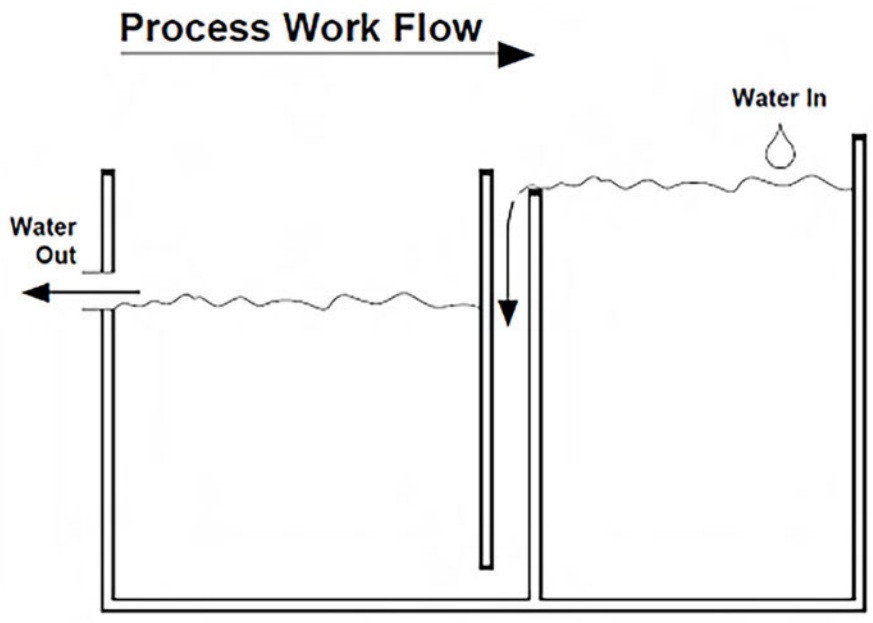


Figure 1: Counterflow rinse diagram. (Source: IPC 740)

cluding the type of contaminants to be rinsed, affinity of those contaminants to adhere to the printed circuit board, etc.

It is more desirable to have brief exposure times in many (presumably cascade) rinse tanks, which will result in a better dilution rate of the contaminants, than a long exposure time in just a few rinse tanks.

There have been countless studies performed on rinsing mechanisms and how to improve rinsing efficiency. Most of the published studies related to rinsing are based upon multitudes of calculations of volume of water flow relative to number of rinse tanks in use[1,2].

## Discussion

Although an absolute rinsing standard for all chemical processes in the PCB industry is unattainable, studies have shown that rinsing can be optimized using many rinse tanks, and the appropriate hang times. While the manageable levels of contaminants vary for different processes, we know that a good dilution rate equates to good rinsing across the board. Determining the appropriate hang time of a panel above the process solution helps to improve the dilution rate, without incurring more water consumption. Research showed that increasing the hang time can decrease rinse water usage, but also that one can determine an optimum hang time. Beyond the optimum hang time, allowing the panel to drain longer further benefits diminish. The results of this optimization will give increased quality of final product with fewer rejects, decreased chemical costs, and lowered burden on waste treatment systems.

Now, there are a few other factors in play here. As we know, circuit boards are flat pieces with many vias in them. Most plating operations (not all) are designed to process the panels in a vertical mode. Higher aspect ratio vias will trap more solution than larger diameter vias. Regardless of the panel thickness and via size, one must contend with drag-out. One can decrease the amount of drag-out by:

- Increasing hang time of the panels to insure more solution falling back into working tank
- Tilting the panels at a slight angle to in sure better drainage (especially helpful for small diameter vias and thicker boards)
- Withdrawing panels slowly from the working tank

Several additional techniques can be employed to not only improve the quality of the rinsing, but also reduce water consumption. These are described below.

### *Counterflow or Cascade Rinsing*

Basically, a single water source flows through multiple rinses in a direction opposite or counter to the flow of the work being processed (Figure 1). Counterflow rinses provide the benefit of multiple rinse stations, but use the water flow of a single rinse. Therefore, rinsing can be greatly improved without using additional water. Both immersion rinse tanks and spray rinse systems can be counterflowed.

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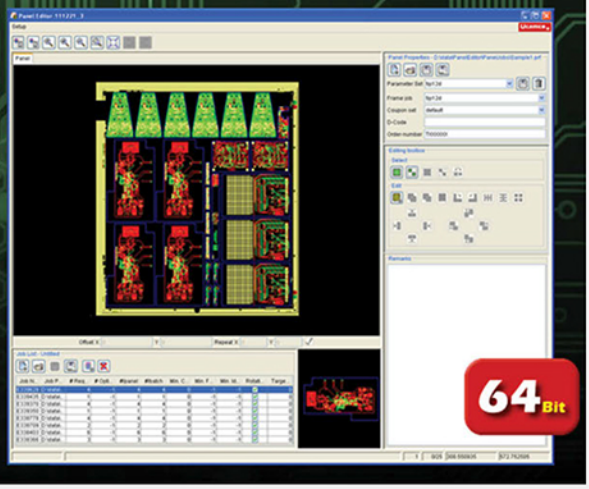


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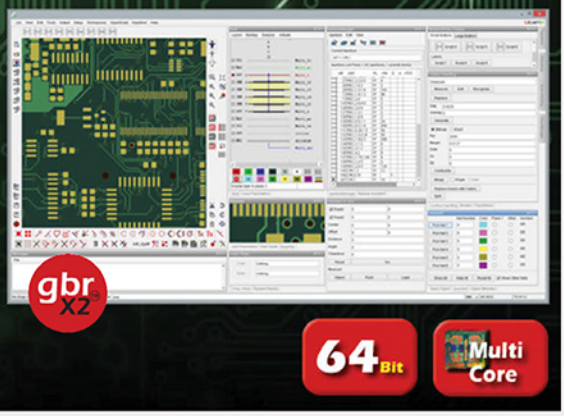


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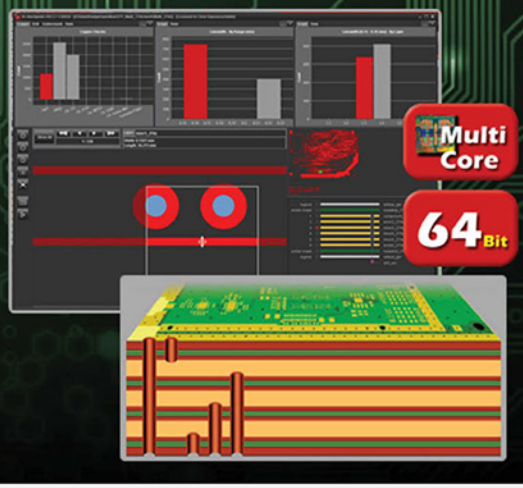


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### *Use of Air Agitation*

Air agitation improves rinsing in two ways: by keeping the rinse water mixed so that concentrated pockets do not occur, and by continuously moving fresh water to the board surface. Air agitation should not be used in rinses immediately after cleaners with a tendency to foam. There are many low foaming cleaners available today. The process engineer should evaluate carefully prior to implementing such a product in production.

### *Spray Rinsing*

Spray rinsing is an effective method to rinse contaminants and process solutions from circuit boards. However, if not controlled properly, there will be a huge amount of water consumed. This can be a very effective way to rinse.

It is easy today to control the amount of water used in spray systems with on-off switches. Meaning that the spray is activated when the boards enter the rinse station. And the rinse is then switched off after the panels exit the chamber. This is not an easy thing to accomplish if one is using a manual operation.

Another concern with spray rinsing is that smaller diameter vias (and thicker boards) do not clean up as well when compared to immersion rinsing or countercurrent rinsing.

### Summary

Improved rinsing techniques often do not require additional water use. Many techniques are both inexpensive and easily implemented, once understood. Some of these techniques include air agitation, sprays (continuous, time or pulsed), counterflows, tempering, longer drip times and new rack designs. Use the tools available and one will not only conserve precious water, but will also ensure a high quality final product.

To ensure the highest quality printed circuit board, do not short change the critical importance of rinsing. **PCB**

### References

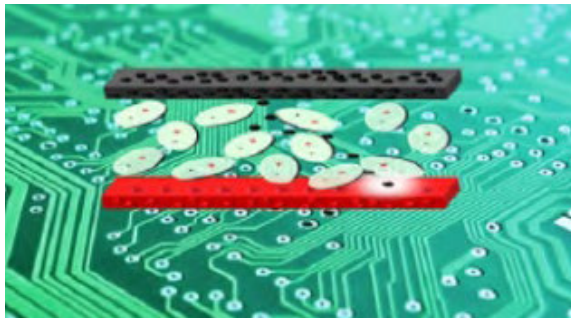
1. T. Mooney, "The Art and Science of Water Rinsing," Metal Finishing Handbook, 1996, p. 135.

2. J.P. Gong, K.Q. Luo, and Yinlun Huang, "Dynamic modeling and simulation for environmentally benign cleaning and rinsing," Industrial and Engineering Chemical Research (1997), pp 63–70.

**Michael Carano** is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.

# Bringing Signals into Phase

How we use and generate electricity has changed dramatically over the past century yet the basic components that control its flow remain remarkably similar. Researchers at KAUST have now developed a novel type of component that could improve the performance of electrical circuits.



Electronic circuitry is traditionally constructed from three primary elements: a resistor, a capacitor and an inductor. A sinusoidal electrical signal passing through these devices will change in signal strength, or amplitude, and the relative timing of the crest of the wave, known as its phase. A resistor will change amplitude only while a capacitor and an inductor can also change phase, but only by exactly one-quarter of the length of the wave, or 90°. Components that could alter the phase of the electrical signal by a different amount would enable electrical circuits with more varied functionality.

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# Become an EXPERT!


**by Keith M. Sellers**
NTS-Baltimore

A year ago, I wrote a column for this magazine that focused on utilizing the experience and knowledge of others to help simplify your life and job. I specifically talked about IPC and how the organization has become a key cog in the machine that is the PCB industry. Specifically, I discussed IPC's Validation Services division and their Qualified Products List (QPL), Qualified Manufacturers List (QML), and Qualified Test Laboratories list. In addition, I talked about the Defense Logistics Agency (DLA), which supports the Department of Defense (DoD). These are all great resources for finding the expertise you might need to help you along your path. But what I failed to mention in that article was the idea of becoming an expert yourself.

Training courses can be found everywhere. All of us have received e-mails and flyers about becoming a better manager, or how to multitask, or how to motivate co-workers…but sometimes it's more difficult to find training specifically geared towards the PCB industry itself. That said, IPC has developed a group of courses, with certifications, that can help you learn more about the products that you are creating/developing/producing as well as keep you up-to-date on any potential changes within the industry.

Currently, there are six training and certification programs overseen by IPC that cover the main areas of PCB/PCA (printed circuit assembly) production:

### IPC J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

IPC J-STD-001 is the preeminent document for all things pertaining to assembly manufacturing. For this training course, specifically, soldering materials and processes are discussed at length, with example images and requirements supplied in the documentation to assist the trainee in understanding acceptable and unacceptable manufacturing situations.

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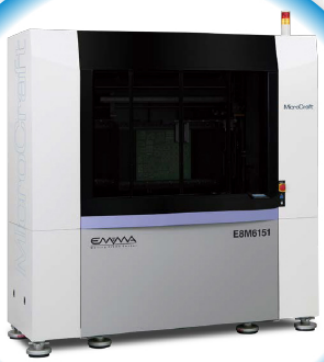

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**IPC-A-600 Acceptability of Printed Boards**

IPC-A-600 is the must-have training for understanding the acceptance criteria associated with printed circuit boards. Like IPC J-STD-001, this training explores the numerous examples of acceptable and non-conforming conditions at the board construction level that are contained within the document. Trainees are specifically educated on PCB quality, providing the backbone for a more complete understanding of the printed circuit board manufacturing process.

**IPC-A-610 Acceptability of Electronic Assemblies**

IPC-A-610 is the most widely used standard that IPC governs and is the cornerstone of most PCB PCA QA departments around the world. The training focuses on various product acceptance criteria, as shown in the document, and explains a variety of topics pertaining to PCA construction, typically paired with IPC J-STD-001.


**IPC/WHMA-A-620 Requirements and Acceptance for Cable and Wire Harness Assemblies**

Simply put, this training and supporting document are the A-600/A-610 for cable and wire harnesses. Classification criteria for various characteristics are summarized and taught, similar to the other documents described above, with "target," "acceptable," "process indicator" and "defect" conditions all explained with both text and visual aids.

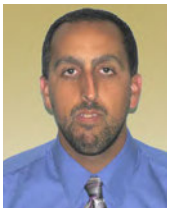
**IPC-6012 Qualification and Performance Specification for Rigid Printed Boards**

Tied to IPC-A-600 for reference and support, this training and document are dedicated to rigid PCBs. As with the other programs described above, acceptance testing and requirements are taught and explained to ensure a needed level of quality conformance understanding.

**IPC-7711 & IPC-7721 Rework of Electronic Assemblies & Repair and Modification of Printed Boards and Electronic Assemblies**

The last of the training courses is a bit different than the others. This training involves a significant amount of hands-on instruction with respect to rework processes and techniques. The document itself provides guidance on the topics of rework, repair, and modification of various component types and styles and is a how-to guide for "fixing" a component yourself!

Of course, there are many other training courses out there in the world that you can also explore. I simply chose to discuss the ones that are at the core of the PCB industry and the ones that are the most well-known. Many resources are out there for other topics that support the PCB industry—microsectioning, failure analysis, non-destructive inspection techniques, etc., just to name a few. Ultimately, you must determine the amount of knowledge needed or desired and then strike out on your own to find such information. Finding an expert can be a somewhat easy venture, but becoming an expert is a far more scenic journey. **PCB**



**Keith M. Sellers** is operations manager with NTS in Baltimore, Maryland. To read past columns or to contact Sellers, click here.

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**Let's Talk Testing: Professor Plum in the Library with the Candlestick...Right?**

Who knew that a phrase from a decades-old popular board game could have some relevance in today's ever-changing world? In the game of Clue, simply put, evidence is collected and then used to solve a mystery. In my world, testing is performed to gather data/results (evidence) and then this information is used to determine the root cause of some issue that is under investigation (solving the mystery).

**Saab and Adani to Collaborate on Aerospace and Defense Projects in India**

Defense and security company Saab and Indian infrastructure conglomerate Adani Group announced a collaboration plan within aerospace and defense in India, aligned with the Government of India's Make in India initiative.

**AT&S Enables "Cool" Designs for Miniaturized High-Power Applications**

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**The International Paris Air Show with ASC's Anaya Vardya**

The International Paris Air show is the crème de la crème of the world's trade shows. This is the big one, where all the aircraft, airline and defense aerospace companies meet to introduce new products, discuss the future of aviation, and make deals. This year I decided to talk to my friend Anaya Vardya, ASC's president and CEO, about the show, why he goes, and what it's like.

**Thin, Flexible Device Could Provide Efficient Cooling for Mobile Electronics—or People**

Engineers and scientists from UCLA, and SRI International, a nonprofit research and development organization, have created a thin flexible device that could keep smartphones and laptop computers cool and prevent overheating.

**New Cadence Allegro DesignTrue DFM Technology Accelerates New Product Development and Introduction Process**

Cadence Design Systems, Inc. announced Cadence Allegro DesignTrue DFM technology, the industry's first solution to perform real-time, in-design DFM checks integrated with electrical, physical and spacing design rule checks.

**DARPA Rolls out Electronics Resurgence Initiative**

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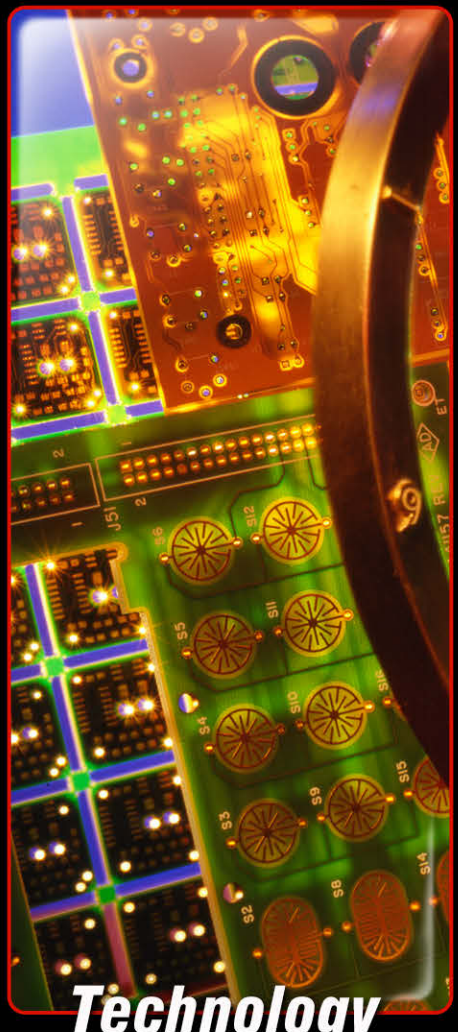


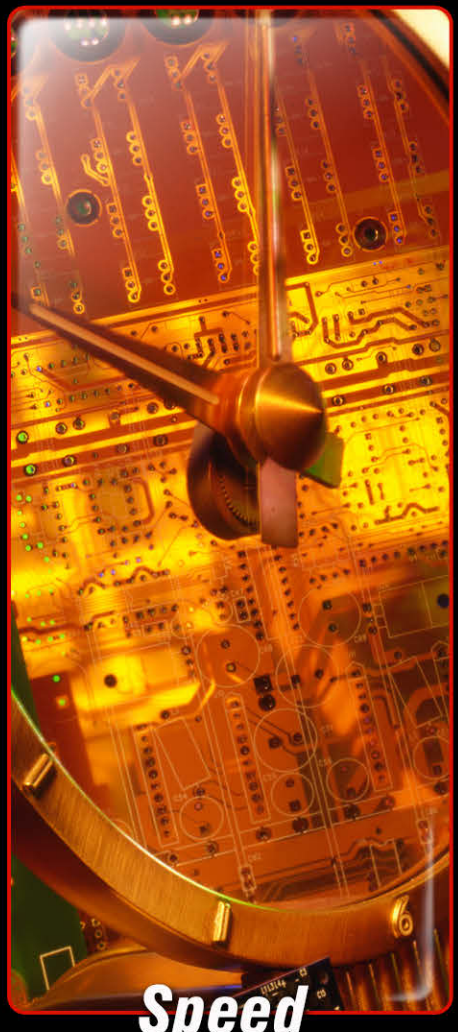


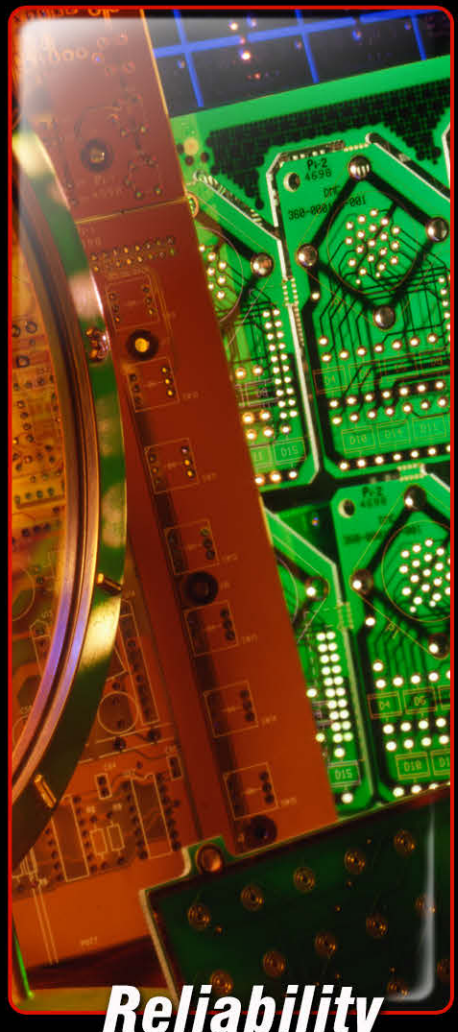


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# Steve's Particular Set of Skills (to become a World-Class Quality Manager)

**by Steve Williams**
THE RIGHT APPROACH CONSULTING

## Introduction

Being a quality professional today is nothing like it was 20 or 25 years ago; on a personal level, I can attest to this fact. It is no longer adequate to appoint a quality manager simply based on a person's command of acceptance criteria and industry specifications; in the 21st century, a truly hybrid executive is needed.

## The Quality Manager Position

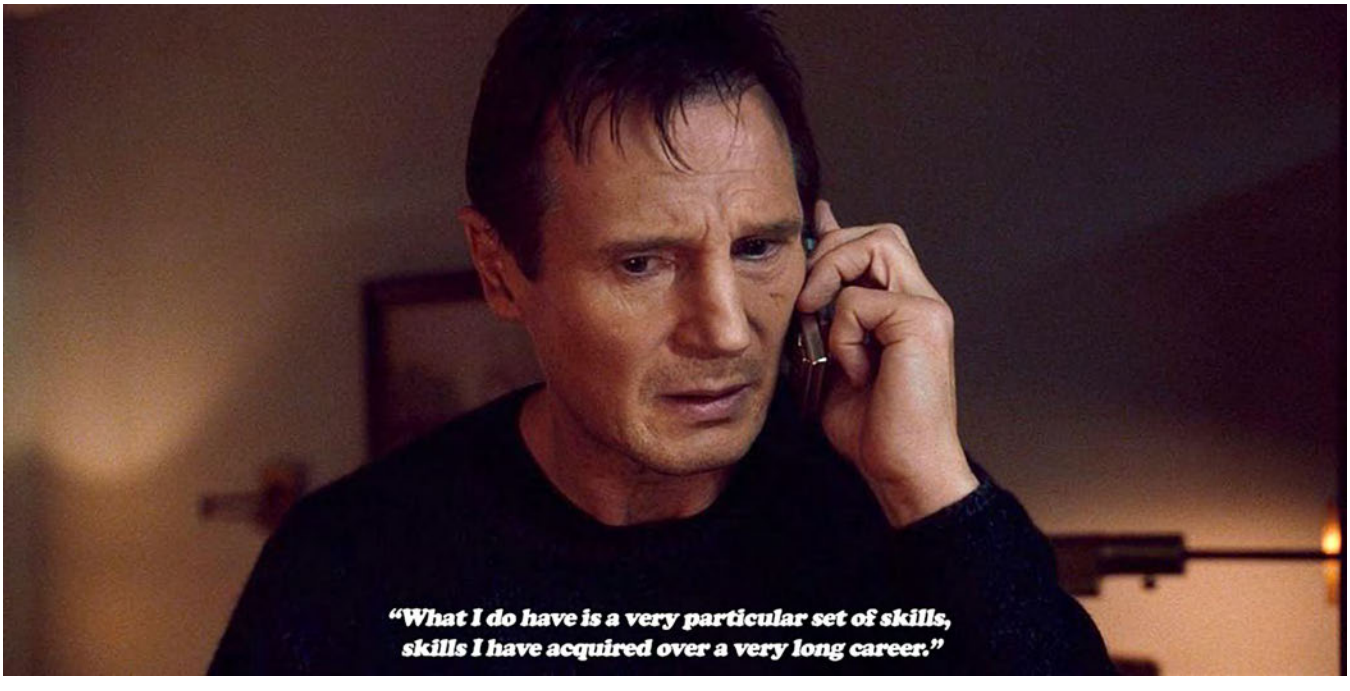
One of the most important decisions a company can make is the selection of the person that will lead the quality organization. This person will most likely be the face of the company with customers, suppliers, and your ISO registrar as the organization's ISO management representative. To differentiate yourself as a world-class organization, the skill set of your senior quality professional must go way beyond the requisite technical competencies called for in the job description.

In this column… "What I will be sharing with you are a very particular set of skills—skills I have acquired over a long career. Skills that will make you a nightmare for any auditor looking to slap you with numerous findings. Skills that will enable you to elevate your organization from the middle of the pack to the rare air of the exceptional." (As a side note, after seeing the 2008 blockbuster movie "Taken," I called my friend Liam Neeson and gave him hell for stealing this skill set quote of mine for his character Bryan Mills!)

## Steve's Particular Set of Skills

### 1. Charisma

Quality management is all about influence; the more influence you have, the more effective you will be. Quality oversees the performance of the entire organization, and must manage this through influence and motivation and not

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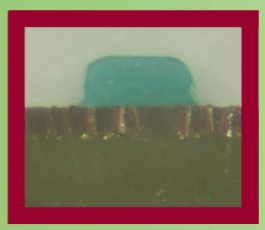

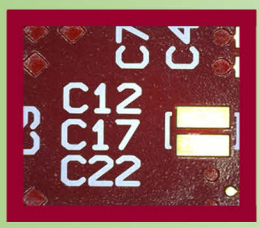


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through direct authority. The charismatic leader inspires the best from others, and one of the best measurements of a quality manager is the performance of those that he influences. Getting results through others is the key trait of a manager, and getting results through others enthusiastically and willingly is the key trait of a leader. This requires charisma—the ability to lead others who want to follow.

## 2. Political savviness

Organizational politics exist in any company, and to claim to not get involved in them is both fruitless and foolish. From the 50-employee mom-and-pop shop to the Fortune 500 company, office politics are a part of life. The key is to both acknowledge and manage it. The ability to play nice with others is a skill that will serve you well not only in business, but in life in general. This extends to customers and suppliers; I have known more than a few quality managers who made a career-limiting decision because they didn't consider the political implications.

"The ability to play nice with others is a skill that will serve you well not only in business, but in life in general. This extends to customers and suppliers."

## 3. Sense of humor

Humor is a character of strength, and as Dwight D. Eisenhower once said, "A sense of humor is part of the art of leadership, of getting along with people, of getting things done." The mastery of when to use it appropriately, and just as importantly, when not to, differentiates an adequate from a world-class quality manager. Humor can put people at ease, foster trust, and diffuse a difficult or contentious situation. Use it wisely!

## 4. Practical business sense

It is often said that engineers and quality folks don't have an appreciation of cost, and this is certainly a fair critique. The successful quality manager needs to balance the best interests of the customer with the best interests of the company, and cost can be an important consideration. Just as engineers sometimes overdesign a product, quality managers sometimes don't consider the financial implications of their decisions. Most times there is more than one way to do the right thing. Decision-making with a cost/benefit mentality is key to the success in the quality manager position.

## 5. Marketing mindset

Today's quality manager, along with every manager, must wear a sales hat along with their functional hat. What I mean by this is, every decision a quality manager makes must be made through the lens of the customer. How will this be perceived? What light does this put my company in? Can I make this into a win-win? These are all questions that the quality manager needs to think through on every decision.

## 6. Innate understanding of human nature

Having a working knowledge of human nature, behavior and psychology will be the difference when negotiating a successful resolution of a difficult situation. Like playing chess, you must always be three steps ahead of the other person, and to do that in business you need to anticipate reactions and plan counter reactions. Whether working with an internal employee responsible for scrap, or with your customer on a product warranty issue, your skill level on this will determine the outcome.

## 7. Ability to convert tribal knowledge

Tribal knowledge is the entirety of a company's expertise, experience, tricks of the trade, and idiosyncrasies of the job that have been learned by employees that may not be captured anywhere. Why is this on the quality manager? It's not—it is on everyone, but the quality manager is on point here. Driving the organization to implement best practices is clearly a

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role a world-class quality manager should not only fill, but embrace. Converting this tribal knowledge into a sustainable system is part of preserving how your company "makes its sausage," and is critical to a company's long-term survival.

## 8. Personality that fosters trust and confidence

I have seen a great many technically competent quality managers epically fail because of their people skills. This goes along with charisma in that the way you relate to others will greatly impact your success. It is critical that employees, management, suppliers and customers trust the quality manager, and have confidence that he/she will be a good steward of their interests. You can build trust by being honest, using good judgement, being consistent, and focusing on the problem, not the personality.

## 9. Ability to remain calm under extreme pressure

Now this is a skill that is mandatory for a world-class quality manager to possess; as they say, never let them see you sweat! By definition, working in quality is a nonstop, high-stress environment where emotions run high when discussing things that went wrong. It is imperative for the quality guy or girl to remain cool, calm and collected in the face of product quality challenges and be seen as the adult in the room. The ability to manage your emotions and remain calm under pressure has a direct link to your performance. A recent survey by TalentSmart that included more than a million people found that 90% of top performers are skilled at managing their emotions in times of stress in order to remain calm and in control[1].

Calmness is contagious, as is agitation. The quality manager often needs to keep people focused on finding a solution without finger pointing, fault finding or creating drama. Problems are hard enough to manage on their own without adding to the problem with emotion. Let's take a lesson from sports; it's not the best athlete or team that always wins. Instead, it's the athlete or team that is best able to maintain their composure and stay calm under the heat of intense competitive pressure that is most successful.

## 10. Ability to be part of the solution

I work with a lot of first-time quality managers, and one of the first things we typically need to overcome is the tendency to feel their job is done once they identify and communicate a quality problem. For example, issuing a corrective action to manufacturing with the "get this back to me when you figure out what happened and have fixed it" attitude. There is enough natural conflict between quality, manufacturing, engineering and sales without creating a quality silo; we are all on the same team and want the same thing—customer satisfaction. Did the quality manager create the problem? Probably not. Does he or she have significant engineering or manufacturing expertise? Probably not. But they can damn sure be part of the solution! World-class quality managers roll their sleeves up and get their hands dirty right next to the operator and figure it out together. One of the most powerful questions a quality manager can ask is "How can I help you?"

### World-Class Roadmap

I have put pen to paper outlining Steve's Particular Set of Skills for quality managers that want to step up their game, but also as a type of job description for companies looking to hire a world-class quality professional. Good ones are hard to find; exceptional ones are even harder, but following this roadmap makes it possible to grow your own. Relentless dedication to developing these 10 skills will guarantee results and put the average quality manager on a path to achieve greatness. **PCB**

### References

1. www.talentsmart.com

**Steve Williams** is the president of The Right Approach Consulting LLC. To read past columns, or to contact Williams, click here.

# 2017 Programs

## August 9
**Wisdom Wednesday** — Webinar
*Members Only*

## September 13
**Wisdom Wednesday** — Webinar
*Members Only*

## September 16–21
**IPC Fall Committee Meetings** — Meeting
*held in conjunction with SMTA International*
*Rosemont, IL, USA*

## October 3–4
**IPC & WHMA Wire Harness Manufacturing Conference** — Conference
*Paris, France*

## October 3–4
**IPC Technical Education** — Workshop
*Paris, France*

## October 9–10
**IMPACT Europe** — Meeting
*Brussels, Belgium*

## October 11
**Wisdom Wednesday** — Webinar
*Members Only*

## October 17–18
**IPC Flexible Circuits-HDI Forum** — Conference
Tutorials and Technical Conference
*Minneapolis, MN, USA*

## November 8
**IPC Technical Education** — Workshop
*held in conjunction with PCB Carolina*
*Raleigh, NC, USA*

## November 8
**Wisdom Wednesday** — Webinar
*Members Only*

## November 14–17
**IPC Committee Meetings** — Meeting
*held in conjunction with productronica*
*Munich, Germany*

## November 14–17
**IPC Hand Soldering Championship** — Competition
*held in conjunction with productronica*
*Munich, Germany*

## December 6–8
**HKPCA International Printed Circuit & APEX South China Fair** — Conference and Exhibition
*Shenzhen, China*

## December 13
**Wisdom Wednesday** — Webinar
*Members Only*

IPC Fall **STANDARDS DEVELOPMENT** Committee Meetings

**September 16–21, 2017**
**Rosemont, Illinois**

Co-located with SMTA International

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- Cleaning & Coating
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- High Speed/High Frequency
- Packaged Electronic Components
- Printed Board Design Technology
- Printed Electronics
- Process Control
- Product Assurance
- Product Reliability
- Rigid Printed Boards
- Testing

**For more information, visit www.ipc.org/fall-meetings.**

**For more information, visit www.IPC.org/events**

# Pursuing New Solutions to the Electronics Sectors' Skills Gap

**by John Mitchell**
IPC–ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

As I have written here before, the skills gap is a chronic problem in the American electronics manufacturing sector.

In a recent survey of our U.S. member companies[1], most said they have a hard time finding local talent to run their businesses. Respondents cited many essential skills that are in short supply, but the most common ones are soldering for production jobs, and engineers with industry experience, especially in process, test, and quality control. Making matters even more challenging, as new innovations emerge, new skills requirements emerge as well.

According to the National Skills Coalition, 53% of U.S. jobs are "middle skill," meaning they require some form of post-secondary education and training beyond high school, but not necessarily a four-year degree. Yet, only 43% of U.S. workers are trained at this level.

Recognizing this challenge, IPC has for years been a leading provider of many education and training opportunities[2] that benefit the electronics sector. Earlier this year, we introduced IPC EDGE, a new online learning management system to provide education to the electronics industry workforce.

But our industry cannot overcome the skills gap all by ourselves. That's why we are constantly advocating for better public policies to address the skills gap. Most recently, we endorsed the Apprenticeship and Jobs Training Act (S. 1352)[3], a bipartisan bill introduced by Senators Susan Collins (R-Maine) and Maria Cantwell (D-Washington).

Apprenticeship programs are a proven model of workforce development, allowing workers to earn an income while they learn and companies to increase the skills of their workforce. According to the Urban Institute, more than 80% of U.S. companies that already have registered apprenticeships say it is an effective strategy for helping them meet their demand for skilled labor, and 94% would recommend it as a strategy to other employers[4].

The Collins-Cantwell proposal would establish the first-ever federal incentives for companies to establish such programs. Specifically, the bill would create a $5,000 tax credit for up to three years for

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companies that hire and pay employees enrolled in a federal- or state-registered apprentice program, as well as allow senior employees near retirement to draw from pensions early if they are involved in mentoring or training new employees.

In addition, the act will help veterans get into skilled jobs that match their military experience by allowing them to count previous military training toward apprenticeship program requirements.

To encourage more inter-generational transfer of skills, the bill would allow individuals near retirement to make early withdrawals from their pensions if they are involved in mentoring or training new employees. To qualify, older workers must be at least 55 and must spend at least 20% of their time training or educating employees or students.

In late July, I had the opportunity to meet with Senator Cantwell's senior staff in Washington, D.C. to express IPC's support for this bill. And in the months to come, we will be working to encourage additional senators to cosponsor the act.

Meanwhile, in June, IPC applauded when President Trump signed an executive order directing federal officials to take several actions to promote apprenticeships and remove regulations that could be an obstacle to them.

Specifically, the executive order:

- Directs the Department of Labor (DOL) to allow companies, trade associations, and unions to develop their own "industry-recognized apprenticeship" guidelines, which the DOL will review for quality and then approve
- Directs the DOL to use available funding to promote apprenticeships, especially in sectors where apprenticeships are not currently widespread
- Creates a federal task force that will recommend ways to promote apprenticeships
- Requires all federal agencies to review and evaluate the effectiveness of their job training programs, and consider how to best consolidate certain programs for increased accountability

IPC also focused on workforce skills in a series of meetings this summer with industry allies and federal officials including Deputy Assistant Secretary for Education for Career, Technical, and Adult Education Kim Ford.

In Europe, IPC is working in support of the European Union's "New Skills Agenda," which is encouraging cooperation between employers, universities, and local authorities in bridging the skills gap in several specific sectors, including advanced manufacturing.

Naturally, it remains to be seen whether these initiatives will bring about meaningful results. But the expanding efforts we're seeing in the United States and Europe are an encouraging sign of progress to come.

To our American IPC members and friends, please help us help you by contacting your local members of Congress and expressing your support of the Collins-Cantwell legislation and the Trump administration's apprenticeship initiatives.

Also, please let us know about your experiences and insights with worker training and education efforts. We're eager to share knowledge and shine a spotlight on our members' good works. **PCB**

**References**

1. Findings on the Skills Gap in U.S. Electronics Manufacturing, IPC bookstore (must be purchased).
2. IPC, Education, Training & Certification
3. Apprenticeship and Jobs Training Act (S. 1352)
4. The Benefits and Challenges of Registered Apprenticeship: The Sponsors' Perspective, Urban Institute.

**John Mitchell** is president and CEO of IPC—Association Connecting Electronics Industries. To read past columns or to contact Mitchell, click here.

# Why choose Fein-Line?

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# Recent Highlights from PCB007

## 1 One World, One Industry: The Future of Electronics in the Automotive Industry

Automotive electronics is not a new topic. While there is a trend for both performance and luxury electronics, many of the recent conversations tend to focus on self-driving/autonomous vehicles. While the technology is exciting, it is just the tip of the iceberg.

## 2 Punching Out! Making the Process Easy (M&A Process Engineering)

In the M&A world, there are companies that make it easy (or at least easier) and those that make it difficult. By making the process easier, sellers should see better valuations and terms, and have a smoother deal process.

## 3 Flex Talk: Knowledge is Power

"What can I do to help drive cost from my design?" This is a question that I am asked routinely. That question is often followed by, "Can I get these faster?" Both questions are even more predominant when talking about flexible circuits or rigid-flex.

## 4 'Global Wisdom. Local Presence' the Theme of HKPCA & IPC Show 2017

The 2017 International Printed Circuit & APEX South China Fair (2017 HKPCA & IPC Show) will again be staged at the Shenzhen Convention & Exhibition Center, China. This year's edition will run from December 6–8, 2017. With the theme of "Global Wisdom. Local Presence," it is hoped that global collective intelligence can be drawn to the show for assisting industry insiders to apply those high-end technologies into local production and enhance their business development.

## 5 Weiner's World—August 2017

IPC is planning to hold a special meeting on automotive electronics for senior executives during IPC APEX EXPO 2019. The meeting will be planned and produced by the IPC Ambassador Council. Its presentations will feature senior members of the entire automotive electronics supply chain.

## 6 It's Only Common Sense: Train the Youngsters and Reveal the Possibilities

There is no doubt there is a shortage of young people in our business. As we all get older, the challenge of finding young people to replace us is getting more severe. Last week in this column, we talked about finding young people in our own organizations and then nurturing them to become an integral part of our companies.

## 7 Hamed El-Abd: A New Beginning, Part 1

While in China recently, Barry Matties joined longtime I-Connect007 friend and contributor Hamed El-Abd of WKK to congratulate him on his upcoming retirement. They reflected on his time spent in the industry, specifically in China, how far it's come, and where it might be headed next.

## 8 EPTE Newsletter: Semi-Annual Review of the Global Circuit Industry

Every piece of electronic equipment uses printed circuit boards. The circuit board industry posted mixed results for the first half of the year. Listed below is a quick snapshot of the global results as well as business trends for consumer electronics.

## 9 Scottish FPCB Manufacturer Flexible Technology Awarded EN9100

Rothesay-based PCB manufacturer, Flexible Technology, has just been awarded the coveted aerospace and defence approval, EN 9100, better known as AS9100.

## 10 All Flex Launches Analytical Service for Flexible Circuitry

All Flex assists users of flex circuits in understanding how to best apply and utilize flex. Analytical Service will help OEMs identify sources of failures and reliability risk of poorly designed flex.

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# Work where you live!

The I-Connect007 China team is seeking an experienced salesperson to generate and manage a revenue stream for our Chinese publications.

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- Sell advertising contracts for monthly magazine
- Develop and cultivate new business
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- Generate and follow up on all leads
- Manage contract renewals
- Account management: work with local and international team to provide customer support
- Phone and email communications with prospects
- Occasional travel

**Qualifications**

Successful candidates should possess a university degree or equivalent, experience with managing and cultivating leads, projecting, tracking and reporting revenue. We are looking for positive, high-energy candidates who work well in a self-managed, team-based, virtual environment.

**Compensation**

This is a base salary-plus-commission position. Compensation commensurate with experience.

**Requirements**

- Must be located in China Mainland, South China area preferred
- Good command of Chinese language, proficient with English speaking and writing
- Able to follow established systems and learn quickly
- Able to maintain professional external and internal relationships reflecting the company's core values
- 2-5 years' sales experience
- Experience with Microsoft Office products
- Must be highly motivated and target-driven with a proven track record for meeting quotas
- Good prioritizing, time management and organizational skills
- Create and deliver proposals tailored to each prospect's needs
- Experience in the electronics industry desirable

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## Leading PCB Manufacturer Seeks Account Manager

Meiko Electronics, a global leader in PCB interconnect solutions for Tier I and II electronics companies, has expanded its global manufacturing footprint to include two campuses in China and two in Vietnam.

We are looking for a full-time account manager to introduce the company and our outstanding capabilities to new customers, primarily in the automotive space.

**Key Responsibilities:**

- Work directly with PCB sourcing teams to generate interest in our company
- Manage all customer relations, including scheduling onsite customer meetings with sourcing team decision makers, factory audit and qualification visits resulting in AVL status attainment
- Manage quality/engineering/logistics issues pertaining to key accounts

**Qualifications:**

- 3 years' professional experience in PCB sales or similar electrical component experience
- Excellent communication and relationship building skills
- Organizational skills, with a strong attention to detail
- Knowledge of Japanese or Mandarin languages a plus

**Location:**

The ideal candidate will have some initial prospective customers located nearby in the Midwest region and the ability to travel as needed to our Asia-based manufacturing locations.

Competitive compensation and benefits package, including competitive base salary, generous bonus/commission plan, medical/dental/vision and life insurance, matching 401k, PTO.

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## CAM Operator

American Standard Circuits is seeking a candidate to join its team in the position of CAM operator. Applicants will need experience in using Valor/Genesis (GenFlex) CAD/CAM software with printed circuit board process knowledge to edit electronic data in support of customer and production needs. Other requirements include:

- 5+ years of experience in PCB manufacturing
- Process DRC/DFMs and distinguish valid design and manufacturing concerns
- Modify customer supplied data files and interface with customers and engineers
- Release manufacturing tooling to the production floor
- Prepare NC tooling for machine drilling, routing, imaging, soldermask, silkscreen
- Netlist test, optical inspection
- Work with production on needed changes
- Suggest continual improvements for engineering and processing
- Read, write and communicate in English
- Understand prints' specifications
- Must be U.S. citizen or permanent resident (ITAR)
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**Skills and abilities required:**

- Technical background in PCB manufacturing/ design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
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Established in 1998, Zentech holds an ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including ISO:9001, AS9100, DD2345, ISO 13485, J-STD 001 with space certification, and is ITAR registered. Zentech was also the first in the U.S. to re-certify for IPC 610 trusted source QML status.

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The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

**Key Responsibilities:**

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- Log, troubleshoot, and provide overall escalation management and technical solutions
- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

**Requirements:**

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
- Experience with PLM/PDM/MRP/ERP software (Program Lifecycle Management) preferred
- Salesforce experience a plus

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Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a high-quality field service technician. This position will require extensive travel, including overseas.

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- Installing and testing Chemcut equipment at the customer's location
- Training customers for proper operation and maintenance
- Providing technical support for problems by diagnosing and repairing mechanical and electrical malfunctions
- Filling out and submitting service call paperwork completely, accurately and in a timely fashion
- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

**Requirements:**

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
- Strong mechanical aptitude and electrical knowledge, along with the ability to troubleshoot PLC control
- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

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## Technical Content Specialist

Indium Corporation is seeking a technical content specialist to guide the development of data-rich, high-level content for the company's semiconductor and advanced assembly materials (SAAM) sales and technical literature. The technical content specialist will work with multiple departments to ensure that all externally-facing technical and sales collateral and internal training materials are consistent in format and of superior quality.

**The technical content specialist will:**

- Assist in the development of key content and ensure consistency of message and format across platforms
- Develop a technically-detailed understanding of Indium Corporation materials and offerings to the SAAM industry
- Curate a library of technical conference papers and associated materials, including content related to Indium Corporation materials and their performance
- Assist in the development of, and ensure consistency for SAAM promotional materials, such as product datasheets (PDS), images, brochures, whitepapers and presentations (technical and sales)
- Attend at least one technical conference and its paper session per year

**Requirements:**

- Technical undergraduate degree (BS in Chemistry/Physics/Metallurgy/Materials Science or Engineering discipline)
- 5 years of work experience in semiconductor assembly or advanced electronics assembly
- Excellent written and spoken English language skills; fluency in Chinese desirable
- Proven ability to work independently with verbal or written instructions

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## PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

**Responsibilities will include:**

- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

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TECHNICA, U.S.A.
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## Southern California Territory Sales Engineer

Technica, USA, a Western regional manufacturer's representative/distributor, has an open sales position for our Southern California territory. The position will be responsible for selling and servicing our entire product line within the specified territory to the PCB manufacturing industry.

This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

**Required Skills:**

- BA/BS degree-desired, in a technical area is preferred
- Two years of outside/inside sales or manufacturing experience in the PCB manufacturing environment is desired
- Self-motivated self-starter with the ability to initiate and drive business with little supervision
- Independent worker with a strong commitment to customer satisfaction
- Understanding of consumable sales process
- Ability to organize activities and handle multiple projects simultaneously with effective and timely follow-up
- Ability to solve problems and make decisions for which there are no precedents or guidelines and be resourceful in nature
- Positive attitude while operating under pressure and be an independent problem-solver
- Computer skills in Windows, Outlook, Excel, Word and PowerPoint
- Must have a valid driver's license with good driving record

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TECHNICA, U.S.A.
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## Western Regional Equipment Service Technician

Technica, USA, a Western regional manufacturer's representative/distributor has an opening for an equipment service technician covering the Western USA, including but not limited to, California, Oregon, Washington, Utah, Colorado, and Arizona. The position will be responsible for servicing our PCB fabrication equipment product line, including installation, troubleshooting, repair service, rebuild service, etc. This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Key responsibilities are to install and service equipment, conduct equipment audit, and provide technical service when appropriate to solve problems.

**Required Skills:**

- 2+ years of experience in a PCB manufacturing environment or similar
- Willingness to travel
- Positive "whatever it takes" attitude while operating under pressure
- Self-motivated self-starter with the ability to initiate action plans
- Ability to work independently with a strong commitment to customer satisfaction
- Excellent communication and interpersonal skills
- Strong ability to use all resources available to find solutions
- Computer skills with ability to write detailed service and equipment reports in Word
- Understanding of electrical schematics
- Able to work in and around equipment, chemical, and environmental conditions within a PCB manufacturing facility

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Premier Training & Certification

## IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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Prototron Circuits

## Experienced PCB Sales Professional

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. Prototron of Redmond, Washington, and Tucson, Arizona are looking for an experienced sales professional to handle their upper Midwest Region. This is a direct position replacing the current salesperson who is retiring after spending ten years with the company establishing this territory.

The right person will be responsible for all sales efforts in this territory including prospecting, lead generation, acquiring new customers, retention, and growth of current customers.

This is an excellent opportunity for the right candidate. Very competitive compensation and benefits package available.

For more information, please contact Russ Adams at 425-823-7000, or email your resume.

apply now

## Process Engineer (Redmond, Washington)

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. We are looking for an experienced PCB process engineer to join the team in our Redmond, Washington facility. Our current customer base is made up of forward-thinking companies that are making products that will change the world, and we need the right person to help us make a difference and bring these products to life. If you are passionate about technology and the future and believe you have the skills to fulfill this position, please contact Kirk Williams at 425-823-7000 or email your resume.

apply now

ARLON

Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing** and **management positions.** All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

more details

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®
311 Turquoise Street Milpitas, CA 95035 (Phone) 408-945-8787

## SALES ACCOUNT MANAGER

This is a direct sales position responsible for creating and growing a base of customers. The account manager is in charge of finding and qualifying customers while promoting Lenthor's capabilities to the customer through telephone calls, customer visits and use of electronic communications. Experience with military and medical PWB/PWA a definite plus. Each account manager is responsible for meeting a dollar level of sales per month and is compensated with salary and a sales commission plan.

**Duties include:**

- Marketing research to identify target customers
- Initial customer contact (cold calling)
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Quantity and delivery requirements
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Bonding
- Submitting quotes and sales orders
- Providing ongoing service to the customer
- Problem solving
- Developing customer information profiles
- Developing long-term customer strategies to increase business
- Participate in quality/production meetings
- Assist in customer quality surveys
- Knowledgeably respond to non-routine or critical conditions and situations

Competitive salaries based on experience, comprehensive health benefits package and 401(k) Plan.

apply now

# Events

**For IPC Calendar of Events, click here.**

**For the SMTA Calendar of Events, click here.**

**For the iNEMI Calendar of Events, click here.**

**For the complete PCB007 Calendar of Events, click here.**

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**IMPACT Europe**
October 9–10, 2017
Brussels, Belgium

**electronicAsia**
October 13–16, 2017
Hong Kong

**IPC Flexible Circuits: HDI Forum**
October 17–19, 2017
Minneapolis, Minnesota, USA

**TPCA Show 2017**
October 25–27, 2017
Taipei, Taiwan

**productronica 2017**
(IPC Committee meetings held in conjunction with productronica)
November 14–17, 2017
Munich, Germany

**HKPCA/IPC International Printed Circuit & South China Fair**
December 6–8, 2017
Shenzhen, China

**47th NEPCON JAPAN**
January 17–19, 2018
Tokyo Big Sight, Japan

**DesignCon 2017**
January 30–February 1, 2018
Santa Clara, California, USA

**EIPC 2018 Winter Conference**
February 1–2, 2018
Lyon, France

**IPC APEX EXPO 2018 Conference and Exhibition**
February 27–March 1, 2018
San Diego, California, USA

**China International PCB and Assembly Show (CPCA)**
March 20–22, 2018
Shanghai, China

**KPCA Show 2018**
April 24–26, 2018
Kintex, South Korea

**Medical Electronics Symposium 2018**
May 16–18, 2018
Dallas, Texas, USA

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DECEMBER:
**Thermal Management**
Keeping off the hot seat.

JANUARY:
**Equipment**
Choosing the right equipment for your current and future needs.

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