AUGUST 2024

I-Connect007

DESIGN007 MAGAZINE

Cost Drivers

Kris Moyer
Instructor, IPC

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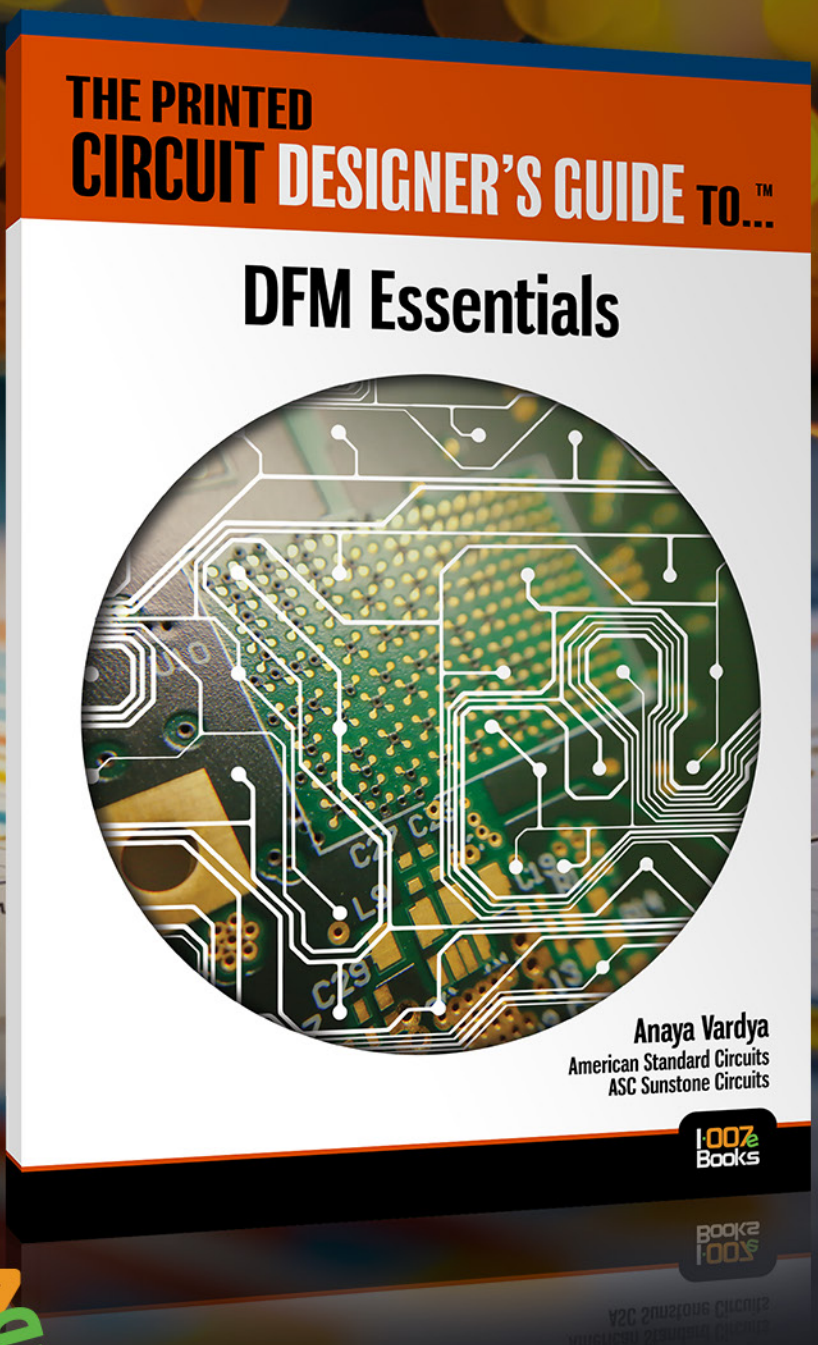

I-007e Books

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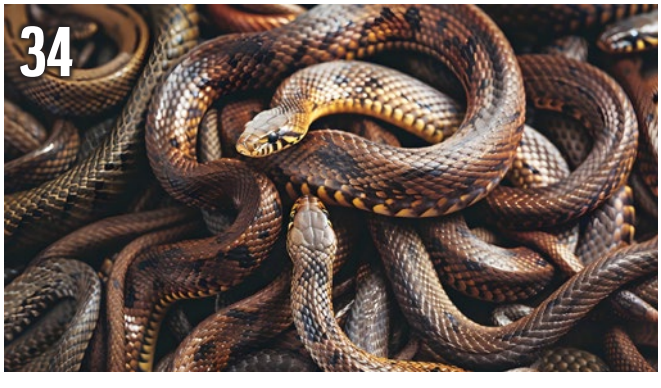
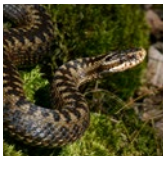
DESIGN007 MAGAZINE

PCB Design Cost Drivers

What's driving your costs? In this month's issue, our expert contributors explain the impact of cost drivers on PCB designs and the need to think in terms of a design budget. They discuss a myriad of design cycle cost adders—hidden and not so hidden—and ways to add value as well. When every decision has ramifications downstream, the more you know, the better.





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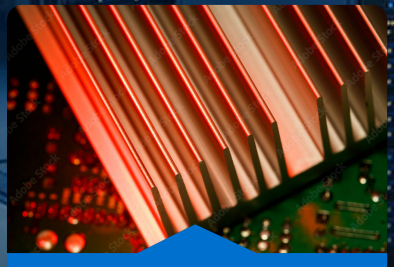

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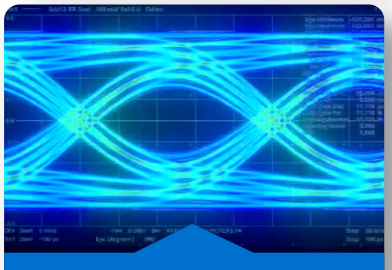

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Watch Out for Cost Adders

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

I've owned a few snakes in my lifetime. In my high school biology class, for example, I took care of our black rat snake for a few weeks. He escaped once, which they all eventually do, and climbed up inside our furnace. My next snake was a nine-foot yellow-tailed python. He suffered an ignominious end when he was killed by the giant rat who was supposed to be his dinner. In my 20s, I had a hognose snake that also escaped, and I never did find him.

Snakes can be tricky, as you can see. This month we focus on one serpent that bedevils PCB designers and design engineers: the cost adder.

Because approximately 70% of the manufacturing costs of a product are determined in the design cycle, every decision a designer makes has some effect—good or bad—on the manufacturing cost, as well as the cost of the final product.

Fortunately, cost adders can be kept at bay: Designers can employ hundreds of tips, tricks, and techniques to keep costs down.

In this month's issue, our expert contributors explain the impact of cost drivers on PCB designs and the need to consider a design budget. They discuss the myriad design cycle cost adders—hidden and not so hidden—and ways to add value. When every decision has ramifications downstream, the more you know, the better.

We start with Jen Kolar's article on common design errors, especially DFM miscues, that can have a bigger impact on cost than you might think. Cherie Litson details areas where she often discovers cost adders hiding, and which teams seem to be constant targets of these troublemakers. Columnist Martyn Gaudion offers "common-sense" tips for adding value to the design cycle. Kelly Dack provides "anti-venom" for PCB design cost adders, and he points out some of the dens where cost adders often lurk, waiting to drive up your manufacturing costs. Michael Marshall has a paper on design cost drivers, which covers dozens of ways designers can add cost into the design cycle, often without realizing it. Rounding out our features is a column by Istvan Novak on the evolution of PCB design costs.

We also have columns by Matt Stevenson and Joe Fjelstad, and articles by Dan Beeker, Erik Pedersen and Richard Koensgen, and Anaya Vardya, as well as an excerpt from Anaya's brand-new book, *The Printed Circuit Designer's Guide to DFM Essentials.*

I hope you're having a relaxing summer. You've earned a vacation. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 23 years. To read past columns, click here.

GLOBAL CITIZENSHIP

The Nexus of Chinese and American Business Relations

by Tom Yang, CEE PCB

Many people I talk to feel there are very few similarities between how Americans and Chinese do business. However, I believe that's not true. That's why I researched the similarities between our cultures for this second column on global citizenship.

Americans Built the Chinese PCB Industry

Remember, it was American companies that taught China how to manufacture circuit boards. Our factories have your fingerprints all over them. So, it should come as no surprise that Chinese and American business practices—while shaped by distinct cultural, historical, and socio-economic factors—nevertheless share several similarities. We still mostly use Western-made equipment and follow IPC standards developed in North America and Europe.

As we have grown more independent in recent years, for example, in manufacturing our equipment and laminates, our commonalities are becoming more relevant as globalization and technological advancements intertwine the economies of both nations. Understanding these similarities can foster better communication, collaboration, and mutual respect between Chinese and American business professionals.

To continue reading this column click here.

Hidden (and Obvious) Design Mishaps With Big Cost Impacts

Feature Article by Jen Kolar
MONSOON SOLUTIONS

At Monsoon Solutions, we provide PCB layout services for the full lifecycle of products, from one-off prototypes to items manufactured in production volume. We also manage manufacturing and assembly for prototype and smaller production runs for both customer-produced and in-house layouts. As a result, we see various manufacturing data packages and work with many different manufacturers. I asked our PCB design engineers and program managers to share the cost adders and cost savers that designers can affect, and it was interesting to see that in addition to more technical responses, some of the biggest culprits were rather simple.

Fabrication Note Errors

Starting with PCB fabrication, one of the most obvious and simplest cost adders is incorrect or missing fabrication notes. As designers, we all like to have a starting point for a layout rather than having to start from scratch, and that often means starting from a similar board, which comes with existing fabrication notes. As a service bureau, we also often work on revisions of designs, and thus we inherit fabrication notes from the previous design. A common mistake I see from designers is when they leave notes the new designer doesn't understand or know if they are required. I will often see them ask the customer about the notes,

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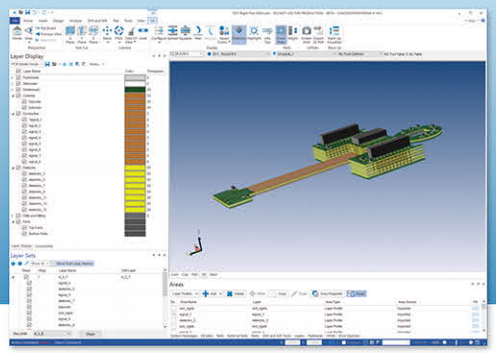

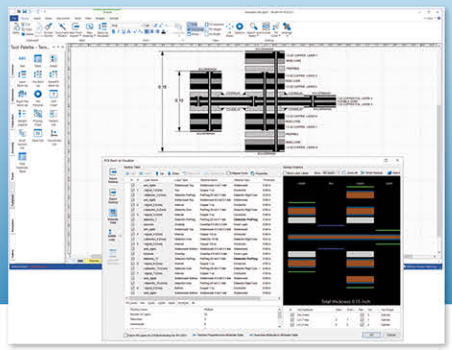

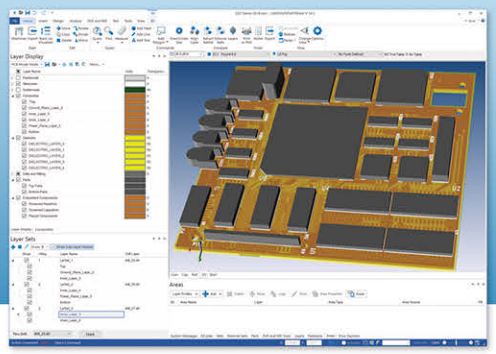

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and it's not uncommon for the customer to not know if they apply either. Rather than removing them, they commonly remain "just to be safe." This often leads to extra processes like via fill, planarize, and plate. It may lead to building to Class 3 vs. Class 2 or extra testing and paperwork requirements. It may lead to adding hard gold vs. just ENIG. It may lead to ordering more exotic materials where standard FR-4 was fine. It also can lead to back-and-forth DFM questions as the fabricator must confirm what does or doesn't apply, and with which offshore vendors can mean delays of multiple days.

Similarly, if there are no fabrication notes, the fabrication vendor is left guessing and may choose processes or materials that are more expensive or not absolutely needed, or they may miss important aspects of the design, like controlled impedances or that a specific thickness is needed for edge connectors. Make sure to review your notes for clarity and correctness before sending them to the fabrication shop. If you are unsure how to specify your requirements, talk to your fabricator.

Another fabrication note mishap is not calling out whether the boards should be v-scored or have mouse bites for breakaway tabs. It is common for offshore high-volume designs to use tabs without scoring or mouse bites and for assemblers to have the tools necessary to depanelize them. This is rarely the case in lower-volume or prototype shops. I have seen countless cases of a customer providing data from a previous high-volume production build that included solid tabs that smaller prototype assembly shops were not able to easily depanelize. If the assembly house is unable to depanelize the board correctly, this could lead to damaged boards, damaged components, and a possible respin of the boards. Verify with your assembly house on how they will want to depanelize the boards and add that to your fabrication notes for your fabrication shop.

"If you are unsure how to specify your requirements, talk to your fabricator."

Copper thieving callouts are a less common fabrication note mistake, but still one that can cost an entire build to be scrapped. It is common for RF boards to have intentional voids that you don't want any copper added to, like thieving. Make sure your fabrication notes clearly specify if thieving can be added, and where on the board it should be avoided. I've seen frustrated customers find out after days of debugging assembled boards that they aren't working as expected due to thieving being added to areas where it shouldn't be. There is no salvaging this mistake; it's a respin.

Now let's address vias-in-pad in thermal ground pads under ICs. In most cases, assemblers will windowpane the stencil to distribute the paste and it's not at all an issue to have non-filled vias in larger center ground pads. If your design doesn't otherwise need via-in-pads filled, then don't call it out for your IC thermal ground pads. Make sure your fabricator knows they don't need to be filled or they might assume they do.

Finally, make sure your fabrication notes clearly call out where parts overhang so that they don't panelize it in a way that they can't be assembled in panel. Forcing assemblers to work "one-up" vs. in array adds cost and time. This is an area often missing from fabrication notes and one that would save a lot of frustration for the assembler if it were added.

Design Mishaps

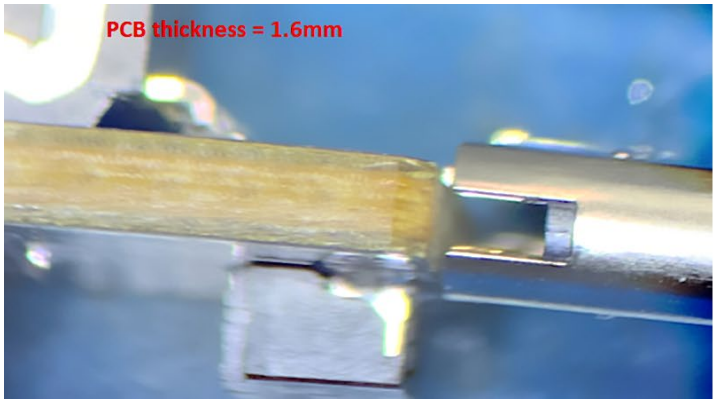
As designers, it's our job to make sure the PCB functions correctly and meets the required specifications. We spend most of our time in design making sure the board meets our internal or customer specifications, but the fabrication and assembly specifications are just as important when trying to avoid increases in cost.

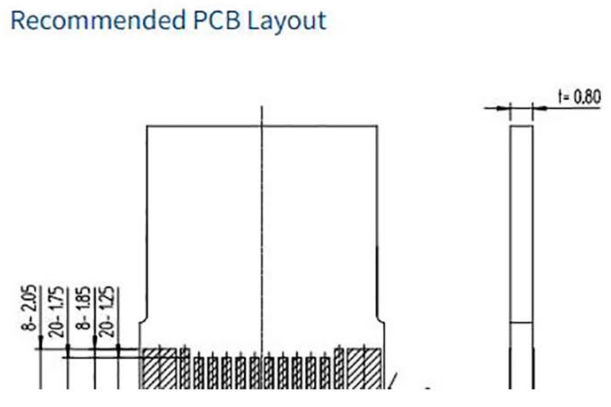
Poor footprint design can often lead to added costs in manual rework, additional stencil orders, and poor yield. One of the most common footprint errors is missing solder mask openings. Missing openings are typically discovered after a stencil has already been ordered, and results in the assembler needing to scrape solder mask off pads and reorder stencils to salvage the build. This kind of rework is not always possible, and if the assembler can't make it work, another set of corrected PCBs will need to be ordered.

A favorite error of mine, and of many assembly shops, is when two designs are panelized together, and they share designators. There are many beneficial use cases to panelize boards together, such as multiple boards that will always be used in a set and share a stackup, but make sure to either do the designs in the same schematic and database or verify that you don't share designators between the designs. A simple way to do this is to use a matching prefix number on your designators for each design. Design A uses C1XX, R1XX, and U1XX, while Design B uses C2XX, R2XX, and U2XX. Also be aware that if too many different boards are together in one array, you can end up with a mismatch of component density across the panel, which can cause warpage during assembly. Combining designs on one panel is often a cost savings attempt that can create more headaches and time cost down the road.

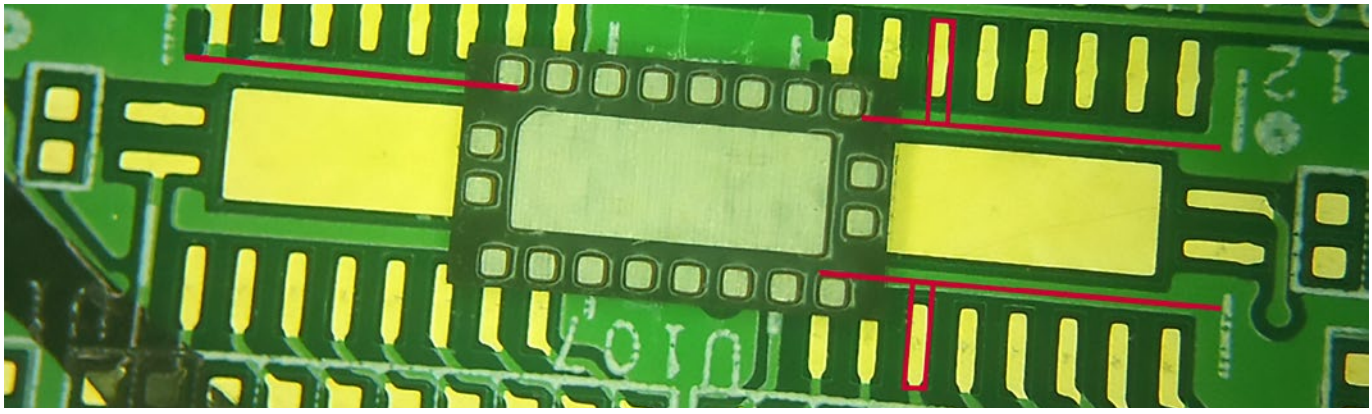
A general area that I can't stress enough in design is the KISS factor: Keep It Simple, Stupid. If you don't need trace width and spacing under 6/6 mils, don't use it. If you don't need microvias, don't use them. If you don't need blind or buried vias, don't use them. If you don't need via-in-pad, don't use it. If you don't need a really tight via/pad aspect ratio, don't use it. If you don't need your components as absolutely as close together as possible, don't do it. Even if you design to Class 3, but your prototype build only needs to be to Class 2, make sure to let the fabricator know. Your fabricator may specify that they can build boards at a 3-mil trace and space, but this doesn't mean they can do it at 100% yield, and the added cost of those failed boards gets passed on to you and your customer.

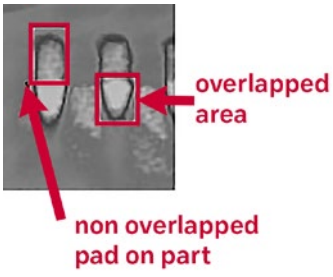
Newer designers tend to use more complicated via structures, smaller features, and tighter spacing to make routing a design easier. Not only does this drive up cost in manufacturing, but it also adds time, and risks yield and





In this mishap case we have a size profile of a board that was intended to insert into another connector. The customer didn't specify a stackup or an overall thickness, so a standard one was chosen by the fab vendor that was too thick. We had to scrap and rebuild.





The footprint was incorrect for this part. You can see the part upside down in the middle and in two locations it was to be placed right underneath the part body. Since this was a pick and place part, the issue wasn't found until X-ray inspection after assembly reflow, so the parts had to be manually removed from each board and the boards cleaned up. As this was a multi-lam build and expensive, we wanted to salvage the boards. This mistake ate up time for everyone. It was a prototype run that was fixed on a later rerun. (Right) What we chose to live with after replacement part.

reliability. It takes more time, skill, and experience to keep a tighter design using through-hole vias, and it's not always possible depending on the pitch of parts, or other electrical requirements, but when it is, that can be worth it in saved manufacturing cost.

This brings up another cost adder that designers and customers may not think about, which is the tradeoff of one-time/upfront costs in design vs. repeated costs in manufacturing. There is often a push to get a design to fabrication as quickly as possible. However, if the designer just had a bit more time, maybe the design could've been done without microvias or via-in-pad, or maybe they could've done it in fewer layers. Designers should try to push back on unrealistic customer schedules and expectations and help explain the benefits of taking the time to do it "right." Remembering that PCB design is fairly late in the product design lifecycle, designers are usually pressured to make up time and are given unrealistic schedules. This leads to mistakes or shortcuts that can result in scrapped boards, which means respins, and that means a lot of lost money and time.

Take time to learn about how the fabrication process works. It is a common mistake for newer designers to create via structures that are impossible to fabricate or stackups that are overly complex and add unnecessary lamination cycles. Sometimes customers drive these complex stackups; designers should push back and help the customer understand the fabrication process and how additional lamination cycles drive up cost. Customers can also be the ones driving use of tight aspect ratio holes or tight placement of parts. Help them understand the risks.

Similarly, take time to learn about how the assembly process works. I've already talked about several assembly issues related to panelization, but something as simple as component placement can drive up costs. Don't place very tall parts next to very short parts. Don't place through-hole parts very close to SMT parts. Space out your parts as much as you can, so rework is a possibility. Make sure to turn those courtyards on while you work on placement. Also, remember to add fiducials, both on the board and on tight pitch, larger BGA, QFN, and other leadless packages.

IPC standards exist for a reason. Know them. They aren't just suggestions. Whenever possible, follow them for both PCBs and PCBAs. If you are knowingly violating a standard, try to

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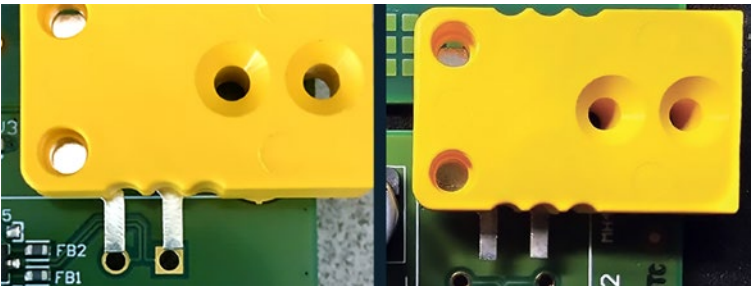
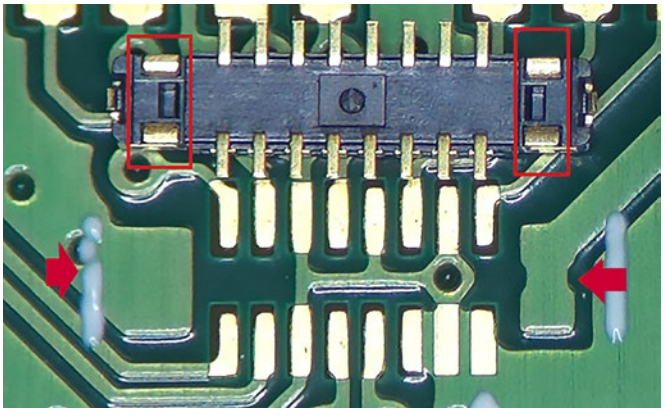


Two different versions of the same problem: The pins on this part didn't match the hole. Attempt 1 (left) we were able to Dremel the pins and fit in the holes. Attempt 2 (right) we ended up gluing the part on the board and soldering wires on the pins and board to jumper it together.



In this case, customer did the layout and didn't include pads for the 4 outer pins of the connector. We had the option of having the shop scrape off the solder mask and manually work the connector in, DNP, or scrap. For this build they chose DNP to salvage it and not spend more cost on the rework.

limit it to as little of the board as possible and make sure your vendors are aware in advance of starting the build. If you don't follow the standards, you risk an expensive or unbuildable board.

Speaking of vendors being aware, one key to saving cost and time is to ensure that complex designs have preliminary reviews early on by the fabricator and assembler. Nothing is worse than spending months on a design only to find out it is not buildable, it is incredibly expensive to build, or can only be built as a one-off with low yield. Review and validate your design rules early and perform a DFM check with representative data as early in the design as possible. It is common to have fabrication vendors approve a preliminary stackup, via structures, and spacing only to realize that once they see the density of the design or the impedance requirements that it is not possible. This requires redoing the design which adds time and cost.

If you know a design will ultimately be a smaller form factor, design your earlier versions to that so you aren't wasting hours redoing the design. Even if you can get away with some shortcuts in prototype runs, avoid them, or you will have to redo the work when you get to the production version. Do it right the first time. This can be a very hidden cost that the designer isn't initially aware of. Ask your customer what their final plans are for the design so you can design to that from the beginning. If they will eventually build to Class 3, set your vias and spacing up accordingly from the beginning. Otherwise, you could be looking at a costly redo to try to add larger pads in a dense design.

This brings us to one of the most important topics and a good closing point: Communicate early and often. Make sure you know all the requirements up front, including mechanical, electrical, budgetary, schedule, and so on. Designers must make a lot of decisions as they are working. If you make them without realizing there are unknown requirements, like keep-outs, high-voltage areas, mounting holes, or testing requirements, you may have a lot of work to redo. We all know time is money. In this case it also can be a sacrifice to quality in an attempt to salvage work done that would have been done differently if the requirement had been known in the first place. Take the time to tell your customers what can be done to make the design better and save them money. They hired you to be the expert, so be one. **DESIGN007**

Jen Kolar is the vp of engineering at Monsoon Solutions, a PCB design service bureau in Bellevue, Washington.

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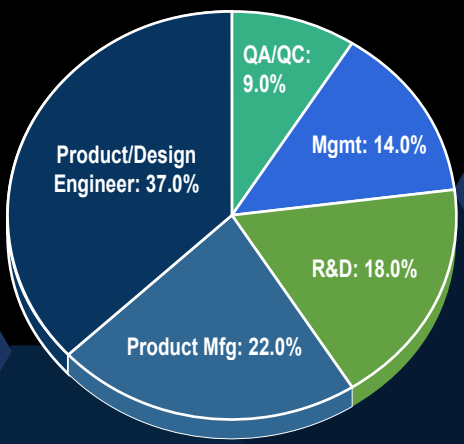

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Hidden Cost Drivers in PCB Design

Feature Article by Cherie Litson, MIT, CID/CID+
EPTAC

I recently taught a CID+ course, and if you've ever taken a CID or CID+ course, you know that we discuss cost adders quite a bit. When I asked the class of 15 design engineers their ideas on the biggest cost adders, the first and strongest response: the project manager.

Are you surprised by their answer? After over 40 years in the industry, I wasn't. If you step back and look at the process of product development, you'll see that many decisions that affect costs down the line really do take root with the project manager.

After reviewing my own experience and that of many other designers, I referenced my favorite source for defining cost adders: the IPC PCBA Checklist 17. Here you'll find most of the cost adders that we all encounter to one degree or another. As you review the checklist and see who is responsible for many of the decisions, you'll find it all starts with the project leader.

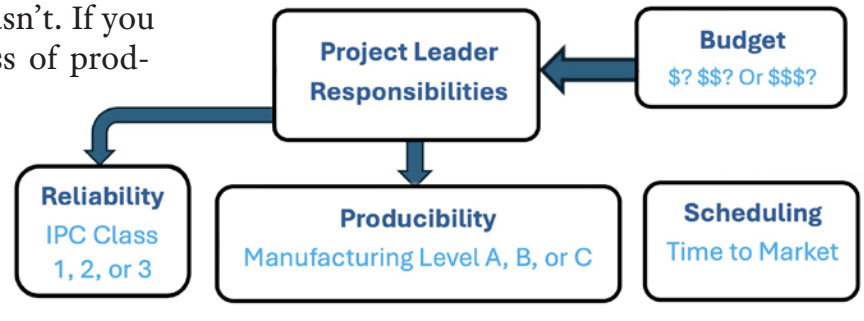
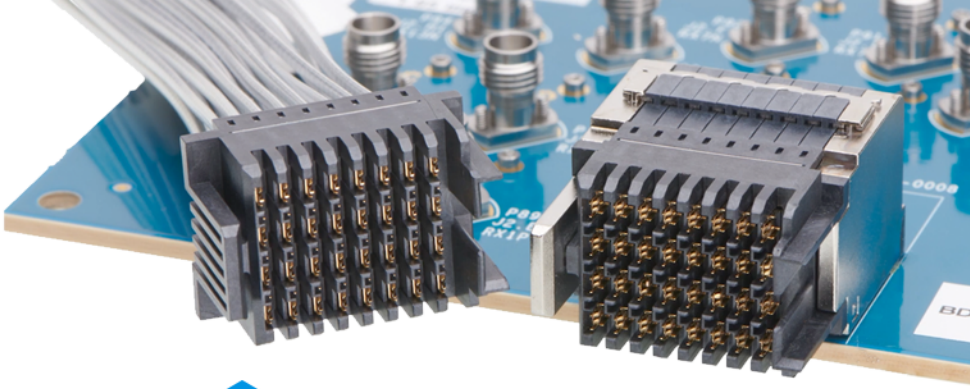
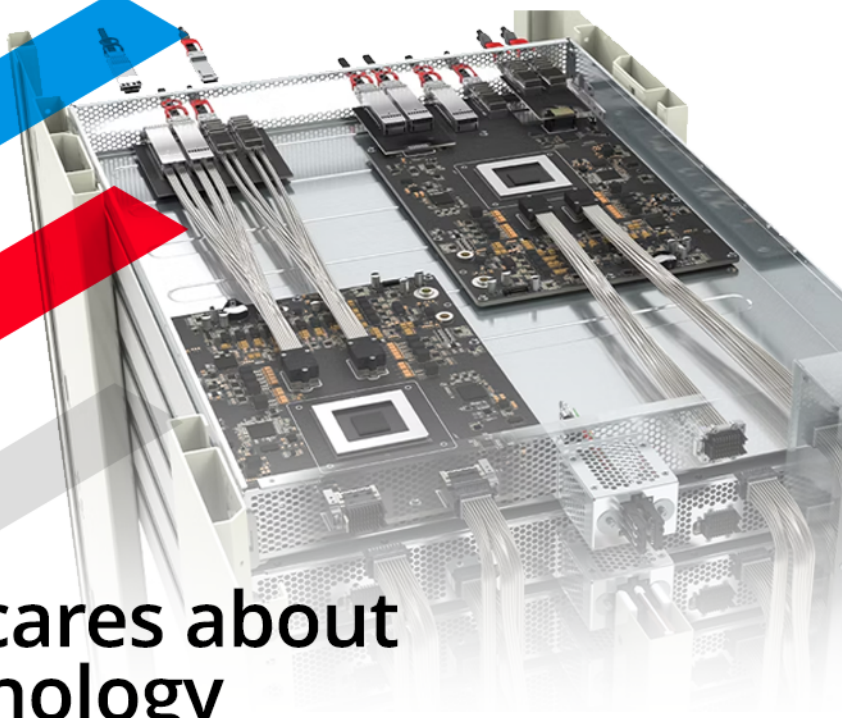


Figure 1: Many of the added—or saved—costs in the PCB design process start with the project leader.





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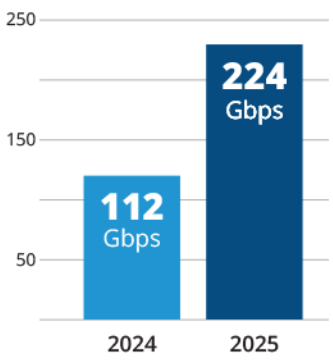

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Everything you've read about the cost-saving process is controlled by the project leader's actions; the project leader is like the chef in the kitchen.

The engineers and designers will then limit their decisions based on the requirements set by the project leader. They become the "sous chef" in the process. The engineers and designers then set the limits and specifications in their documentation affecting purchasing, fabrication, assembly, and test. They become the "station chef" or "line chef." That's why the CID and CID+ classes focus so much on the design engineer's decisions. But no one really addresses or guides the project leaders for their role in the cost saving process.

So, project leaders, this is for you. Here are some guidelines for getting those cost savings you so desire.

1. Start With the Team

The first cost saving method starts with the team. Having all the input possible at the very beginning and periodically during the project development allows all players to realize the impact of their decisions.

Team meetings can be online and/or in person. Representatives from all those working on the product development should attend. A good project leader has regular design reviews to be sure everyone has input to the project. No finger pointing. True input and problem-solving generate creativity and real cost savings. This is not an easy task. Setting limits for the product features and defining what goes into this model and future models is critical for making sure everyone works toward the same objectives.

2. Identify What Can Be Done

The second cost-saving method is to identify what can and cannot be done concurrently. Many times, this depends on the product's maturity. Look at what can be reused from previous products and designs. If one group is waiting for information from another, discover what else they can contribute to the overall completion of the project.

When designers are waiting for input, they

Checklist at the Project Start Level

E	Responsible	Demand on Assembly	IPC Standard	Information	Check
1	Project Leader	IPC Class 1, 2 or 3?	IPC-2221	Any Additional/Exceptions	
2	Project Leader	IPC Level A, B or C?	IPC-2221	Any Additional/Exceptions	
3	Project Leader	IPC Level A, B, C or D?	IPC-1752	Material Declaration	
4	Project Leader	RoHS 1 or RoHS 2?			
5	Project Leader	Touch up and Repair allowed?	IPC-7711/21	Valid for both printed board and printed board assembly?	
6	Project Leader	Surface finish on components?	J-STD-002	Different surfaces have different wetting. Can be of importance for achieving IPC Class 3.	
7	Project Leader	Process Sensitivity Level (PSL)	IPC-020 and IPC-075	Max Temp, Thermal gradient and H_2O Sensitivity.	
8	Project Leader	Surface finish on Printed Boards?	IPC-4552, IPC-4553 and IPC-4554	Different Surface Finishes have Different wetting and durability.	
9	Project Leader	MSL on components	J-STD-033	Moisture Sensitive Level of more importance for a Pb-Free process.	
10	Project Leader	Marking and Labeling of Components, printed boards and Printed board's to Identify Pb, Pb-Free and Other Attributes.	J-STD-609		
11	Project Leader	Voids?	IPC-7095	In the balls of BGA and CSP components	
12	Project Leader	UL class?		Underwriters Laboratories	
13	Project Leader	Cleaning and Conformal Coating	IPC-CH-65	See Checklist I, page 19.	
14	Electronic Designer	EMC on the printed board and components?	Needed for CE marking	Different Standards/Demands in different countries?	
15	Electronic Designer	Impedance?	IPC-2141		
16	Electronic Designer	High speed/frequency?	IPC-2251		
17	Electronic Designer	High amperes?	IPC-2152		
18	Electronic Designer	Base material properties for mechanical, electrical and thermal?	IPC-4101	All Base Material have different values for Tg, Td, Dk and CTE.	
19	Project Leader	Cooling in- & outside printed boards?	IPC-2221		
20	Electronic Designer	Cu foil quality?	IPC-4562	Different Cu Foils in the market	
21	Electronic Designer	CAF base material?	IPC-9691	Conductive Anodic Filament	
22	Electronic Designer	Embedded in the Assembly?	IPC-7092		
23	Electronic Designer	BGA/CSP on the Assembly	IPC-7095		
24	Electronic Designer	QFN on the Assembly?	IPC-7093		
25	Electronic Designer	Flip Chip on the Assembly?	IPC-7094		
26	Electronic Designer	Minimum isolation distances between holes and tracks?	IPC-2221 and IPC-2222		
27	Electronic Designer	Final size (LxWxT)?			
28	Electronic Designer	Number of layers?	IPC-4121	Buildup of an multilayer printed board	
29	Electronic Designer	Mechanical tolerances?	IPC-2615	Mechanical Drawings Standard	
30	Electronic Designer	Assembly SMDx1, SMDx2 THT or in combination?			
31	Electronic Designer	Predestinated component placements and forbidden areas?	IPC-7351		
32	Project Leader & Electronic Designer	Documentation requests material declaration	IPC-2611, IPC-2612 IPC-2612-1, IPC-2614 and IPC-2615	If not all needed data are included, the interface between CAD and CAM at the printed board and printed board assembly supplier will be unclear.	

Figure 2: A marked-up excerpt from the IPC PCBA Checklist 17.

can do the following: Research, get training, start mock designs and templates, perform library maintenance, and assist others with their tasks. This can often contribute to speeding up the design process.

While waiting for input, engineers (electrical and mechanical) can do the following: Component engineering and end-of-life verifications on components, be trained on software, research new manufacturing methods, identify critical test criteria, double-check their schematics for wording and pin connections, and work closely with purchasing to certify alternate sources.

Be cautious of purchasing "deals." Make sure it will work with the design. Many good designs have gone bad because a part wasn't available and the new one didn't meet the "form, fit, and function" criteria. Or the panel excising method was changed from "routing" to "scoring" and there wasn't enough clearance to the board features for that process and breakage happened due to mechanical stresses.

For manufacturing, timing is critical. Fabricators shouldn't get too far ahead of the finished design or be caught unaware of what their needs will be. Keep the board shop in the loop for what you plan to do. Your fabricator may need to review your layer stackup to purchase new or additional material. Assembly may need to take early action for component procurement. Many times, manufacturing can offer solutions they have used with other clients.

3. Design Once, Build Many

The third cost saving method is to remember this mantra: "Design once, build many." Take the time to design thoroughly. Doing this can often support going directly from prototype to build. I've done this with new designs. A great chef never serves an undercooked meal.

Designing a board only once also cuts production costs. There is no real need to keep building multiple prototypes with fixes in the product. Quit paying for wasted supplies and time for multiple turns. Quit paying for "fixes" in the production runs. We have incredible software products to support mechanical and electrical analysis of any product, so use them.

4. Educate Yourself

The fourth cost saving method is to educate yourself. Since the PCB design process often becomes the hub of the project, take the CID exam. (Yes, I teach it, but the CID really is a great idea.) Get to know the terminologies and processes involved in designing and manufacturing the board. You don't have to be an expert; just be familiar with all the parts of the processes and be able to plan with them. You may discover new ways to speed up the process and cut costs.

The entire team needs to be able and willing to check themselves and each other. Be willing to explore and learn new methodologies and processes. Every design is different. Every manufacturer has different capabilities. Everyone needs to be open to new suggestions. Be sure to do it in a supportive manner.

One of my dad's favorite lines when he saw someone struggling with a task was, "Would you like to learn another way to do that?" While his suggestions didn't always work, we both learned new options and gained a better understanding of how to accomplish the same thing. Maybe the way we've always done it just doesn't work as well as it did, and there are other ways to accomplish a specific task, process, or goal from a different perspective.

Finding the keys for getting the most "bang for your buck" starts by finding the cost adders for each design. **DESIGN007**

Cherie Litson, MIT CID/CID+, is the founder of Litson1 Consulting and an instructor at EPTAC and Everett Community College. She has more than 30 years of design experience, and has been an instructor since 2003.

Commonsense Cost Cutting

The Pulse

Feature Column by Martyn Gaudion, POLAR INSTRUMENTS

One difference between engineering and pure science is that engineers (in most situations) are looking for cost-effectiveness. They do so by designing the most appropriate level of technology to maximize profitability with acceptable levels of application functionality.

One area that is often overlooked is the energy cost of PCB production. At a recent EIPC conference, Dr. Maarten Cauwe of IMEC in Belgium presented a combined study of the lifecycle impact (LCI) of electronics systems and subassemblies[1]. The study looked at the supply chain as well as the energy impact of HDIs, the power consumption of repeated plating cycles, and the energy impacts of different metal finishings.

One side point was the move to lead-free soldering, which has raised energy consumption across the board. I wonder if legislators will hear this message and, at some point, cause a U-turn in the industry where the lead-free project, once deemed worthy, no longer seems like a good idea. Half a century ago, CFCs were miracle chemicals. Now, not so much. Changing times and emphasis, with effects that take decades to emerge, mean that ideas that once seemed sensible can, with the benefit of hindsight, seem not so good. The study is interesting

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

Every day we get questions like those. And we love it. We have more than 600 PCB experts on 3 continents speaking 19 languages at your service. **Regardless where you are or whenever you have a question**, contact us!

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because it attempts to put together a whole-of-life model for the electronics ecosystem rather than looking at individual items in isolation.

Detail Matters

While IMEC studies are effective from a top-down standpoint of the whole energy cost of electronics and subsystems, at the day-to-day level, it is down to individuals and teams to make a difference. Additionally, the cost of PCB design is not solely down to energy, though that plays a part at every point. The fact that the type of build alone can impact the cost should be considered, as well as the material choices.

When considering materials for high-speed boards, especially those intended for volume use, it is wise to assess whether each layer needs high-speed materials. The savings can be considerable if basic materials can be used in layers where speeds are low or moderate. Clearly, a different approach is required for low volume. However, if the volume is low because of a prototype application, it's worth exploring the same material choice used in volume to pre-empt any surprises should you prototype in an exotic material and back off the specs on less critical layers in final production quantities.

Short, Slim, and Smooth

Per my recent column on high-speed designs, you can reduce the need for exotic materials if you have the luxury of keeping the high-speed lines as short as possible. Losses are directly proportional to line length. If a compact design is viable, you can save on both the cost of materials and the consumption of square meters.

Panelise With Waste Minimisation in Mind

Designing with panel size in mind can save on material costs. The late Martin Cotton was a firm believer in optimising the total design to

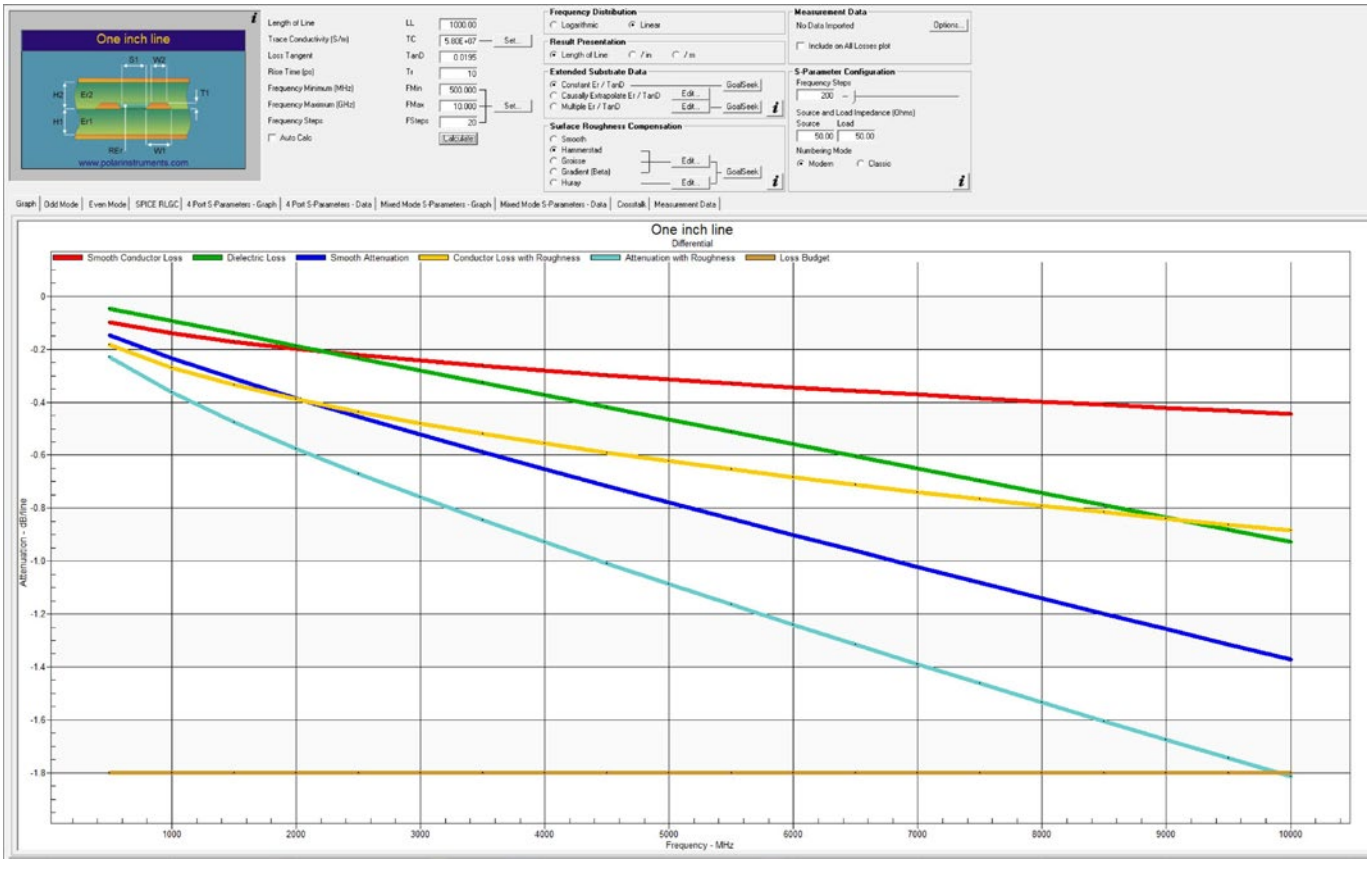

Figure 1: Half the length, half the losses.

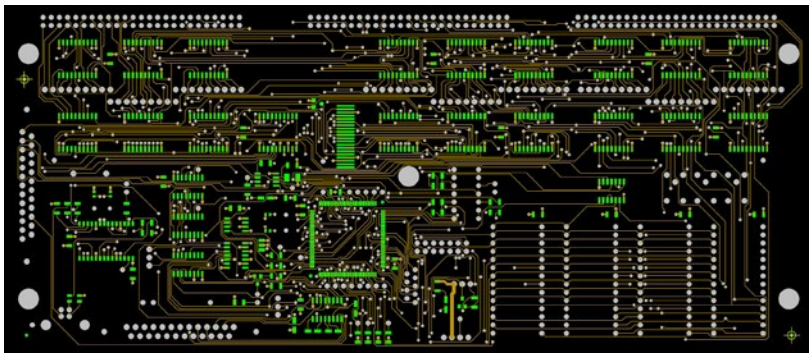

Figure 2: A single PCB.

maximise the use of standard panel size. While panelisation software helps with optimisation, the designer can make life easier for the fabricator by considering the panel size when designing the entire system. It is also worth noting that PCB fabricators have made large strides in optimising panel use and being able to fabricate closer to panel edges.

Simulate Where You Can

Simulation reduces the number of prototype turns and simulates how a design may respond to normal component variation in production. Monte Carlo simulations for electronics design allow you to see how much variation to expect over typical production runs. Monte Carlo tools add a dose of realism to the engineering process, as it's easy to be seduced by the multi-digit precision of modeling tools and circuit simulators. Tools with the ability to run simulations with expected parametric variations add confidence to the design process and give the designer more confidence in the finished yield, reducing the need to run extensive and expensive physical prototype turns.

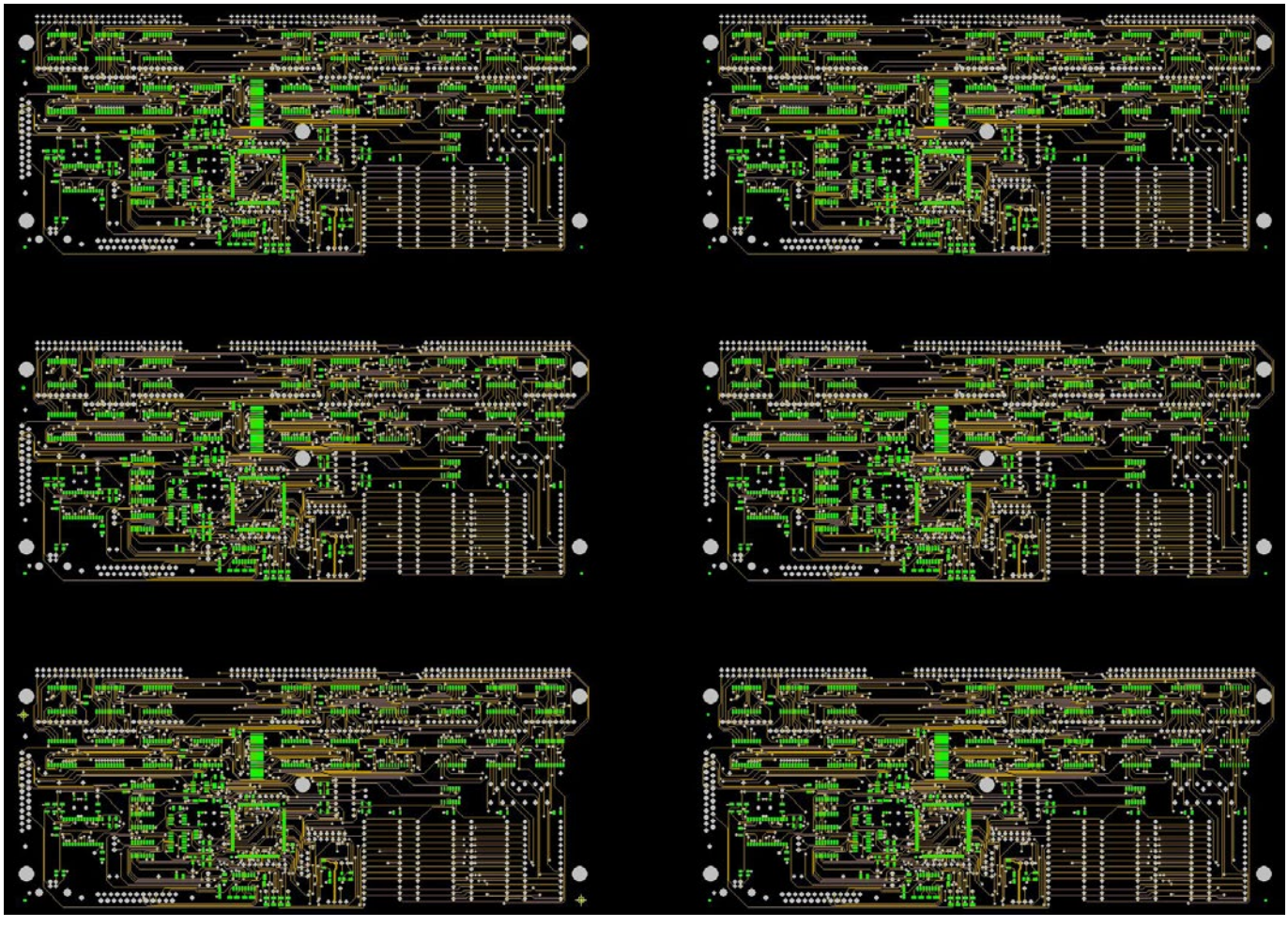

Figure 3: Six up. Panelisation easy with simple shapes, but for more complex outlines, panelisation software tools can increase the board yield per square foot of material.

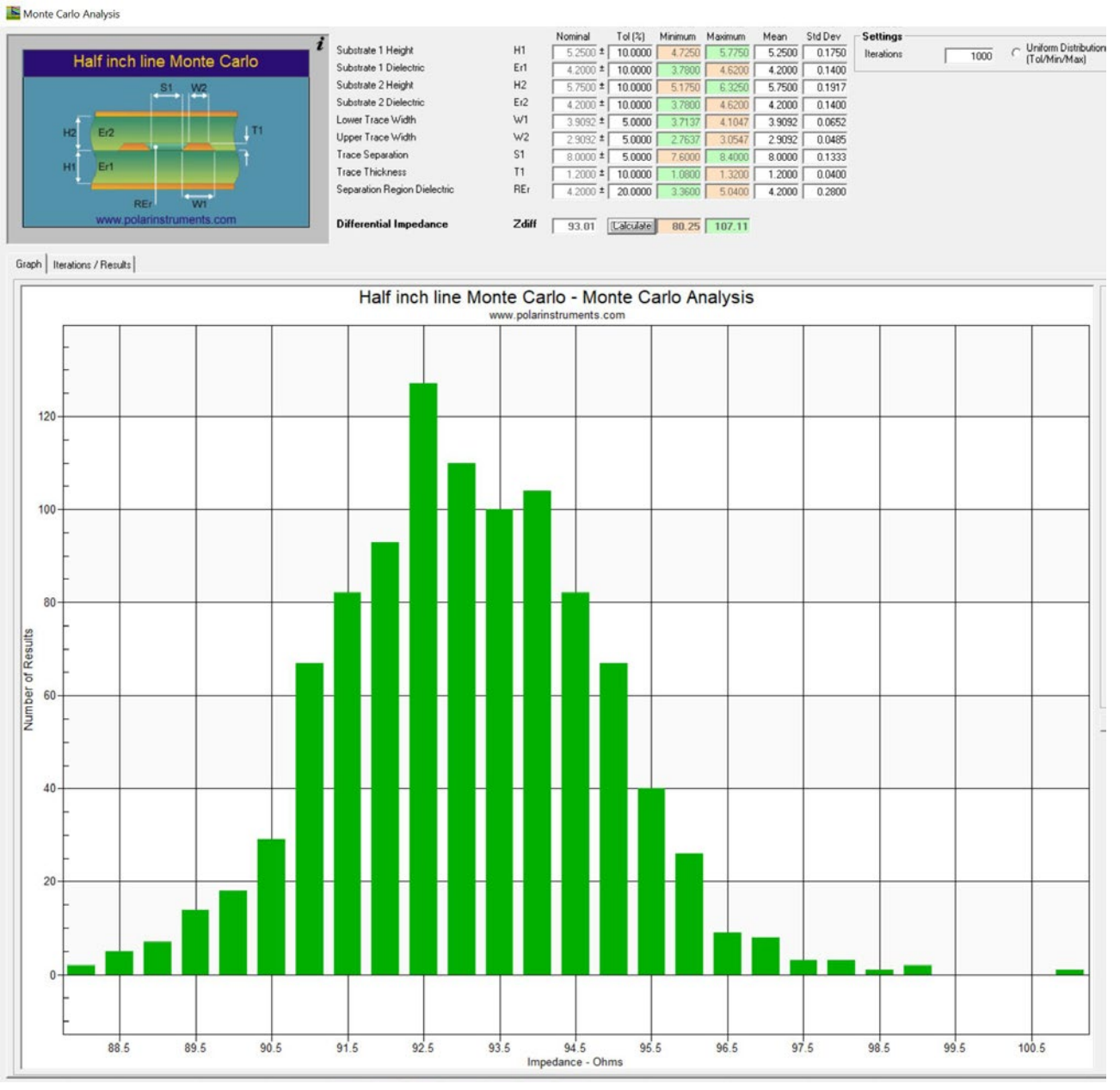

Figure 4: Running production simulation allows you to see how much window you have for production variation and helps maximise yield.

Conclusion

Always keep an open mind and look for cost savings from different angles. My opening note on energy costs is interesting for fabricators because, with energy costs being high, saving energy for the same functionality by choosing an alternate stackup is a win all around. There are many ways to save costs, so it pays to keep your eyes open for innovative solutions. **DESIGN007**

References

1. "A parametric approach to quantifying the environmental impact of PCB manufacturing," by Cauwe, Willems, and Geerinckx (IMEC/IMEC/ACB), CMST IMEC Research Group, Ghent University BE.

Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns, click here. Martyn is the author of *The Printed Circuit Designer's Guide to… Secrets of High-Speed PCBs,* Parts 1 and 2.

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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Cost-optimize Your PCB Design and Specifications

Article by Erik Pedersen and Richard Koensgen, Illustrations by Hervé Chevaleyre
ICAPE GROUP

Knowledge is the key to identifying the small details that makes the big cost difference for your printed circuit board. There are many types of printed circuit boards and multiple choices between the development of schematic and BOM to PCB technology selection, electronic PCB design, mechanical and physical properties, and PCB specification.

Component Technology and BGA Size

The component size and technology have the most significant influence on the PCB cost. Most surface-mounted microchips can be designed into standard PCBs with plated through-holes. If the same microchip comes in a BGA package, it might need microvias and buried vias using a higher wiring density to be designed into an HDI PCB. Generally, PCBs containing BGAs become HDI PCBs when the ball center-to-center pitch is below 0.8 mm. If your physical board properties allow it and the component availability is equal, you should strive to find the BGA with the largest pitch to reduce the component and PCB cost.

For example, the same BGA microchip can be found with pitch 0.8 mm, 0.6 mm, and 0.5 mm. The 0.8 mm pitch BGA can be routed on an eight-layer standard PCB with a price index of 100. The 0.6 mm pitch can be routed on a (1-6-1) eight-layer, one-step HDI PCB with a price index of 200. The 0.5 mm pitch BGA can be routed on a (2-4B-2) eight-layer, three-step HDI PCB with a price index of 350. The number of lamination steps is the most signifi-

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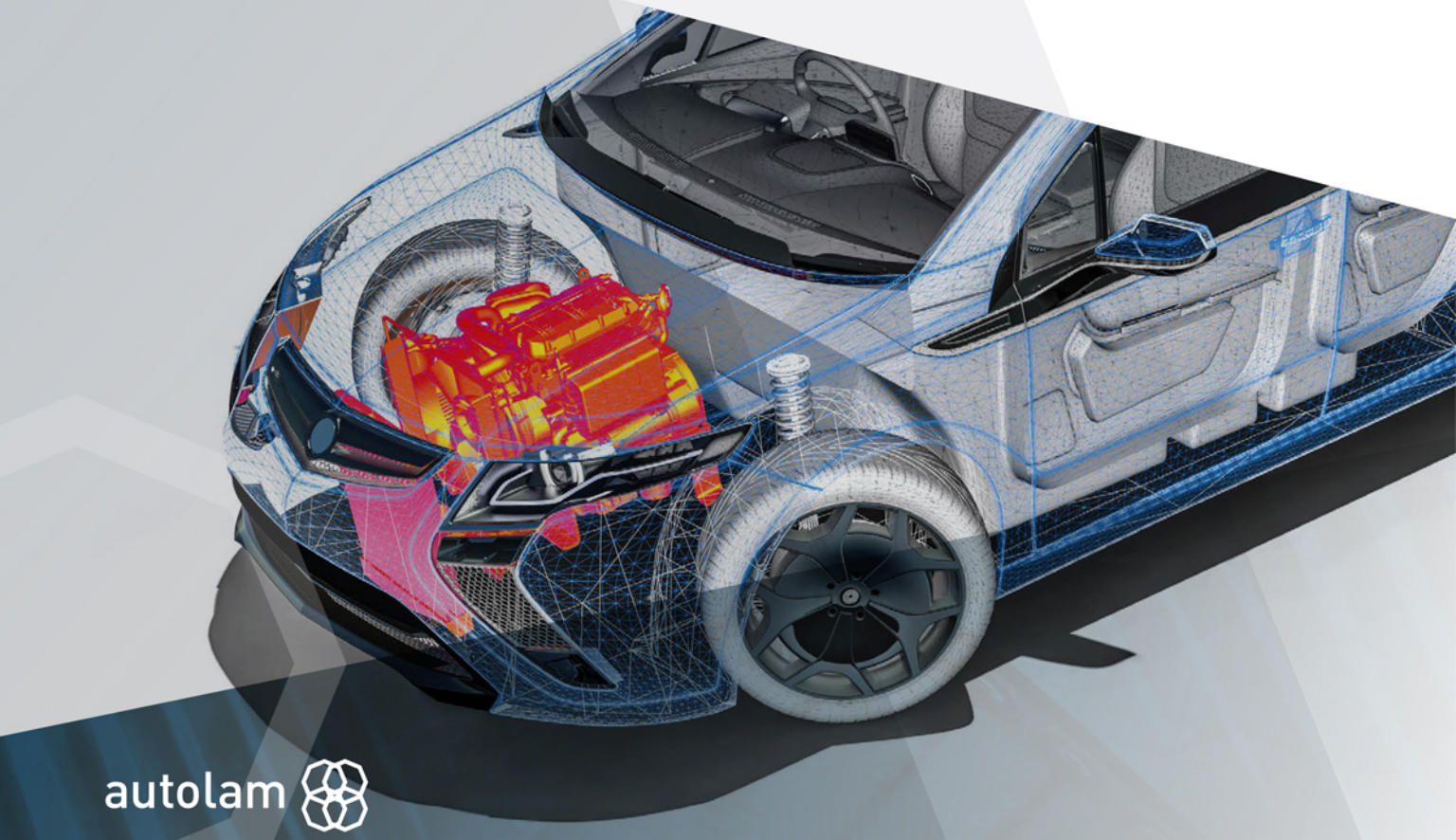

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cant cost driver for HDI and ultra HDI PCBs. Designs with BGAs equal to or less than 0.4 mm and multiple rows challenge the capability of HDI suppliers, which leads to the use of UHDI design parameters and thereby reduces the availability and increases the cost.

Material Selection

Correct material selection that complies with the performance and functionality of your application also plays a crucial role in the PCB cost.

The most common stackups of standard PCBs are specified with 35 µm Cu on all layers. The manufacturer starts on 17.5 µm Cu on outer layers and 35 µm Cu on inner layers, since the final outer layer Cu thickness reaches approximately 35 µm after plating. But 35 µm Cu on the inner layers isn't always required and can be replaced by 17.5 µm for the current flowing in many electronic devices. This, in turn, lowers costs.

Beyond this, Cu thickness above the standard 35 µm represents a considerable extra cost.

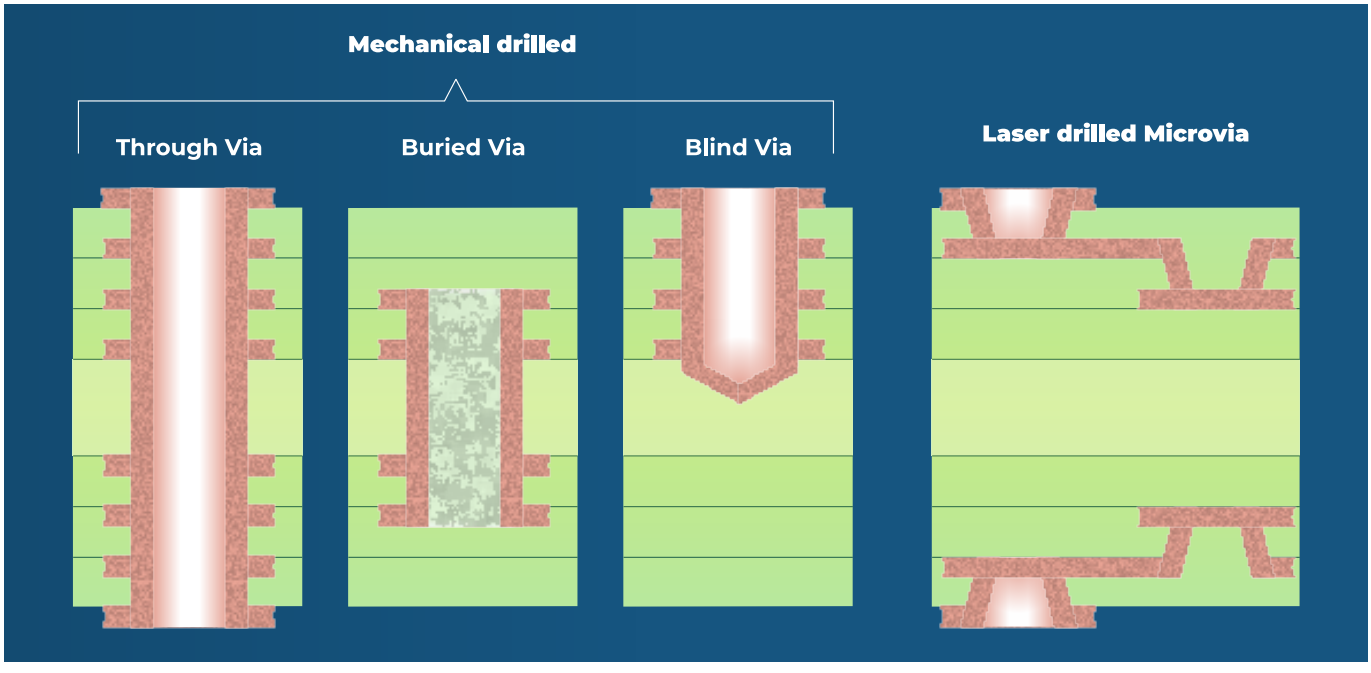
The base material choice depends on the PCB technology used for your application and the performance needed. By specifying a specific brand and type of material, you diminish the supplier availability and often prolong the lead time of the suppliers by adding material purchase time.

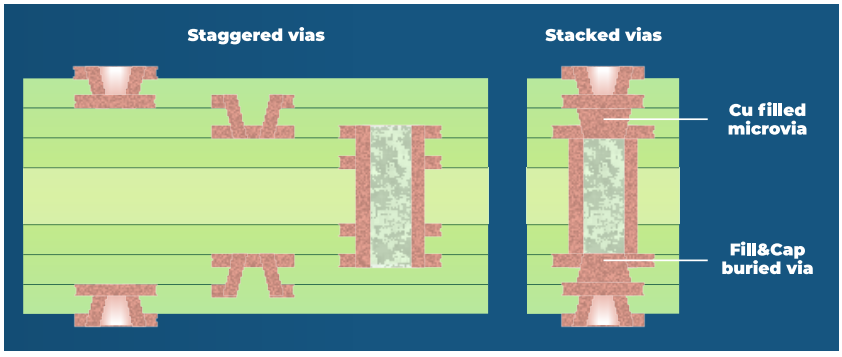
Seeking advice on the material specification from a specialist like ICAPE can save time and money by ensuring that your choices are based on performance rather than a specific brand and type of material. We recommend specifying the important critical material characteristics for the performance of your application, including glass transition temperature (Tg), coefficient of thermal expansion (CTE), dielectric constant (Dk), dissipation factor (Df), comparative tracking index (CTI), and maximum operating temperature (MOT). Thereby you allow the supplier to provide their offer based upon the most available and cost-optimized material fulfilling your specified criteria.

PCB Thickness and Stackup

Standard stackups contain only one sheet of prepreg in between each conductive layer. Using two or more sheets of prepreg will increase the PCB cost by approximately 2.5–6 USD/m^2 per sheet.

The most common PCB thickness is 1.6 mm, but could the thickness be reduced to 1.0 mm or 0.8 mm without compromising the mechanical or electrical performance? Reducing the thickness can provide direct cost savings on the PCB price of 1–2 USD/m^2, but it also reduces the weight, leading to large cost savings on the





freight and finally, it will reduce the weight of your application.

Panel Design and PCB Separation

Suppliers use standard-size production panels between 18" x 24" to 21" x 26" but some of the newest factories are increasing to double-size production panels like 28" x 49" to optimize the production cost. Most PCBs are delivered in a customer-defined delivery panel designed to optimize the assembly cost. The optimization of the supplier production panel and the customer-defined delivery panel is very important to minimize material waste.

Panel designs of PCBs with odd shapes can lead to undesired and inefficient material utilization. Engineering of these panel designs using rotated steps and nesting, resembling the old computer game Tetris, will often lead to substantial cost savings.

Rigid PCBs are mostly either milled on a CNC routing machine using a standard routing bit of 2 mm, prepared for depanelization by V-cut scoring, or a combination of both CNC milling and V-cut.

The V-cut is cheaper and faster for both the PCB manufacturers and for the post-assembly depanelization, but it leaves a rough PCB edge, and ceramic components must keep a minimum 2–3 mm board edge safety distance to avoid undesired component stress during the V-cut depanelization.

The depanelization of panels with break-tabs is more time-consuming since every break-tab must be removed by a mechanical cutter or the gentler routing method.

PCB Complexity and Design Wiring Density

The component size and wiring density are the main qualifiers of the PCB technology and layer count needed. Design features like minimum trace and space as well as minimum via-hole size limit the supplier range and thereby have a direct impact on the PCB price.

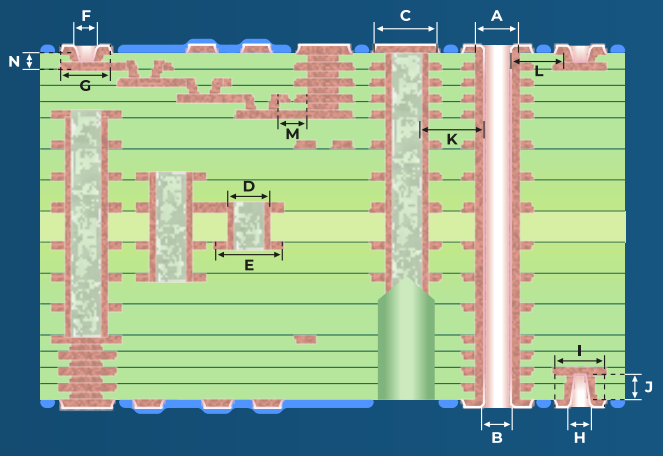
We are often asked specific questions about the cost impact of increasing the number of layers, adding microvia steps, reducing trace width and space, reducing hole sizes, etc.

Layers vs. price: Going from two to four layers increases the PCB cost by approximately 50% and for every two layers up to 12 layers will increase the cost by approximately 30%. At higher layer quantities, the percentage increase per extra layer pair declines.

Standard ML vs. HDI additional microvia steps: Going from a standard 10-layer PCB to a 10-layer one-step microvia HDI increases the cost by 50–60%. Adding buried vias from layers two to nine and microvias from layers two to three plus eight to nine increases the cost by 100%. Each additional microvia step increases the cost by 100%.

Trace and space: At ICAPE, we recommend that mainstream low-cost products use 6 mil/150 µm trace and space since all suppliers will be available, including the really dedicated low-cost suppliers. Reducing the trace and space to 4-mil/100 µm may exclude some dedicated low-cost suppliers, increasing the cost. Reducing the trace and space to 3-mil/76 µm will further reduce supplier choice and will mainly only be possible for HDI suppliers. Reducing the trace and space to 2-mil/50 µm will only allow suppliers with UHDI capability.

Minimum via hole size and tolerance: Most suppliers can offer plated through-hole 0.3 mm via-hole size without additional cost. Reducing to 0.2 or 0.25 mm via-hole size may increase



	Mechanical Drilled Holes Laser Drilled Holes	Standard in mm	Advanced in mm	Standard in mil	Advanced in mil
A	PTH & Buried Hole	0,20	0,15	8	6
B	Finished PTH & Buried Hole	0,12	0,07	5	3
C	PTH & Buried Pad diameter	Drill + 0,25	Drill + 0,15	Drill + 10	Drill + 6
D	Buried Hole single core	0,15	0,10	6	4
E	Buried single core Pad	Drill + 0,2	Drill + 0,12	Drill + 8	Drill + 5
F	Microvia Laser drilled	0,10	0,06	4	2,36
G	Entry & Capture pad	Drill + 0,15	Drill + 0,12	Drill + 6	Drill + 5
H	Skip Via Drill	0,20	0,15	8	6
I	Skip Via Pad	Drill + 0,2	Drill + 0,18	Drill + 8	Drill + 7
J	Skip Via depth	0,15	0,2	6	8
K	PTH to PTH	0,35	0,3	14	12
L	PTH to Microvia	0,279	0,228	11	9
M	Microvia to Microvia	0,25	0,15	10	6
N	Microvia Dielectric	0,06-0,08	0,10	2,36-3,15	4

the cost by 5–6 USD/m^2. Going below plated through-hole 0.2 mm via-hole size is only recommended on PCB thickness less than 1 mm and it will increase the price significantly. The common finished tolerance on plated through-holes is ±0.1 mm; tighter tolerances may require a change to a more sophisticated surface finish.

Additional expensive processes:

- Peelable mask and Kapton tape
- Hard gold
- Edge plating and plated half holes
- Plated through-hole copper requirements beyond IPC Class 3
- Back-drilling
- Countersink holes
- Via filling IPC type 5, 6, and 7

Surface Finish

The surface treatment must comply with the component choice, but it is important to consider the price implications of your choices. The main surface treatments based on price are: OSP, LF HASL, immersion Sn, immersion Ag, ENIG, and ENEPIG.

The surface treatment percentage influence on the price depends on the PCB cost driven by the technology, layer count, and board complexity.

On a two-layer PCB, the surface finish using LF HASL would represent 8% of the total cost. On the same PCB using ENIG, the surface finish would represent 30% of the total cost. On a 10-layer PCB, the surface finish using LF HASL would represent 2.5% of the total cost. On the same PCB using ENIG, the surface finish would represent 9% of the total cost.

The relation of the PCB costs to the surface finish and assembly technology of components can result in considerable cost savings, which you can easily use to your advantage.

Summary

The cost structure varies between suppliers, and it is difficult for PCB developers and designers to predict the most cost-optimized design and PCB specification. Having an experienced partner like ICAPE Group is your easiest pathway to extensive PCB-technology knowledge and related cost impacts. **DESIGN007**

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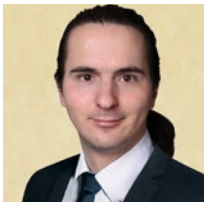
Erik Pedersen is FAE and quality director at ICAPE Group.



Richard Koensgen is a field application engineer at ICAPE Group.

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My Anti-venom to PCB Cost Adders

Target Condition

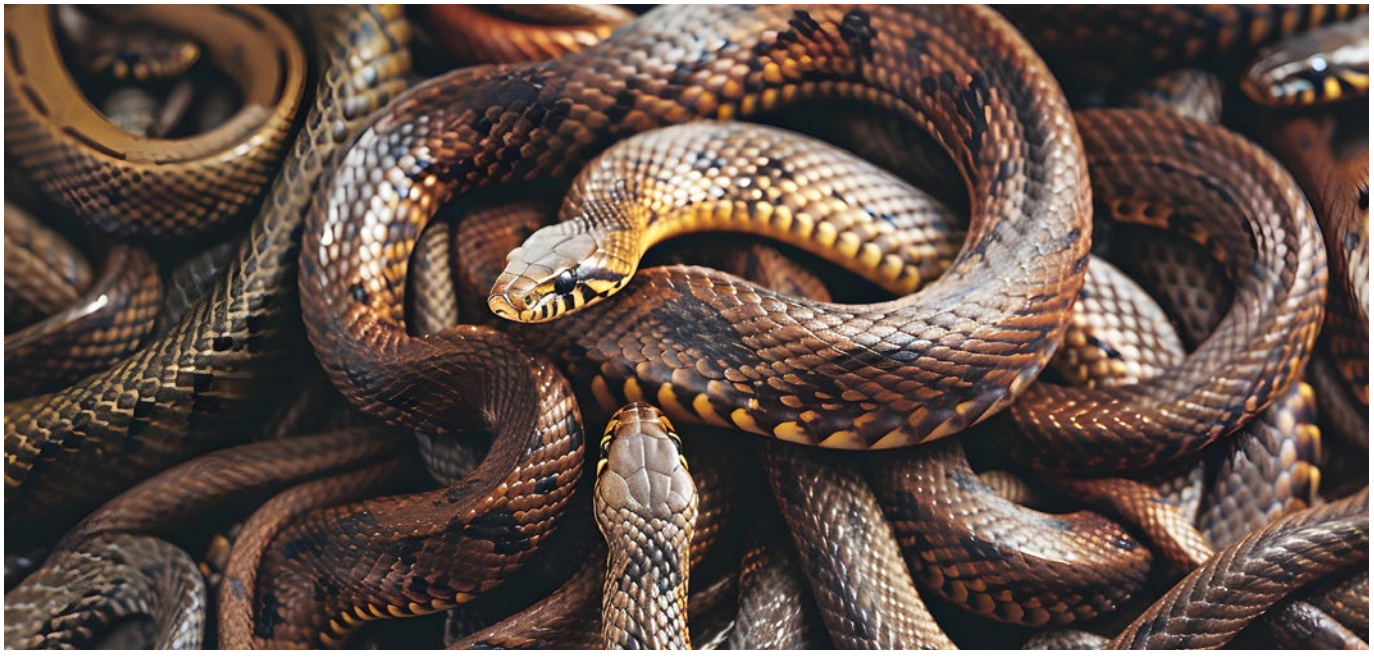
Feature Column by Kelly Dack, CIT, CID+

As a kid, I remember long, hot, cross-country trips to the Midwest with my grandparents to visit relatives. Riding in the backseat of a 1970s station wagon without air conditioning, the only thing I had to look forward to was stopping at Stuckey's in Oklahoma, which had a snake farm right next door. As luck would have it, after a hundred miles of passing signs advertising "Ramona's Snake Farm," Grandpa pulled in and made my trip come alive. I'd never seen a poisonous snake up close, and there were hundreds of them.

Snake pits, snake handlers, and venom-milking demonstrations garnered lots of oohs, ahs, and applause from the motor-tourists, including me. The handlers explained the snakes' habitats and unique characteristics and, most importantly, how to avoid getting bit. I left the snake farm with a greater understanding of snakes, and I'm proud to say I've never been bit.

One fairly benign species is *Vipera berus,* known as the common European adder, a venomous snake that isn't particularly aggressive, nor is its bite fatal. However, PCB designers risk getting bit by "adders" of another kind: *Serpens addit nimium pretium,* or simply, cost adders. Often coiled up in product development teams' brainstorming sessions or lurking inside the unexplored settings of our PCB design tools, these dangerous critters are of the profit-killing species.

In my walkabouts through the PCB design and manufacturing jungles, I've met many PCB designers who have suffered painful bites from these cost adders. These critters are particularly



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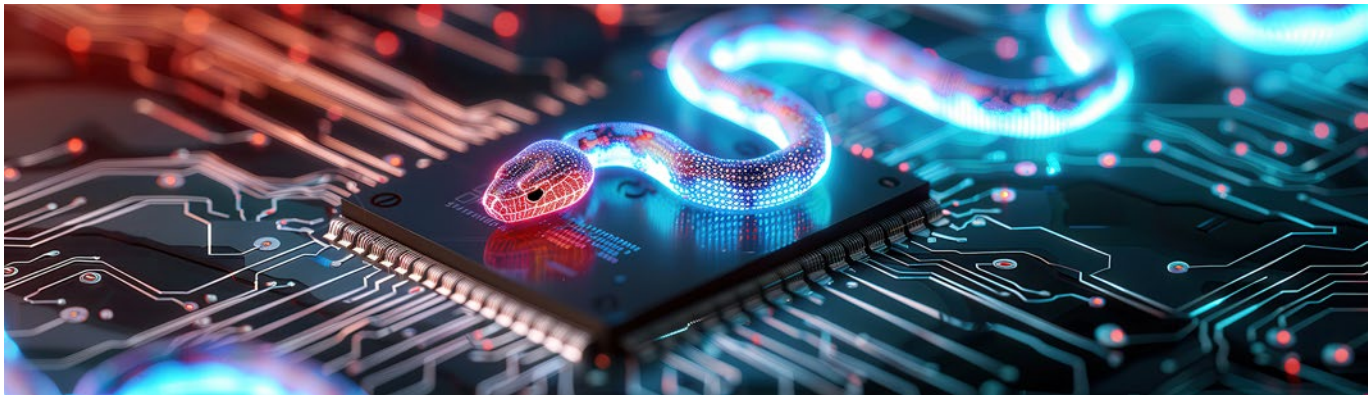


dangerous when a PCB designer steps naively into unfamiliar areas and does not know where to look. I have been bitten many times by the cost adder, but I've learned from my mistakes.

Now, I'm offering a few free doses of cost adder anti-venom.

Species: *Serpens Materia* (Material Cost Adders)

While most think of PCB material as simple glass-epoxy sheet stock or FR-4, PCB laminates have expanded into very advanced, brand-name, trademarked product lines that target specific performance and operational requirements for advanced PCBs.

When a PCB design layout goes to production, be wary of *Serpens materia*. Fabrication drawing notes must contain a material specification through which the PCB is made. Global PCB fabrication suppliers prefer simple glass/resin or polyimide laminates that can be readily procured from multiple sources. But often, PCB designers make the mistake of specifying brand-name materials or part numbers when it is not required. Other designers even declare "no substitutions." Designers who proceed in this manner without advanced understanding and justification are reaching dangerously into the den of *Serpens materia*. When their design moves to volume quantities, they will most certainly experience a painful strike from this adder with swelling of cost and necrotic product profit margin to follow.

The anti-venom for *Serpens materia* is modest but powerful. It must be injected directly into the design fabrication note-specifying material. After dosing, a basic material note's brand name, cost swollen specification can heal by stating: "Materials: Laminated, glass base, epoxy resin type FR-4 series or equivalent per IPC-4101 with Tg >/= 130°C and a Td >/= 300°C electro-deposited copper foil. Nominal base (starting) copper thickness for all layers shown on stackup detail."

Species: *Serpens Processus* (Process Cost Adders)

There are many ways to process a single feature on a PCB. For example, a board edge can be routed out, punched out, V-scored, laser cut, or even cut with an abrasive water jet. The way the designer lays out the shape of the board geometry will allow or eliminate many of the available processes. If a board outline maintains a rectangular shape, it can tolerate almost any process and allows the supplier to use V-scoring, which can be very cost-effective.

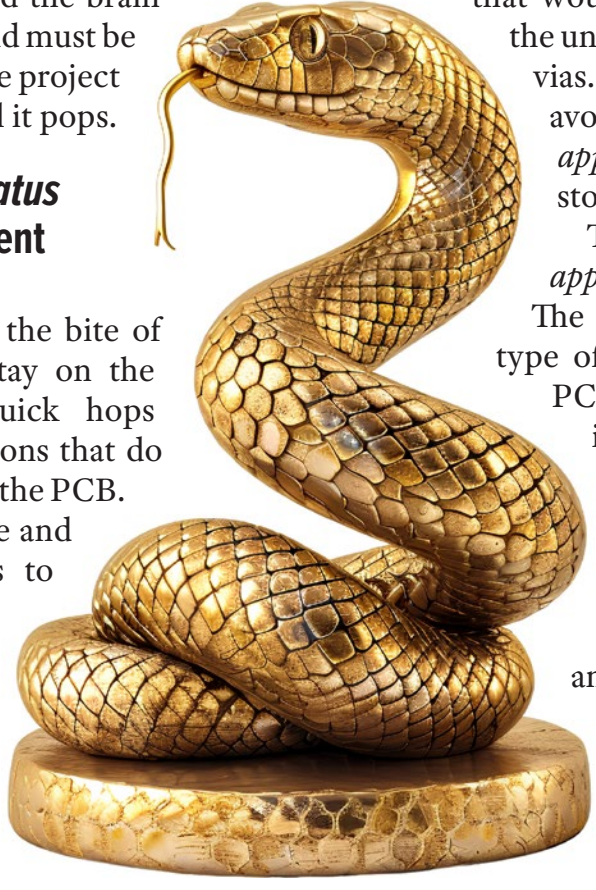
But rounding the corners to eliminate a sharp edge means an additional process step of routing to form the rounded edge. With rounded corners and straight edges, a PCB can be processed with a combination of V-scoring and routing at a cost for the additional process. Rounded features on a PCB outline are notorious hiding places for *Serpens processus* because of the additional process of routing and associated machine time or shifting the processing to a tab-route solution requiring mouse bites.

Mouse bites can cause localized stress on the PCB edge and lead to component cracking. *Serpens processus* is a wily species, often cohabiting with other, beneficial process species. To avoid being bitten, designers must focus on design constraints, keep them simple, and be aware of design features that add processing. Common lairs for process cost adders are PCB outlines, hole definitions, unique sizing, finishing, or coatings, especially ones requiring extended cure times.

The anti-venom is applied topically and serves mostly as a repellent; PCB designers must apply heavily during times of early project planning and treat fellow stakeholders who might be unaware of the dangers. Signs of an early bite, however, will materialize via stakeholder team suggestions describing oversized, curvy-shaped PCB designs with both plated and unplated countersunk mounting holes. In rare cases, wild visions of PCB stackups capable of carrying 80 amps and running down an ordinary soldering line must be treated immediately. In these cases, the venom of the process cost-adder has reached the brain tissue of this stakeholder and must be stopped before reaching the project budget and swelling it until it pops.

Species: *Serpens Apparatus* (Machinery and Equipment Cost Adders)

The safest way to avoid the bite of *Serpens apparatus* is to stay on the high ground, making quick hops between the machine stations that do the work of manufacturing the PCB. If a designer can clearly see and understand what it takes to hop to the next machine station without falling to the adder-infested jungle floor, the chances of being bitten by *Serpens apparatus* decrease greatly. But many PCB designers fail to study the equipment and capabilities of the fab and EMS providers, relying only on the PCB design software as a GPS guide.



We see news stories about travelers not researching their destination and winding up in dangerous situations by relying solely on GPS. Unfortunately, designers often suffer the same metaphorical fate. PCB design software can convert almost any geometric feature into a process machine language. Via padstacks are not only identified as drilled and plated holes, but our layout tools now invite designers to select from several filling and capping options without identifying the added cost or equipment needed.

Just last week, I had to rescue a designer who had fallen to the jungle floor in this manner. He'd pressed some via definition buttons and unknowingly stirred up a nest of *Serpens apparatus.* In the nick of time, I yelled, "Cost adder, watch out!" Once we scrambled back up on the DFM observation platform for a design review, we could clearly scope out the equipment that would have been required for the unnecessary filled and capped vias. We were lucky enough to avoid being bitten by *Serpens apparatus* and lived to tell the story.

The anti-venom for *Serpens apparatus* does not yet exist. The best prevention for this type of bite involves traveling to PCB design and manufacturing trade shows and taking frequent tours of PCB and EMS manufacturing facilities. There is simply no better way to get in touch with the equipment and the people who run it. To remain above the manufacturing jungle canopy and to know where to jump next, PCB design-

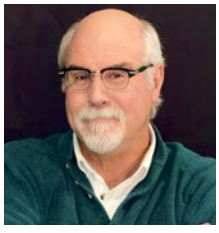
ers must become familiar with the following equipment and their respective capabilities and design requirements:

- Drilling machines
- Photoimaging equipment
- Plating and etching tanks
- Wet coating machines
- Laser direct imaging machines
- Printing machines
- Flying probe test equipment
- Solder printing machines
- Pick-and-place equipment
- Conveyers and pallets
- Reflow ovens, wave and selective soldering equipment
- Optical inspection equipment
- Routing, nibbling, and v-scoring equipment
- Functional and in-circuit test equipment

Know Your Cost Adder Species

As PCB designers, we cannot wander blindly and naively within our PCB design layout tools—clicking buttons and assigning values—without the ability to count the cost of such actions. Whenever we guess what is needed to form a PCB feature without understanding, we are, in effect, sticking our appendages into the cost adder's den. If you're like me, you are a PCB designer who learns in person. You need to get a tactile understanding of the subject matter at hand. To educate yourself with the excitement of a kid in a snake farm, you need to make every effort to tour a PCB manufacturing facility and/or attend a trade show displaying lots of materials, processes, and equipment. There, you can safely wander the aisles and view many PCB manufacturing cost equivalents to rattlesnakes, water moccasins, vipers, and all the various types of adders safely behind the glass or yellow lines painted on the concrete floors.

Before it's too late, slowly and cautiously step away from your PCB design laptops. Do not make any sudden moves. Turn and run to the closest PCB manufacturer or trade show to learn more about what it takes to keep PCB project costs low. **DESIGN007**



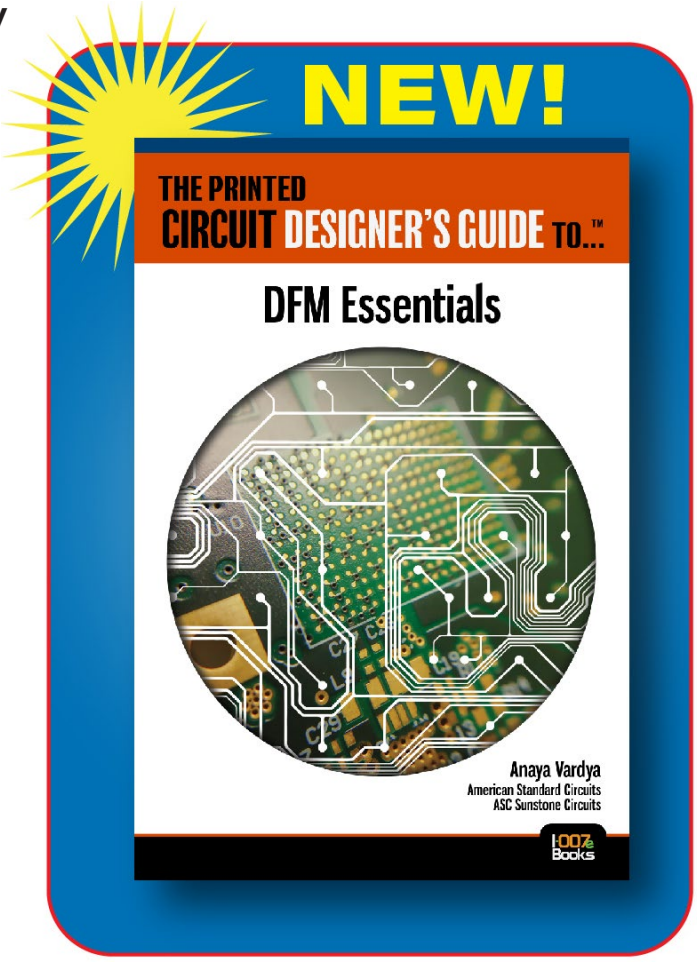
Kelly Dack, CIT, CID+, provides DFx centered PCB design and manufacturing liaison expertise for a dynamic EMS provider in the Pacific Northwest while also serving as an IPC design certification instructor (CID) for EPTAC.

To read past columns, click here.

BOOK EXCERPT

The Printed Circuit Designer's Guide to... DFM Essentials

Chapter 10: Cost Driver Summary



Low-cost Adders (<10% board cost)

Complex routing and scoring mean a small increase in process time, but a process is still required which will be driven by NC programming; it may limit tool life as a function of diameter. Thicker or thinner PCBs (>0.093" [0.229 mm], <0.030" [0.762 mm]) means a material cost variation but it is minimal. Via plug or button print requires a small process change to the screen-print mask dot.

Medium-cost Adders (10–25%)

Regarding drilled hole quantity, there is a cost adder for high-density design-driven hole count and process time. With smaller drilled hole size, the small drill diameter (<0.010" [0.254 mm]) limits throughput and stack height. Embedded resistors with Ohmega/Ticer technology will need additional core testing and finished board verification. Non-FR-4 materials, like PTFEs, can be 10 to 20 times the FR-4 cost, and material cost is generally 25–50% of the board cost. Edge plating will have additional processes required prior to plating.

High-cost Adders (>25% board cost)

Advanced technologies may become "science projects" with industry non-standard processing or materials, or "bleeding edge" technology (<0.003" [0.076 mm] L/S, 1:1 aspect ratio microvias, 0.4 mm BGA technology, etc.). Sequential lamination and complex via structures, as well as metal core or external heat sink requirements, also add cost.

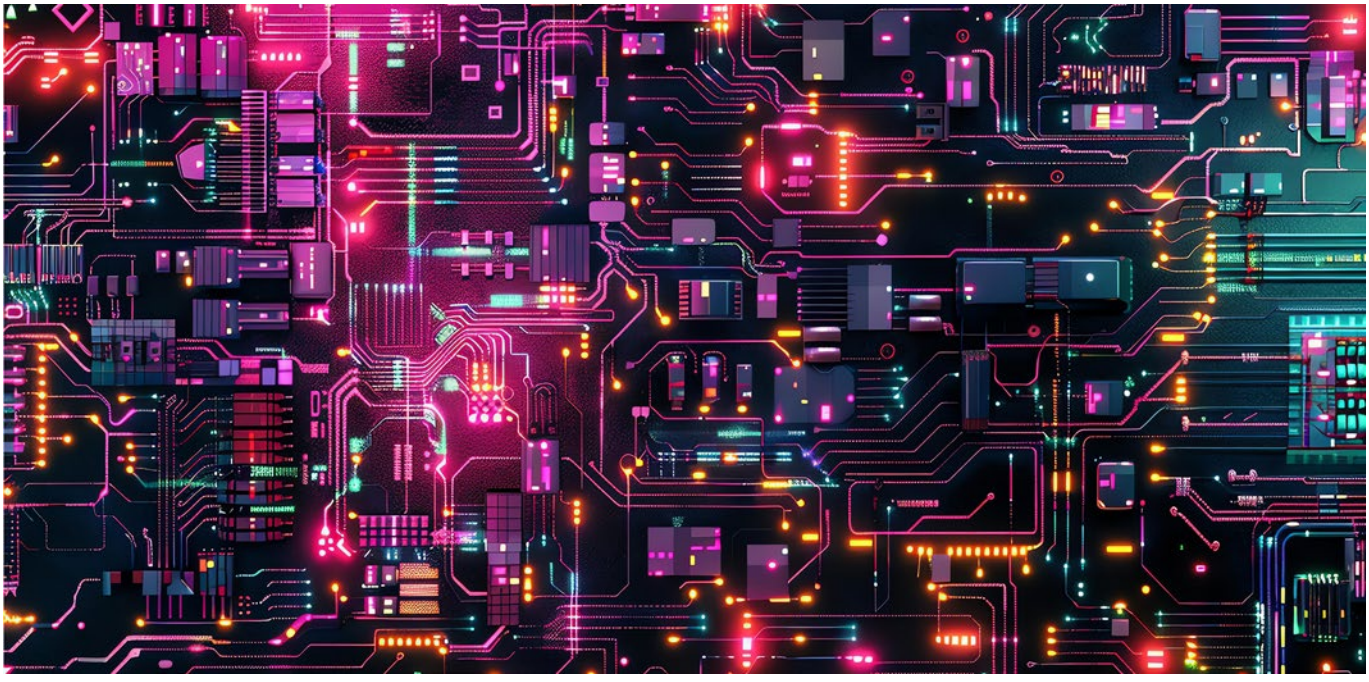
If layer count will be >30 layers, the yield impact can be significant. Combination/hybrid material sets can be high-cost adders. Regarding material/panel utilization, test coupons and board size can greatly reduce panel utilization; array configurations reduce panel utilization with unusable real estate; and there may be limited availability of panel sizes.

Selective plating means multiple surface finishes or multiple thicknesses, complex processing requirements (e.g., masking), and the yield risk of combining non-standard processes. There are also cost adders for line width and spacing below industry standards for any given copper weight:

- ½-ounce copper: 0.003"/0.003" (0.076 mm x 0.076 mm)
- 1-ounce copper: 0.004"/0.004" (0.102 mm x 0.102 mm)
- Ultra-high-density interconnects
- Sub 1 mil line/space (25 and 15 micron)

Understanding the cost drivers in PCB fabrication and early engagement between designer and fabricator are crucial elements that lead to cost-effective design success.

This chapter was extracted from the newly published book, The Printed Circuit Designer's Guide to DFM Essentials, now available free from the I-Connect007 library.



Impact of the Altium-Ansys Partnership on PCB Design

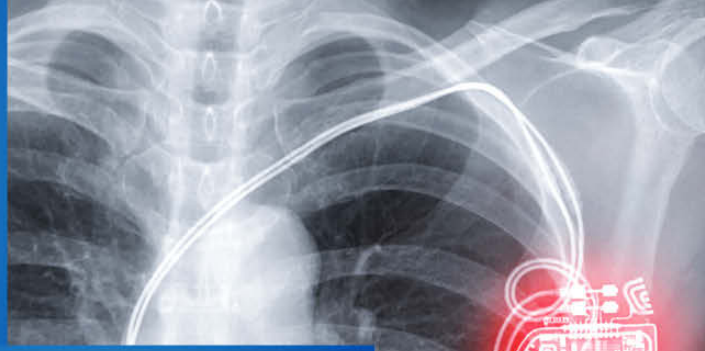
Article by Josh Moore
ALTIUM

There's a saying in electronics hardware design: "There are two types of electronics designers: those who have signal integrity problems and those who will." This adage emphasizes the inevitability of encountering and the need to address signal integrity (SI) and power integrity (PI) issues.

It has often been used as a clever yet prophetic sales and marketing tactic by software vendors at a time when electronic products were rapidly evolving, becoming higher-performing and increasingly complex, integrating a multitude of functions into ever-smaller form factors. This inevitably contributed to a significant increase in signal quality and power problems.

It was also a time when design organizations and their engineering teams were working to overcome numerous challenges, evolving and adapting their design methodologies and processes to overcome the increase in signal- and power-related problems.

- **Complexity in electronic designs:** Circuit and systems complexities made it challenging to ensure that designs meet the required specifications for performance, reliability, and new regulatory compliances without extensive testing and revisions.
- **Cross-domain design and simulation silos:** The printed circuit board (PCB) simulation EMI, EMC, thermal, and signal behavior had to be performed independently from the layout designer by simulation specialists using specialized tools.



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This separation was inefficient and error-prone, as ad-hoc processes and manual transfer of data between tools contributed to inaccuracies, miscommunication, and a lack of coherence in the design process.

- **Iterative design and simulation cycles:** The lack of integration between design and simulation tools resulted in an iterative and lengthy process of design, testing, and redesign, often late in the design cycle. This not only slowed down the development process but also increased costs associated with additional prototyping and testing.
- **Performance and reliability issues:** Without the ability to accurately simulate the real-world behavior of electronic components and systems during the design phase, there were higher risks of encountering performance issues or failures in the final product. This often led to increased warranty claims, product recalls, or field repairs.
- **Time-to-market pressures:** Reducing the time to market for new electronics products was crucial. The disconnect between the design and analysis phases led to longer development cycles, as potential issues only become apparent late in the design process, requiring costly and time-consuming revisions.

If those challenges and issues sound all too familiar, they should. They are just as relevant today as they ever were, and they're being further exacerbated by the inevitability-turned-certainty of signal integrity and power integrity-related issues inherent in modern electronics hardware.

While modern electronics hardware requires more comprehensive simulation for signal and power integrity, thermal reliability, and electromagnetic analysis, the goal remains the same: to ensure the final product meets the required specifications and regulatory compliances to perform as intended in the real world.

Although it may seem counterintuitive, by employing the best simulation tools, design organizations can and do achieve that goal, as evidenced by the plethora of properly functioning electronics products in the world. However, simply having the best simulation tools is not enough for design organizations, as many still struggle and need help with the numerous operational and efficiency challenges that lead to potential scheduling delays, increased costs, and time-to-market risks.

Overcoming those organizational challenges can be achieved through effective and efficient communication and collaboration between PCB layout designers and simulation engineers. Integration of the two domains is highly dependent on a functional, iterative process involving numerous cycles of design, simulation, and adjustment. Streamlining the iterative process through intelligent, bidirectional integration can eliminate simulation-related operational and efficiency challenges. These challenges arise from all-to-common disjointed, manual, and isolated design methodologies.

Industry Leaders Join Forces

To address these challenges, Altium Ltd. and Ansys Inc. are bridging the gap between

"Simply having the best simulation tools is not enough for design organizations..."

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the PCB design and simulation domains. Their partnership has streamlined electronics hardware design by seamlessly integrating Ansys HFSS advanced simulation capabilities within the Altium PCB design process.

The collaboration between Altium and Ansys is driven by a shared vision to eliminate the disconnect between electronics design and advanced simulation, a common hurdle in electronics development that often leads to inefficient design iterations, scheduling delays, increased costs, and time-to-market risks.

This collaboration culminated in the development of the Altium-Ansys Co-Designer smart digital bridge. It provides design organizations with an intelligent, bidirectional integration that enables continuous data exchange between the Ansys and Altium electronics design packages, replacing manual data exchanges and inefficient communication methods between designers.

Benefiting From an Evolved Process

A dysfunctional and disjointed design process is often marred from the start as PCB layout designers begin the design in isolation, without input or consideration for all the signal performance and power delivery requirements or implications. Without early collaboration and input from simulation engineers, organizations struggle to avoid the inevitable late-cycle delays, redesigns, and respins that stem from isolation. These challenges and their impacts on project time and cost are exacerbated as design complexities increase.

Even with some level of collaboration throughout the design process between PCB designers and simulation engineers, that collaboration is often through ad-hoc methods, including emails, screenshots, and casual conversations. These ad-hoc methods lack precision and intelligence, contributing to design adjustments that have the potential for misunderstanding or guesswork.

It is also far too common that multiple late-design prototype, test, and redesign cycles are accepted as a necessary evil. Waiting until the later stage of the design means design tweaks (big and small) are virtually guaranteed, requiring time-consuming redesigns and costly respins.

> "It is too common that multiple late-design prototype, test, and redesign cycles are accepted as a necessary evil."

The transition to a functional, iterative process fundamentally transforms the interaction, communication, and collaboration between layout designers and simulation engineers throughout the design cycle, from one of isolation and fragmentation to one of seamless and intelligent integration.

From Isolation to Left-shifted Collaboration

Enabling intelligent and integrated communication and collaboration early in the process allows simulation engineers to participate and contribute their insights on signal performance and power requirements in conjunction with the physical design considerations right from the start. This level of integration introduces real-time communication abilities between the designers and engineers. Inter-tool communication allows immediate discussions and clarifications of simulation results, fostering informed and targeted design adjustments.

From Late Cycle to Iterative Simulation

Instead of waiting for a nearly completed, or even worse, a completed design before conducting simulations, designs can be evaluated early and iteratively throughout the layout process. Simulation engineers and PCB layout designers can work seamlessly and synchronously, allowing for quicker iterations and faster convergence on optimal solutions, and significantly reducing development time and optimizing resources. This integrated design process is far more efficient, eliminating time-consuming late-cycle redesigns and reducing costly respins.

From Prototyping Risk to Strategic Verification

This proactive approach also allows virtual prototyping to be a strategic part of the verification process. Based on insights from iterative design refinements and simulations, it allows for real-world verification sooner in the overall product development process, minimizing post-development setbacks. This helps to ensure that the design is rigorously verified before entering production.

It underscores the importance of transforming the PCB design and multi-physics analysis process from a series of disconnected, manual steps into a cohesive, collaborative effort between PCB layout designers and simulation engineers. By doing so, design teams and engineering organizations can achieve a more efficient, effective, and successful design process, leading to higher-quality products and more predictable outcomes. **DESIGN007**

Josh Moore is a director of product marketing at Altium.

A Comprehensive Guide to Navigating Cost Drivers and Sustainability in PCB Production

Feature Article by Michael Marshall
NCAB Group

In May, I had the privilege of presenting "Cost Drivers in PCB Production" to attendees at the SMTA Wisconsin Expo. This presentation, one of our most popular, received tremendous feedback, inspiring us to share our insights more broadly through a comprehensive white paper on the subject.

In the realm of project management, cost drivers are elements that influence the overall expense of a project. These cost drivers can be categorized into two types: hard cost drivers and soft cost drivers. Understanding these categories is crucial for accurate budgeting, cost control, and financial planning. This white paper delves into the specifics of both hard and soft cost drivers, providing insight into their impacts effective management strategies, while also keeping in mind the aspects that contribute to the sustainability impacts of a PCB.

Hard cost drivers encompass direct, tangible costs that are quantifiable and associated with the physical aspects of a project. These costs are typically straightforward to estimate and track, making them critical components of project budgeting. In the white paper, we break down aspects like board size, layer count, and via types.

Soft cost drivers, on the other hand, are indirect costs related to the electrical design, engineering analysis, drafting, and modeling of the board. Hiring skilled professionals, using advanced design software, and conducting feasibility studies are integral to this phase. While these costs are not directly tied to physical components, they are essential for ensuring the project's feasibility, safety and adherence to desired specifications.

To explore this detailed article on cost drivers and sustainability impacts, click here.

References

NCAB Group offers a variety of design resources, including seven PCB design guidelines for multilayer, HDI, copper coin, semi-flex, UHDI, flex/rigid-flex, and stackups and impedances. We also provide a PCB checklist and some handy PCB design tips to help you get your PCB design right from the start.

Michael Marshall is a field applications engineer for NCAB Group.

MilAero007 Highlights

CACI Awarded $2 Billion Task Order to Provide Modern Digital Solutions to NASA ▸

CACI International Inc announced that it won an eight-year contract valued at up to $2 billion to provide digital solutions technology to standardize and centralize 11 of NASA's IT services under the NASA Consolidated Applications and Platform Services (NCAPS) award. NCAPS expands CACI's current relationship with NASA and will bring enterprise-wide automation across more than 200 systems from various NASA locations into a single program, thus enhancing efficiency while boosting productivity.

ispace RESILIENCE Lunar Lander Successfully Achieves Testing Milestone in Preparation for Mission 2 ▸

ispace, inc., a global lunar exploration company, announced today that the flight model of its HAKUTO-R Mission 2 RESILIENCE lunar lander has successfully completed thermal vacuum testing and remains on schedule for a Winter 2024 launch.

BAE Systems, GlobalFoundries Collaborate to Strengthen Supply of Essential Semiconductors for National Security Programs ▸

Under the strategic agreement, the companies will align technology roadmaps and collaborate on long-term strategies for increasing U.S. semiconductor innovation and manufacturing, with the joint goal of advancing the ecosystem for domestic fabrication and packaging of secure chips and solutions for use in aerospace and defense systems.

Lockheed Martin Selected To Develop Next Generation Weather Satellite Constellation ▸

NASA has selected Lockheed Martin to develop and build the nation's next generation weather satellite constellation, Geostationary Extended Observations (GeoXO), for the National Oceanic and Atmospheric Administration (NOAA).

Shane Whiteside Appointed as New PCBAA Chair ▸

Summit Interconnect President and CEO Shane Whiteside was recently appointed as chair of the Printed Circuit Board Association of America (PCBAA), replacing Travis Kelly, CEO of Isola Group. Shane's distinguished career in PCB manufacturing lends itself well to PCBAA's mission as an important advocacy vehicle for the PCB industry.

NASA, Boeing Provide Next Update on Space Station Crew Flight Test ▸

NASA and Boeing continue to evaluate Starliner's propulsion system performance and five small helium leaks in the spacecraft's service module, gathering as much data as possible while docked to the International Space Station.

DARPA Researchers Highlight Application Areas for Quantum Computing ▸

DARPA's Quantum Benchmarking program kicked off with the goal of reinventing the metrics critical to measuring quantum computing progress and applying scientific rigor to often unsubstantiated claims about quantum computing's future promise.

DESIGN TIPS #124:

ETCH COMPENSATION

What is minimum space and trace? The answer depends on the starting copper weight.

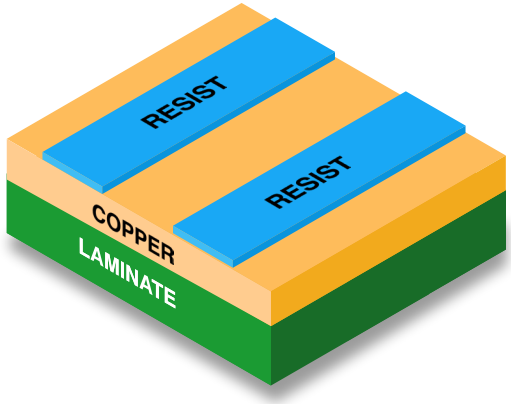
This is because we must do an etch comp on the traces in CAM to compensate for known etch loss. The space between traces after compensation will play a role in whether a board can be manufactured.

The lower the spacing width, the higher the cost. Designers don't always account for the proper starting copper weight after edge compensation.

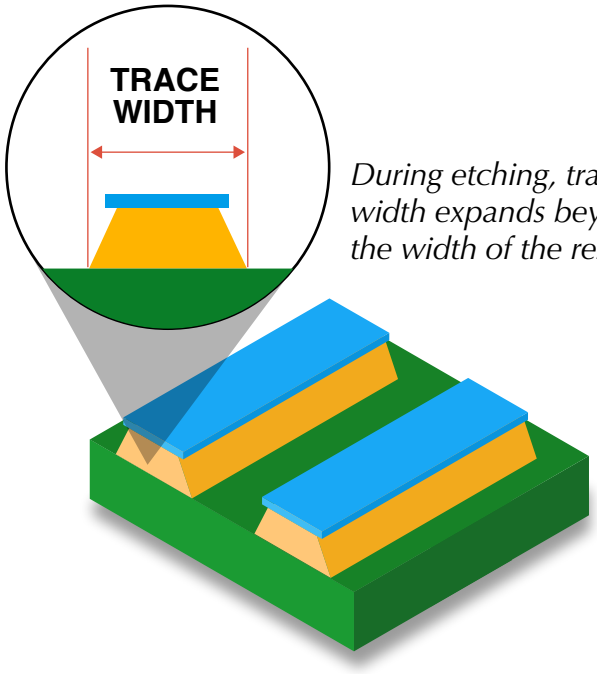
Design tips:

- For accurate starting copper weight, **add a half mil (.0005″) to all copper features**.
- **Start with 3/8 or 1/4 oz. foil**, reducing etch comp and less likely to cause a spacing issue.
- **Boards that call for full body electrolytic gold are not comped** to avoid gold slivers occurring during the etching process.

Before etching



After etching



During etching, trace width expands beyond the width of the resist.

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An Evolution in PCB Design Costs

Quiet Power

Feature Column by Istvan Novak, SAMTEC

In this column, I want to cover my experiences, particularly where costs are concerned, with printed circuit boards from the 1960s to the present day. I grew up in an apartment building in downtown Budapest, where I began doing hobby projects building circuits at our kitchen table. Now, I'm lecturing about the most recent advances in signal integrity at Oxford. We've come a long way. Over the decades, new technologies allowed users to have more layers, lower-loss dielectrics, fine-pitch surface connections, blind and buried vias, and HDI and HDI+ board constructions that allow us to design higher performing systems. I expect this trend to continue.

Today, to connect multiple components into a compact circuit, we mount the components on a printed circuit board. But in the late 19th and early 20th centuries, people would hammer nails into a wooden board and then wrap the leads of multiple components around them (the original breadboard). Household electronics, like vacuum-tube radios, amplifiers, and record players, all used a similar concept. The connection between components was done with wires, which were easy to replace if needed, and allowed connections in any direction. However, finding a particular wire in a chaotic three-dimensional wire blob was a real challenge.

As the number of connections increased, so did the possibility of mis-wiring something and manufacturing also became time-consuming. The printed circuit board technology gradually emerged. (If you are interested in the history of printed circuit boards, see references 2 and 3.) In the 1960s and '70s, the main cost driver was the number of layers.

Figure 1: A Philips B5X21A vacuum-tube radio with discrete wiring. You can see the front, middle (with the back removed), and back (with the cover removed and a jumble of wires and component leads). Fun fact: This radio still works even though it was manufactured in 1963[1].

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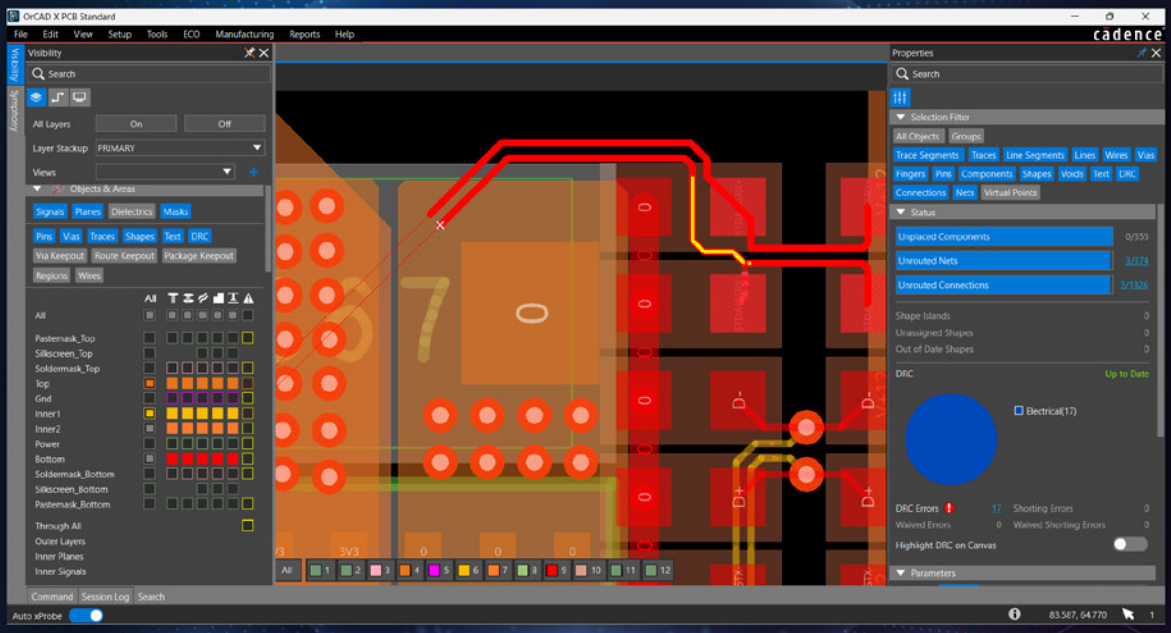

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PCBs on Layers

In the early days, PCBs had one or two connecting layers, which required only a single dielectric sheet with a conducting layer on one or both sides. As a child, electronics fascinated me, and as soon as I could read, I turned to hobby magazines. Some described the new technology: Instead of discrete wires, they could draw connections of electronic circuits on copper-clad dielectric, and then etch away the copper where the connection wasn't needed.

Later, I made little gadgets with transistors that I had purchased from a local hobby shop that sold materials, tools, and components for radio amateurs and hobbyists. With the non-market economy in those days, a transistor cost about the same as six pounds of bread.

I built small portable radios on homemade printed circuits. The first attempts failed miserably. The hand-drawn pattern of ink that had to be baked before etching often peeled off too early. Once I discovered the correct temperature, length of baking over the kitchen gas range flame, and the proper etching time, the boards became more reliable. An example is shown in Figure 2. It is the audio amplifier of a battery-powered portable radio I built in the late '60s[4].

By the late 1990s, glass-reinforced epoxy had replaced Paper Bakelite, and etching and plating had become carefully optimized and automated processes. The circuit complexity required several routing layers, plated through-holes, and blind and buried vias (which had recently become available). Instead of manually drawing the pattern with ink, engineers used CAD software to perform the routing. The CPU module in Figure 3 (reproduced from Slide 12[5]) had a 20" x 8.5" 24-layer PCB. The board did not have blind or buried vias and used only standard low-cost FR-4 laminates, but it had selective gold plating. The price of the prototype bare boards in small quantities was around $600.

As production ramped up, prices came down. In the 2000s, the cost of bare PCBs with standard laminate materials, no blind or buried

Figure 3: CPU module of SUN Microsystems V880/V890.

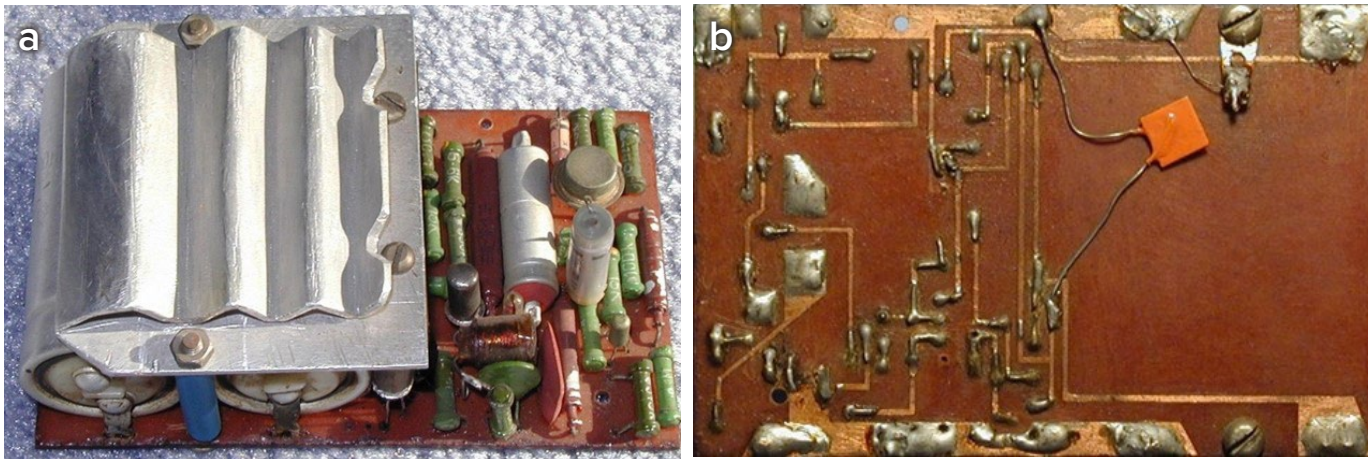

Figure 2: Homemade printed circuit board from the late 1960s. Figure 2a shows the top view of the single-layer PCB with the components. Figure 2b is the back side of the board with the copper traces. There was no need for vertical connections or plated through-holes, so the cost of the driver was simply the cost of the laminate. The color of the bare dielectric reveals this was an early Paper Bakelite board laminate. I recall the cost was probably around the price of a couple of scoops of ice cream at the time.


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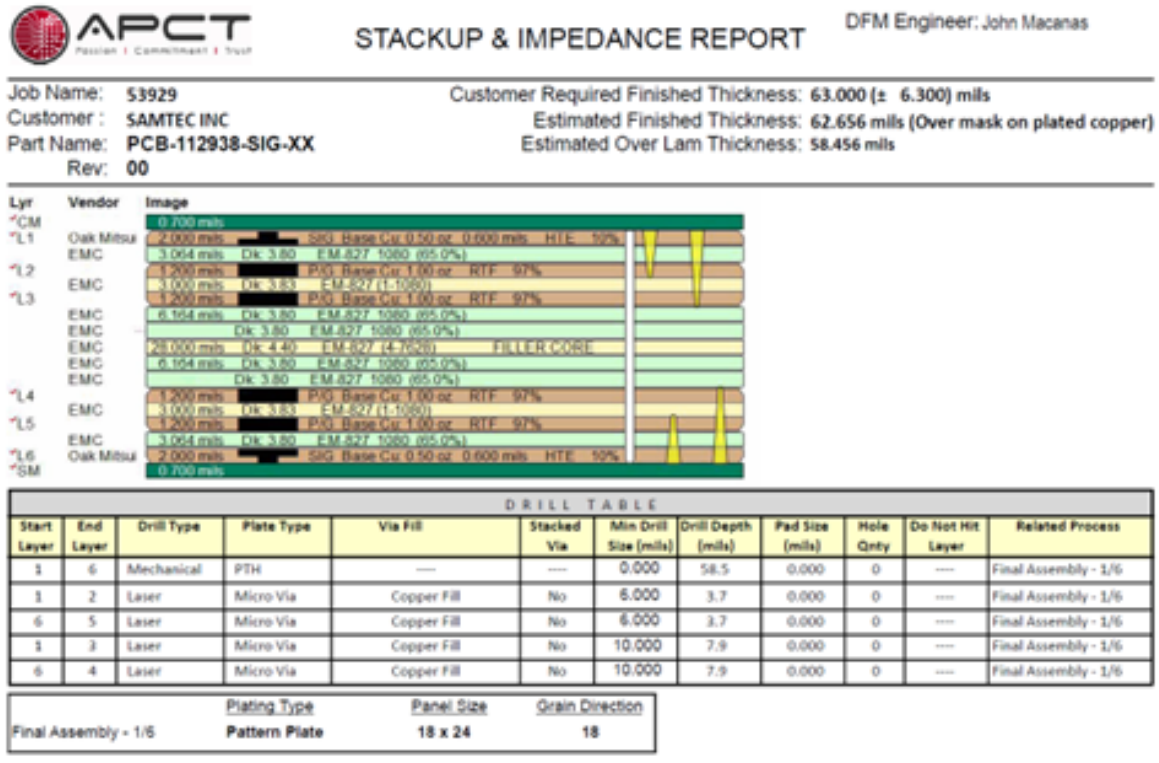

Figure 4: Six-layer board stackup and material definition.

vias or special finishes, could be calculated by multiplying the board's square footage by three times the number of metal layers. As an example, consider a board of 12" x 8" with 10 layers and no special technology. This board size means a 0.8 square foot area. As each processed metal layer was estimated having a cost of $3, the estimated cost become 0.8 x 10 x 3, or $24.

Now, we've reached the 2020s. In another article I wrote[6], I describe a simple six-layer board designed and built in 2023. The board was built with regular FR-4-like laminates and had four blind-via layers: two on the top and two on the bottom. The blind vias were copper-filled, but not planarized. Exposed copper was gold-plated. Due to the usually fixed setup costs commonly called non-recurrent expenses (NRE), the cost was a strong function of the number of boards in small quantities. The price of these boards was around $400 each.

As PCBs have evolved over the past 60 years, so have their associated costs. Now, with more efficient manufacturing, new technologies (such as 3D printing), and more automation, I expect to see even more changes in the costs of PCBs that will make them more efficient to produce, thus helping both the manufacturers and the consumers. **DESIGN007**

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Istvan Novak is the principal signal and power integrity engineer at Samtec with over 30 years of experience in high-speed digital, RF, and analog circuit and system design. He is a Life Fellow of the IEEE, author of two books on power integrity, and an instructor of signal and power integrity courses. He also provides a website that focuses on SI and PI techniques. To read past columns, click here.

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Asymmetric Hybrid Printed Circuit Board Design: Warpage Considerations

Article by Kaspar Tsang, Gause Hu, Jimmy Hsu, Aje Chang, Alan Sun, Brian Ho, Ryan Chang, and Thonas Su

Editor's note: This excerpt is from a white paper presented at IPC APEX EXPO 2024, and is intended to give an overview and recommendation on the topic. To see a list of full papers and other conference proceedings, please click here.

Abstract

The printed circuit board (PCB) accounts for a significant portion of the PCBA's (printed circuit board assembly) BOM (bill of material) cost. Designs with hybrid PCB stackup are adopted to reduce the cost of the PCB by using less expensive laminate materials in layers that do not have routings for high-speed signals (e.g., power and ground layers). The conventional hybrid PCB stackup design is symmetrical in the middle[1]. This engineering technique has been employed in the data center industry for quite some time. To extend the idea and optimize the purpose of hybrid PCB stackup design, the feasibility of an asymmetric hybrid stackup is currently being studied.

Asymmetric hybrid stackup offers greater flexibility and potential cost savings in high-speed traces routing[2]. However, the mechanical reliability risks in the asymmetric hybrid stackup are even more challenging than those in conventional hybrid PCB stackup. In this research, a team with diverse expertise, including design, material, and PCB manufacture process, was formed to study the effects of (1) different hybrid mate-

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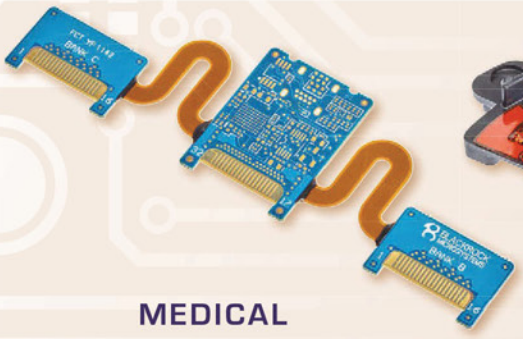

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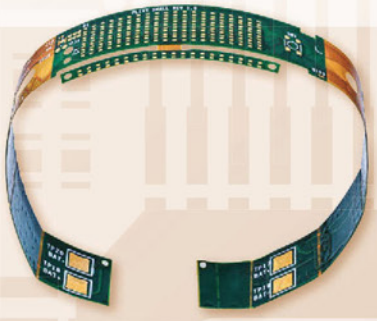

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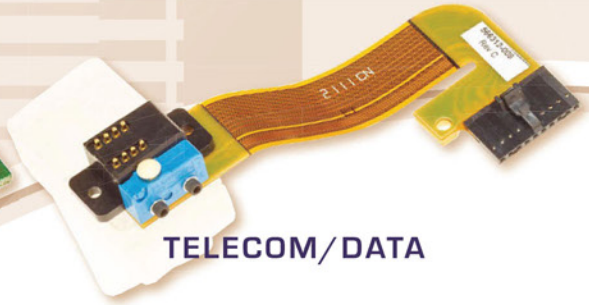

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rial combinations, and (2) various asymmetric hybrid stackup constructions on mechanical reliability performance using a qualitative approach. Unlike most other research that uses test coupons as the subject, a production-level data center mainboard design was used in this study, which provides more reliable test results and more accurate assessments.

Reliability test methods and results concerning warpage, delamination, via reliability, and brief signal Integrity comparison will be discussed in this paper. Recommendations on PCB manufacturing and design guidelines to mitigate the reliability risks associated with asymmetric hybrid PCB will also be provided.

Introduction

Reliability risks (warpage, delamination, conductive anodic filament, and via reliability) remain the major concerns in the usage of asymmetric hybrid PCB stackups. Conventional wisdom suggests that the manufacturing challenges and reliability risks of asymmetric hybrid PCB stackups are even higher than with symmetric hybrid PCB stackups. This research aimed to (1) understand the effects of different copper-clad laminate (CCL) material combinations and various constructions on the reliability performance of the asymmetric hybrid stackup, and (2) establish design and manufacturing guidelines to mitigate the reliability risks of the PCB, using a qualitative approach.

The assessment of reliability risks in the PCBA process, such as solder joint integrity, shock and vibration performance, as well as effects on components, falls beyond the scope of this research.

Stackup Designs

A 110-mil thick stackup (a thickness covers the majority of the data center mainboard design) containing 2 ounces of inner copper has been designed. Various asymmetric hybrid constructions for the stackup are considered in Table 1.

Table 1: Stackup design strategy

Stackup	Design Strategy	Layer of material (ULL1/ VLL)	Layer of material (Mid-A)	NOTE
#1	Pure high-speed material	15	0	Baseline
#2	Hybrid layers locating closer to center	13	2	Effect of hybrid layer location
#3	Hybrid layers locating midway between center and bottom	13	2	Effect of hybrid layer location
#4	Hybrid layers locating closer to bottom	13	2	Effect of hybrid layer location
#5	Half hybrid material/ half base material	8	7	Effect of hybrid layer quantity and construction
#6	All cores with hybrid materials	8	7	Effect of hybrid layer quantity and construction

PCB Design Recommendations

Based on the test results from this study, a couple of qualitative design recommendations could be established as follows:

a. When using asymmetric hybrid construction, it is essential to use a "thermal-mechanical robust" hybrid material.

b. By "thermal-mechanical robust," it means that the hybrid material, when used in a pure homogenous stackup, should be capable of passing reliability tests at the concerned thickness, hole size, and pitches.

c. The copper weight of the mirror layers in the stackup (e.g., L2 and L17 of an 18-layer stackup) must be the same, and the copper circuitry density must be similar (within a 5% difference).

d. The coefficient of thermal expansion (CTE) of the base material and the hybrid material shall also be similar.

e. Non-functional pads may be added to some plated through-holes to enhance delamination performance ("anchoring" the laminate). Roughly speaking, non-functional pads shall be added every 22 to 40 mils apart. However, keep in mind that the use of non-functional pads may have adverse effects on plated through-holes that connect to high-speed signal lines.

f. There shall be no known compatibility issues of the two materials (e.g., outgassing at the junction of the hybrid during lamination process) as advised by the CCL suppliers.

When the above requirements are met, there seem to be no restrictions on the (a) hybrid material loss category, (b) hybrid layer quantity, and (c) hybrid layer locations. This offers much more flexibility in routing.

In this study, the test board was designed as a 16-layer stackup with a thickness of 110 mils and a via-via pitch of 0.6 mm. Based on the test results and previous experience of PCB and CCL suppliers, the limits of asymmetric hybrid design could potentially be pushed to a 22-layer stackup with a thickness of 130 mils and a via-via pitch of 0.6 mm.

Conclusions

This research aimed to explore the thermal-mechanical and reliability risks of asymmetric hybrid PCBs using a qualitative approach.

Based on the test results, we can conclude that an asymmetric hybrid PCB stackup, when combined with suitable materials and following the technical recommendations from PCB designers, can yield reliability performance as good as a pure homogeneous material stackup design. Care should be taken to ensure that the evaluation has been conducted and focused solely on PCB raw card level performance. While some test matrices and material combinations demonstrated good reliability performance in this study, it does not imply that all the materials can be randomly combined and yield equally positive results. Companies intending to use asymmetric hybrid PCB stackup in their products are strongly advised to conduct their own research and develop their technical know-how, particularly concerning the effects of such PCB stackup on PCBA level reliability performance. **DESIGN007**

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Ryan Chang is with Intel in Taipei, Taiwan.
Thonas Su is with Intel in Taipei, Taiwan.

Dan Beeker (right) with (2nd from left) Troy Hopkins and Rick Hartley (center) at PCB East 2024.

Dan Beeker: Outstanding in his 'Fields'

Interview by Andy Shaughnessy
I-CONNECT007

At PCB East, I met with Dan Beeker, technical director at NXP Semiconductor, and a speaker at the conference. Dan always gives a spirited interview, so I asked him to discuss his class and challenges in the industry today.

Andy Shaughnessy: Dan, I understand your class was packed. Tell us a little about the class.

Dan Beeker: This was my first time teaching a class on the free day at PCB East, and that was pretty exciting. Mine was the first class of the day, and that can sometimes be a little scary because people might not come, but I ended up with a pretty full class. The class was focused on the behavior of electromagnetic waves. We're talking about a very simple perspective on wave theory and electromagnetic field theory. I put together a series of slides that explained what fields are, how you contain them, and how they behave in those structures.

My favorite analogy for electromagnetic field theory is the idea of plumbing. In water pipes, you have something stored in them, much like the energy stored in the space between a trace and a ground. That's the basic structure: Discreet conductors separated by a space. This is different from the ideas in the past that a blob of power vias does something and a blob of ground vias does something else to the fields. A blob of power vias or ground vias doesn't help you deliver energy. Each blob is made up of the same conductor. If you put power and ground vias together, then each of those discrete spaces follows the rules, and energy can be stored in those spaces.

It takes time. When you turn on the faucet for your hose, the water doesn't come out instantly. The water takes time to travel, and the same thing is true with energy, which travels at 6 inches per nanosecond in a PC board. The energy has no idea what's at the other

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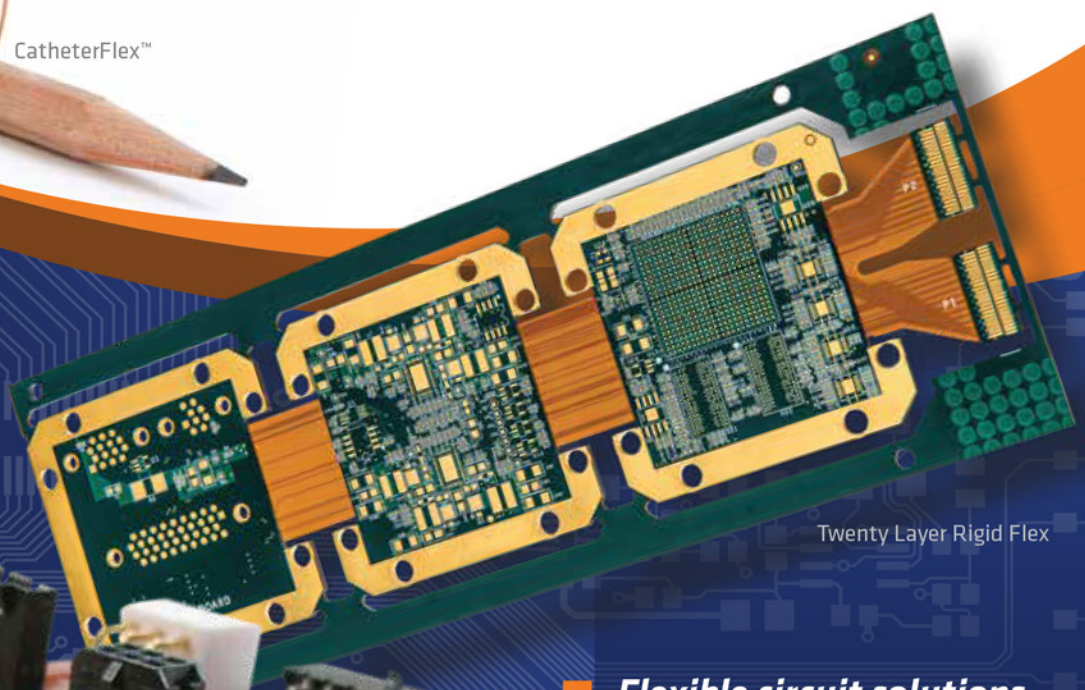

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end, so it just goes full bore till it gets to the other end, and then it behaves based on what's at the end of the pipe. If the pipe is connected to another pipe, it flows into the new pipe (the switch there is turned on). If there's a machine there (i.e., something that wants to use that energy, such as a motor, a light bulb filament, or a speaker), then that energy will be converted from an electromagnetic field into kinetic energy.


Dan Beeker

It will continue to consume that energy as long as it's present. If the pipe is open (the switch is turned off), the field will get to the end, and it will start to pile up, because it didn't know it wasn't supposed to go there, and it can't go anywhere. It will finally, at some point, reach equilibrium, and all the energy will be stable.

When the switch turns off, the energy behind the switch will no longer move. The energy in the new pipe will continue to behave according to what it's being told at the other end. It will be consumed. It will be transmitted to another space, or it will stop moving. That basic approach is what I wanted everyone to understand.

From that perspective you can really start to make good decisions on doing your PC board design. It's really simple. The behaviors are predictable, once you understand that the energy is in a space, not in a wire. If the energy flowed through wires, there would be no such thing as radio because there are no wires connecting you to the radio station. That was the foundation of my talk.

Why do PCB design engineers tend to focus so much on circuit theory and less on field theory?

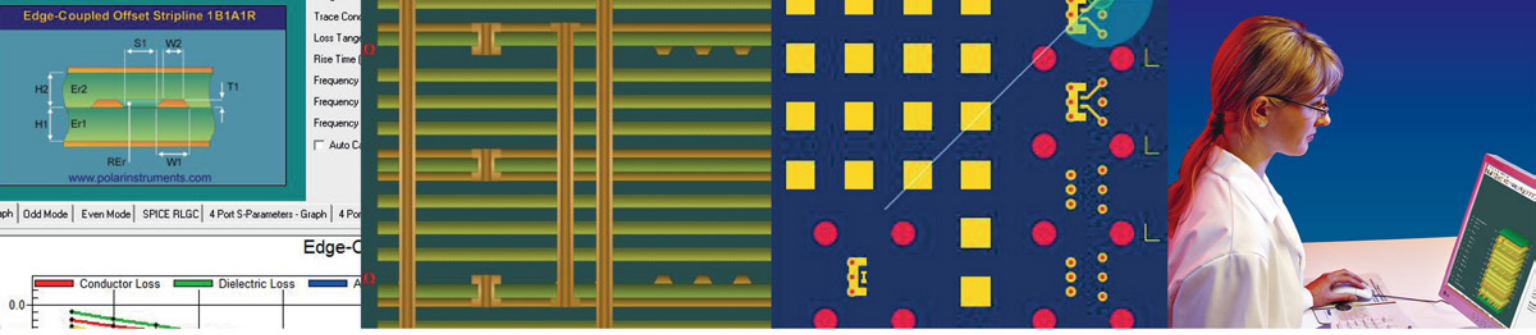
I have no idea. For some unknown reasons, the entire electronics industry has embraced the concept that when you put this energy on a printed circuit board, it suddenly changes from an electromagnetic field, which travels at the speed of light, to electrons traveling in wires, even though electrons have mass and can't travel at the speed of light. We have proof every day that this is wrong, but we firmly believe it. I would have fought to the death to defend that perspective if Rick Hartley hadn't corrupted me and shown me the evil of my ways.

Rick corrupted and corrected you.

Yes, he corrected me. That's the challenge facing the industry right now: We're still focusing on circuit theory, which really isn't about electromagnetic field energy, when what we're trying to do is build systems that generate, control, and consume electromagnetic fields. That's our challenge. We're still not connecting those dots at the university level. Are they not teaching electromagnetic theory or are they just not teaching it the right way?

Current is electromagnetic field moving in a dielectric. An ampere is one coulomb per second passing through a space. It's like gallons per minute in a water hose. It's not a measure of how many electrons are running past, and the current doesn't go back to where it came from. There is no return current. The electromagnetic field goes from where it was to where it has to go based on the nature of the plumbing that it's connected to. As a result, our job is to figure out where we want it to go and make a structure that the energy will follow. It will follow the path that's made up from power supply or signal conductor, dielectric, and ground conductor, which people call a return.

That flow of energy, from the source to the load, has to be through a completely intact pipeline. When all the switches are closed, you need to look from the load back to the power supply and see a dielectric that's bounded on both sides to provide the intact transmission line for the field energy to move through. If it's not intact, there will be discontinuities that



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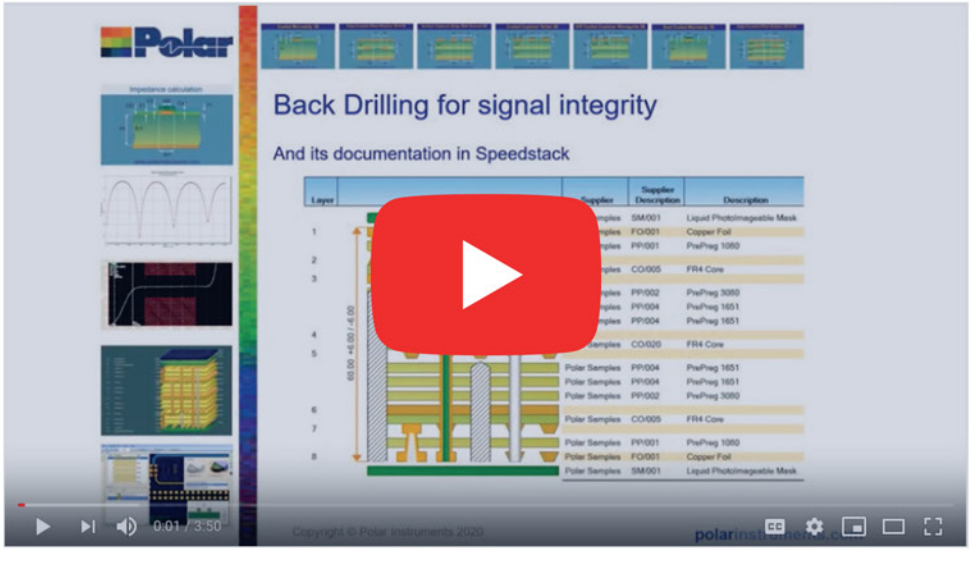

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"When I design a system, it works."

will cause it to take longer for the field to travel. Because it has larger spaces, it takes more time to fill those spaces up, and there are usually other signals that will be in those spaces, and they'll all contaminate each other. There will be interference with other signals.

You said that when you were younger, you focused mainly on the circuit and not on the field, yet you still managed to get designs right. What changed?

Years ago, when the rise and fall times were not too steep, you could get away with that approach, but now you can't. We used IC technology that allowed us to do stupid things that didn't make it break. The main focus was always, "Does it work?" not "Is that the right thing?" What didn't make it break became the rules that we designed for.

As we changed the technologies of the circuits, the switching speeds got faster and energy levels got higher, we didn't change the rules, and we started seeing a gradual increase in failures as this new technology permeated the products that we've designed. Now, you don't have any choice, especially with PCIE and all the other fast buses switching at 60 or 70 picoseconds. At this level, you can't screw around. I'm working right now on processors that have 5 nanometer geometries. So, the energies on these devices are switching in hundreds of femtoseconds. We have a part right now that has 40 watts on the core supply. There's a huge amount of energy that you have to deliver and because of the geometry of the transistors, it has to be really close.

How close can you put those capacitors? Are they on the bottom of the board? That's a 20 picosecond round trip. Is that close enough? Do I have to put capacitors on the top of the board where I've got a 2 picosecond round trip? Those are starting to be decisions that must be made. I'm working on a few products where I've had to put the capacitors directly between the balls. I put 01005 caps between the ball sites for the power supplies, because of the nature of my structure. By the time I get to the capacitors on the bottom of the board through multiple connectors, I'm 40 or 50 picoseconds away. People want to put a 4-ohm load on a 16-ohm driver and it's trying to deliver four times more power than it's rated for. That means it's going to heat up 4x or more than it's supposed to, and it's going to let the smoke out.

What advice would you give to designers who have been primarily educated to focus on circuit theory? What do they need to understand?

The first thing is to repeatedly listen to my song "All About The Space" so that earworm gets stuck in your head. That was a fun song (sung by Dan's daughter to the tune of "All About That Bass"). It's not complicated. Sunlight, which is electromagnetic energy, comes from the sun. None of that is being delivered by wires. It's not electrons that are carrying energy on a printed circuit board. It's the same energy. Therefore, it's still electromagnetic field and it travels in the dielectric.

Is there electron movement? Certainly. The poor electrons are being kicked around by the evil field. There is some movement of electrons, often described as electron drift, but they move at a relatively slow velocity, because electrons have mass. Don't focus so much on the electrons. It's all about the space. There's a lot of information out on the web. The bottom line is this: When I design a system, it works. It's not that I'm super smart. It's because the rules are so simple. When you follow them, the results are predictable. It will work.

Good stuff. Thank you very much for your time.

Always a pleasure, Andy. **DESIGN007**

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Integrated Passive Devices: Design Solutions With Many Benefits

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Many good ideas have often escaped broader appreciation in the electronics industry. Some have come in and out of favor over time, including the integrated passive device (IPD).

The first IPDs appeared in the late 1980s and early '90s, driven by a desire to miniaturize electronics while decreasing cost and increasing performance. Those drivers remain key today. Just like an IC package, engineers integrate resistors, capacitors, inductors, etc., into a packaged device, and then mount and interconnect them to a printed circuit board. This can significantly reduce the number of discrete components that might otherwise be required for an assembly design, and using an IPD can simplify PCB assembly processes and lower assembly and final product costs.

This IC-like manufacturing process would involve depositing thin layers of resistive, dielectric, and conductive materials onto a suitable substrate (often silicon, glass, or ceramic) using physical vapor deposition (PVD) or chemical vapor deposition (CVD). However, it is also possible to assemble an IPD discrete device using a traditional SMT process and solder to mount the resistors, capacitors, and inductors to a small PCB or ceramic circuit that has terminations at designated locations (Figure 1).

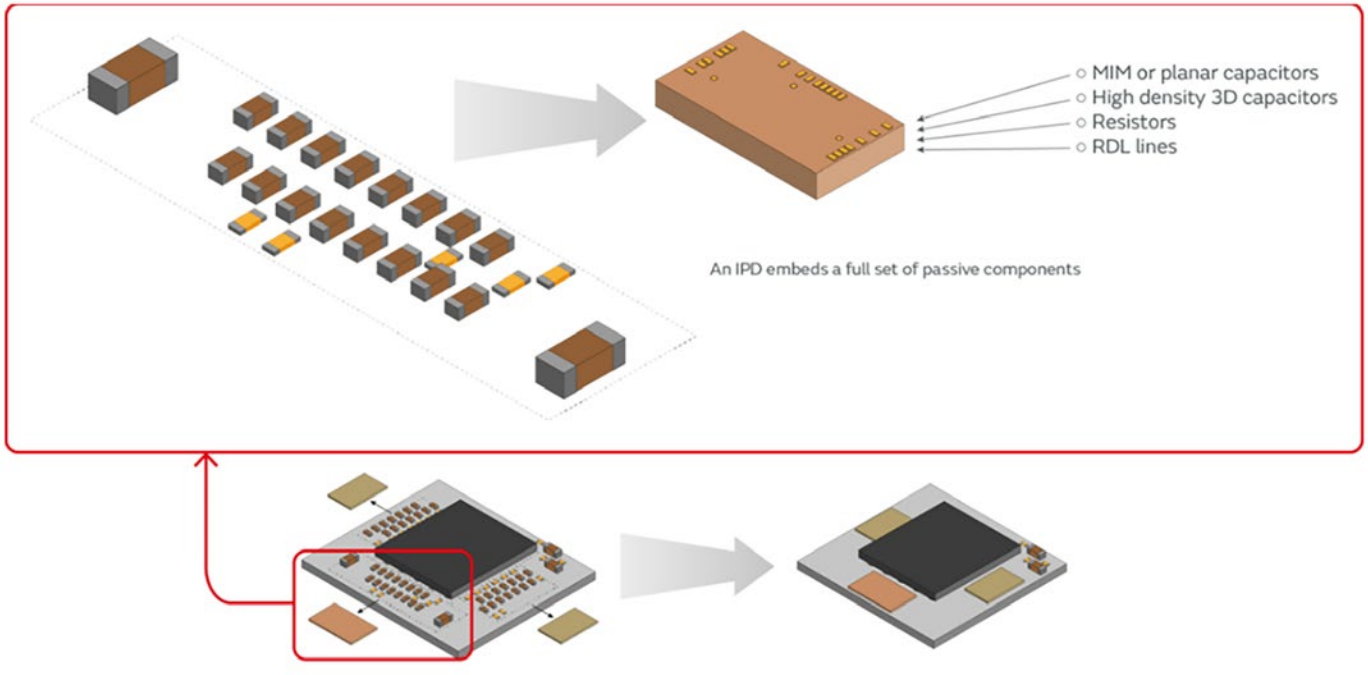

Figure 1: An IPD (integrated passive device) can integrate numerous discrete devices into a single package, thereby reducing the number of components that would otherwise require individual handling, validation, and assembly. (Source: Murata)

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Other benefits of IPDs include:

- **Miniaturization:** To shrink the size of products, designers have occasionally used IPDs to save space on printed circuit boards to replace myriad discrete passive devices.
- **Performance improvement:** Integration of passives into packages can reduce the parasitic effects that often occur in some designs and can lead to better electrical assembly performance.
- **Enhanced reliability:** The integrated passive component can be manufactured and assembled using fewer solder joints and interconnections, resulting in more reliable electronic designs. (This is something that has not gone unnoticed by me and is now considered an opportunity for exploration using the Occam Process for their manufacture.)

With the benefits just accounted for, it should not be too surprising that integrated passive devices have found some reasonably broad acceptance. For example, when one attempts to establish where IPDs have found greatest acceptance, it's almost everywhere. Today, IPDs are widely used in various applications, including RF modules, wireless communication devices, medical devices, automotive electronics, and consumer electronics. One highlightable benefit of IPDs is their ability to enhance performance while saving space, making them suitable for high-frequency and high-performance application. However, in broad brushstrokes, the following are a few more specific places where they have provided benefits.

In consumer electronics, such as smartphones, tablets, and wearables, the adoption of IPDs has reportedly been quite high due to the stringent space and performance requirements as discussed earlier. One estimate has it that perhaps 70% of modern consumer electronic designs in recent years have incorporated some form of IPD.

As new cars continue to consume evermore electronics, the automotive industry has demonstrated significant interest in the adoption of IPDs, particularly in advanced driver-assistance systems, infotainment systems, and power management modules to name just a few. Estimates of adoption rates in automotive are similar to that of consumer electronics. In telecommunications equipment, especially for RF and high-frequency applications (think 5G), IPDs are widely used to enhance performance and reliability. With a solid foothold, it is likely they will continue their march into coming generations of products. The same holds true for medical and industrial products, and the list goes on.

When it comes to suppliers, a long list includes familiar names such as Vishay, AVX, Murata, Texas Instruments, Johanson Technology, OnChip Devices, and STMicroelectronics. They offer a wide range of passive electronic components, including resistors, capacitors, inductors, and integrated passive components, with off-the-shelf and custom solutions to meet specific design needs.

Integrated passive devices offer designers an opportunity to significantly reduce their designs' complexity while improving performance and reliability. I encourage you to learn more about them. **DESIGN007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."

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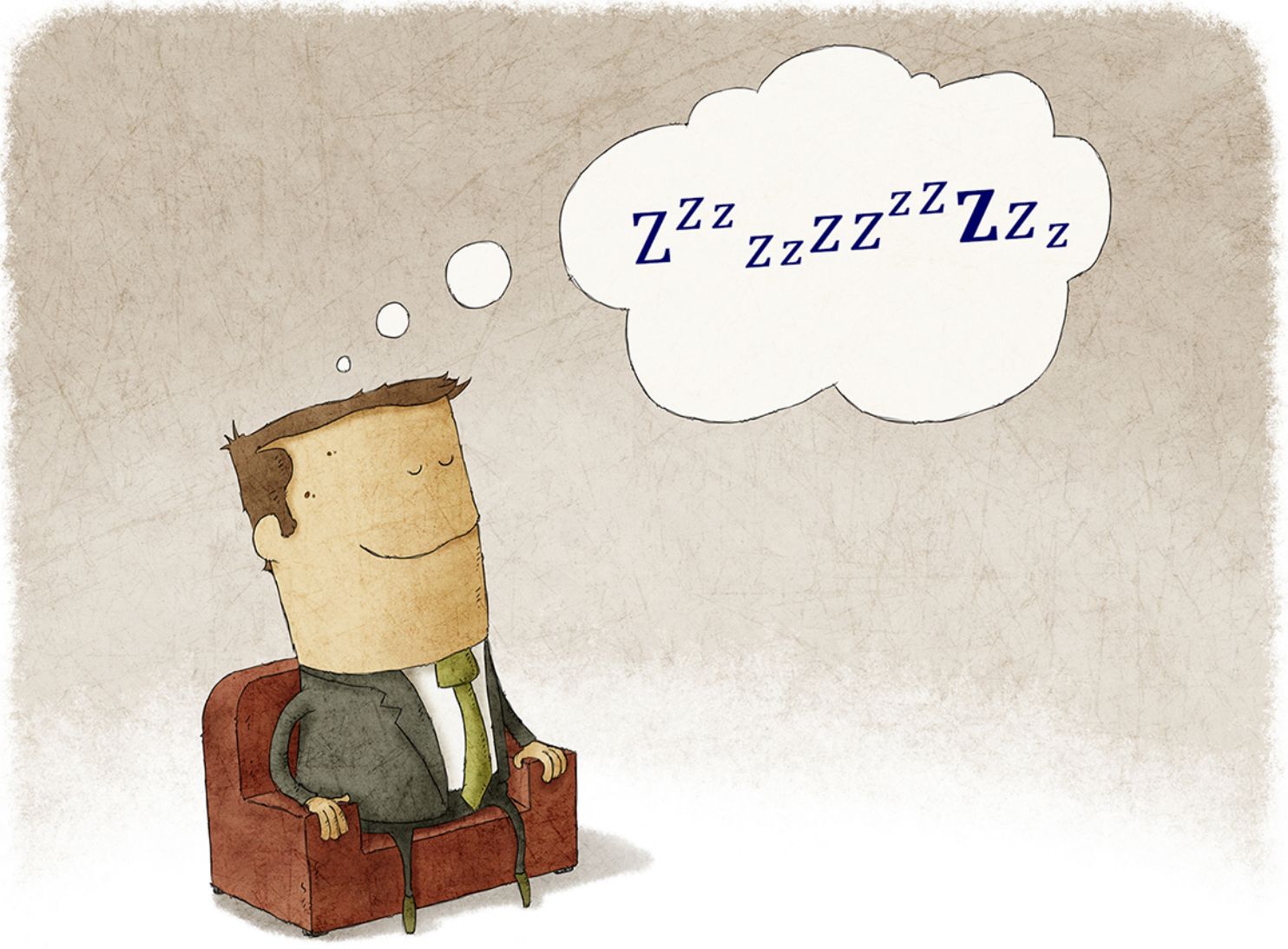

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UHDI FUNDAMENTALS:

UHDI Applications for Aerospace

Article by Anaya Vardya
AMERICAN STANDARD CIRCUITS

Ultra high density interconnect (UHDI) technology refers to advanced manufacturing processes used to create extremely compact and highly efficient electronic circuits at the sub-1-mil line and space level. In aerospace applications, UHDI is crucial due to the stringent requirements for weight, reliability, and performance in a challenging environment. Here are some specific aerospace applications of UHDI:

1. **Avionics systems:** UHDI is used in avionics systems to create compact, lightweight, and reliable printed circuit boards. This includes flight control, navigation, communication, and monitoring systems.
2. **Satellite technology:** Satellites require highly reliable and compact electronic systems. UHDI technology is used to build these systems, ensuring they can withstand the harsh conditions of space.
3. **Unmanned aerial vehicles (UAVs):** UAVs, including drones, benefit from UHDI technology in their guidance, communication, and payload management systems, where space and weight savings are critical.
4. **Radar systems:** Radar systems used in both civilian and military aerospace applications require high-performance electronics. UHDI technology allows for creating complex radar systems with improved performance and reliability.
5. **Power management systems:** Efficient power management is crucial in aerospace

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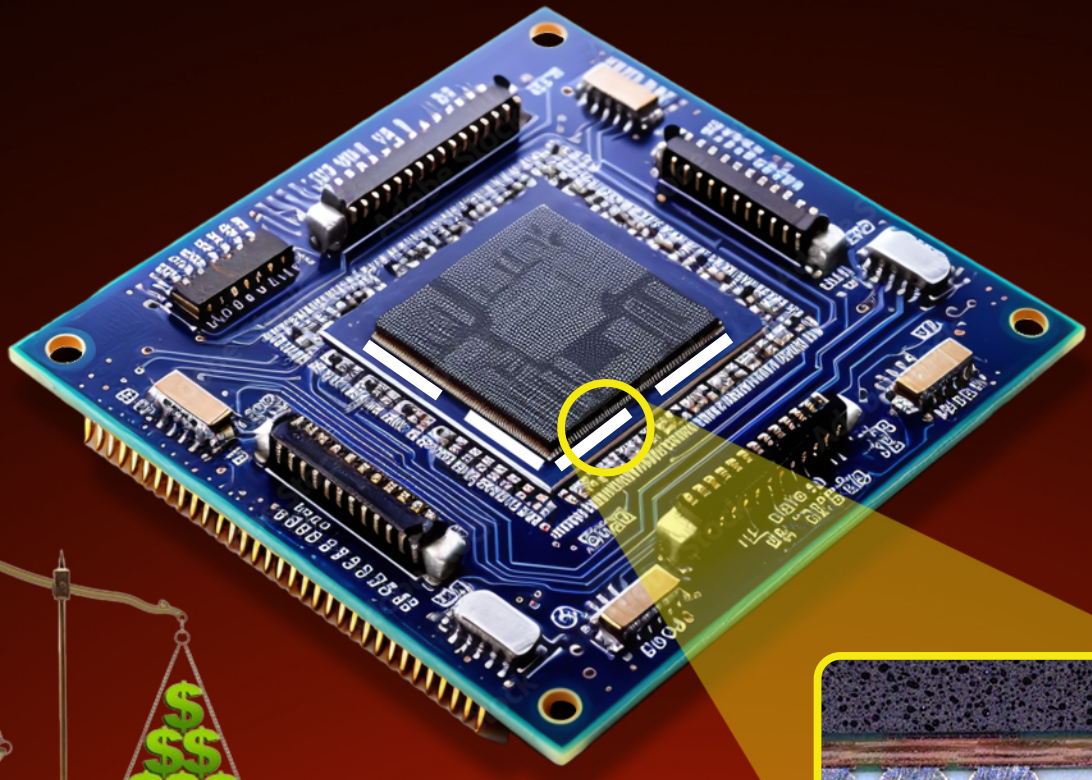

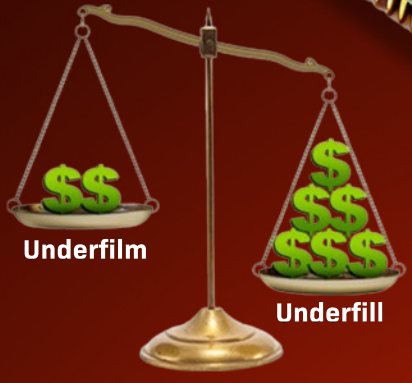

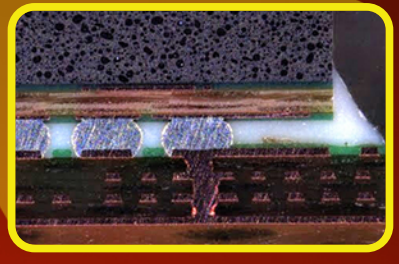

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applications. UHDI technology helps develop compact and efficient power management systems that can handle the high power demands of modern aircraft.

6. **In-flight entertainment and connectivity:** UHDI is used in the development of advanced in-flight entertainment and connectivity systems, which require high-density electronics to deliver robust performance while minimizing weight and space.
7. **Control systems:** Flight control and engine control systems use UHDI technology to integrate multiple functions into a compact space, enhancing performance and reliability.
8. **Environmental control systems:** These systems, which manage temperature, pressure, and air quality in aircraft, benefit from the compact and reliable nature of UHDI technology.
9. **Missile and defense systems:** In military applications, UHDI technology is used in missile guidance and defense systems where high performance and reliability in extreme conditions are essential.

The implementation of UHDI technology in aerospace ensures that electronic systems are as efficient, lightweight, and reliable as possible, meeting the increasingly rigorous demands of the industry. **DESIGN007**

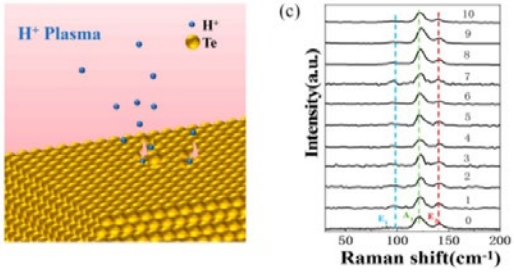
Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals.* He is the author of *Thermal Management: A Fabricator's Perspective* and *The Companion Guide to Flex and Rigid-Flex Fundamentals.* Visit I-007eBooks.com to download these and other free, educational titles.

Plasma Irradiation Transforms Tellurium's Electronic Properties

A breakthrough study by researchers from Changchun Institute of Optics, Fine Mechanics and Physics, and Chongqing University has revealed a novel method to manipulate the electronic properties of tellurium crystals using plasma irradiation.

Tellurium, a chemical element with unique electronic characteristics, has long fascinated scientists for its potential applications in electronics and optoelectronics. However, methods to effectively modify its electronic properties have been limited. In this research, published in the journal Nanomaterials, the team explored the effects of plasma irradiation on tellurium crystals.

By exposing tellurium crystals to plasma irradiation, the researchers observed significant changes in the material's electronic properties. This non-intrusive technique allowed for precise control over the modification process, opening up new possibilities for the design of advanced devices.



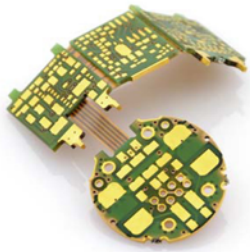
The study found that plasma irradiation effectively modified the surface of the tellurium crystals, leading to changes in their band structure and conductivity. These alterations have the potential to enhance the performance of tellurium-based devices in areas such as photovoltaics, sensors, and optoelectronic switches.

The significance of this research lies in its potential to revolutionize the way we manipulate materials for technological applications. By understanding how plasma irradiation can modify the electronic properties of tellurium, scientists can now design and fabricate devices with enhanced performance and novel functionalities.

This breakthrough demonstrates the power of plasma technology in materials science and engineering. As the research continues, it is expected that new avenues for the development of advanced technologies will be unlocked.

(Source: Changchun Institute of Optics, Fine Mechanics and Physics)

Focused on Flex



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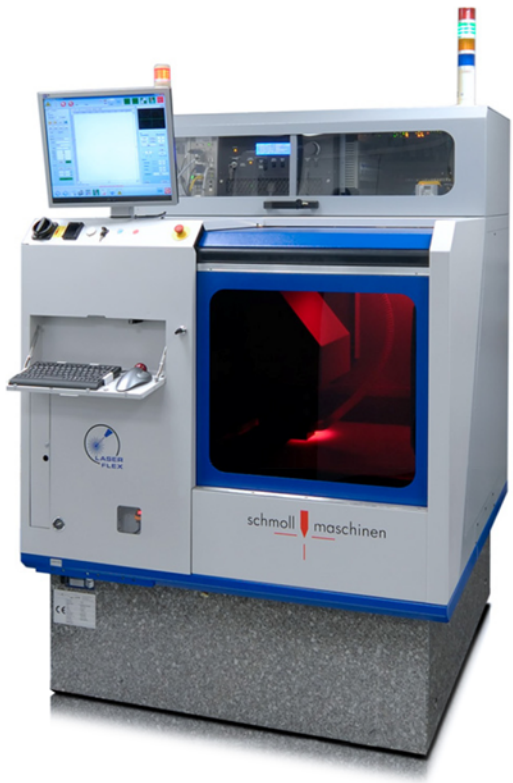

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Designing for Reality: Electroless Copper

Connect the Dots

by Matt Stevenson, ASC SUNSTONE CIRCUITS

Roll up your sleeves because it's time to get messy. In a recent episode of I-Connect007's On the Line with... podcast, we discussed electroless copper deposition. This process deposits a copper layer into the through-holes and vias of what will eventually be a PCB.

Electroless copper deposition feels like a black box to many people. It sort of looks like a black box, too. The boards go in one side, come out the other, and emerge differently. So, let's crack open that black box and look inside.

This manufacturing step involves a chemical deposition of copper. Specifically, it is a chemical-catalyzed deposition of copper, mainly to the epoxy inside the holes. Electroless differs from electrolytic in that electrolytic deposition relies on electricity. However, there is too much insulating material in the different layers of the PCB for electrolytic processes to work in through-holes.

Without electroless copper deposition, boards later end up with voided copper holes in the manufacturing process. Understandably, this preparatory step is critical for the manufacturer to get right. When done correctly, it creates a very fine layer of copper that makes the connection from top to bottom through the through-hole. Since this thin layer of copper is conductive, it allows a later electrolytic process to deposit a more thorough layer of copper.

Preparing for Electroless Copper

This step isn't simply spraying a bit of copper in the holes. It is a multi-chemical process that involves many chemical baths, rinses, and other processes. To prepare for this step, the manufacturer first needs to clean up the residue left behind by the drilling process.

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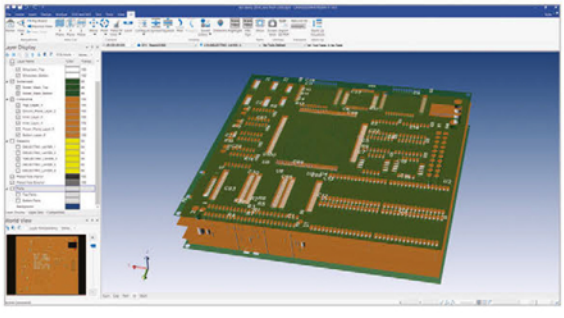

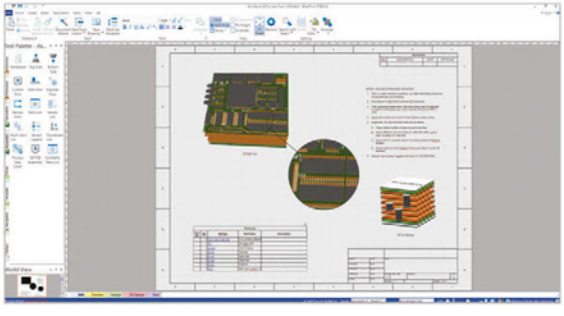

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The challenge is that drilling creates heat. This tends to melt and possibly smear epoxy over the internal copper connections of the circuit board. Smeared epoxy creates a possible insulator between copper connections and the through-hole, eliminating or making an unreliable connection. The manufacturer needs to remove these smears chemically. It's called the de-smear process. This results in a uniform, clean surface—perfect for the application of electroless copper.

Next, we remove other remnants from the drill process. The drill can sometimes produce copper burs on the surface, like when drilling through a 2×4. Any bumps or protrusions need to be removed. Maintaining the smooth surface plane throughout this process is crucial. We use a mechanical scrub to remove these irregularities on the surface created by the drilling process.

Designers may have concerns about rough surfaces left by this step, primarily because the scrub uses a nylon brush to roughen both sides of the panel surface. Copper is porous but very smooth. It needs to be roughened to get good adhesion during the dry film lamination process. Copper roughening is a great equalizer to keep the adhesion of the dry film photoresist during the plating processes.

Time for Electroless

After being de-smeared, smoothed, and roughened, the boards go into the baskets that enter the electroless copper process. They first go into a chemical bath to help slightly swell the epoxy. As it swells, it becomes more porous, allowing the copper and catalyst to enter. When the swelling decreases, it has a more uniform copper coverage.

The catalyst is a palladium-based process. Palladium is not cheap, but it works very well. A catalyst initiates a reaction but is not consumed. The catalyst gets into all the through-holes and deposits in the epoxy. Later, the palladium will attract the copper ions in the electroless copper bath and act as a nucleation site for a reaction to occur. The copper bonds to the palladium, creating a copper layer about 30 to 70 micro-inches thick.

> "Heat tends to melt and possibly smear epoxy over the internal copper connections of the circuit board."

Two forces act against the copper plating. First, all the air needs to be removed from the through-holes. Manufacturers use mechanical processes such as vibration, thumping, and agitation to increase the fluid flow through the holes and move the air out. There are other tricks to help break the surface tension and increase the opportunity for getting copper in all those holes. If you fail to get copper in every hole, it creates a void, which may lead to a missed connection later, which means a scrapped panel.

Another potential challenge to the electroless copper process is in the aspect ratio—the thickness of the panel to the smallest drill size. For example, a 100-mil thick panel with a 10-mil drill creates a 10:1 aspect ratio. This is common and shouldn't challenge too many manufacturers. But as you get thicker panels and smaller holes together, the increased aspect ratio becomes more problematic. Eventually, manufacturers must rely on capillary action to get fluid in and out of the holes.

However, capillary action won't be enough. Once you place the solution in the hole, you need to continually replace it to ensure enough

copper is in contact with the catalyst. Getting the hole wet once is good, but you need to replenish that action. Mechanical processes are used to get fluid through the holes numerous times to produce a thick enough coating.

The copper needs to be thick enough to survive the pre-clean processes and the initial dunking of panels into a sulfuric acid bath, which happens later in the manufacturing process. Portions of the pre-clean process will etch copper away if uninhibited. Enough copper must remain after those processes to ensure adequate electrical conduction for electroplating.

Electroless Copper Design Considerations

If the electroless copper deposit goes wrong, voids in through-holes could cause manufactured PCBs to end up in the scrap heap. Luckily, designers can consider this possibility when designing for the reality of manufacturing. To avoid problems during this process, use the largest vias possible. While there are sometimes good reasons to use micro-vias and high aspect ratio holes, aim for a 10:1 aspect ratio or smaller. The smaller the aspect ratio, the better the chances the boards will be reliable long-term and properly yielded to minimize costs.

To learn more about designing for the reality of the PCB manufacturing process, check out more episodes of On the Line with.... DESIGN007

Matt Stevenson is vice president and general manager of ASC Sunstone Circuits. To read past columns, click here. Download Matt's book, *The Printed Circuit Designer's Guide to... Designing for Reality* and listen to the podcast here.

Creating Artificial 'Muscles' for Safer, Softer Robots

Northwestern University engineers have developed a new soft, flexible device that makes robots move by expanding and contracting—just like a human muscle.

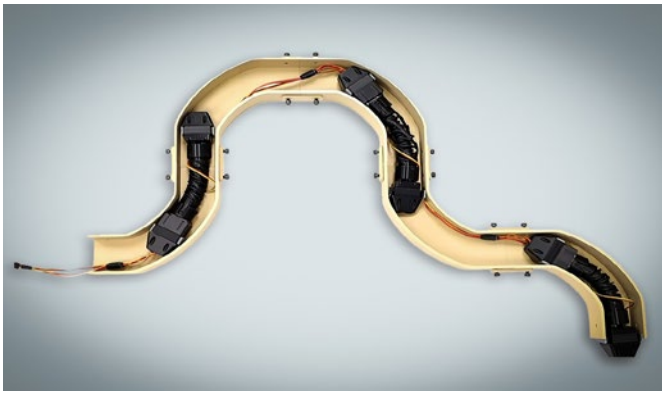
To demonstrate their new device, called an actuator, the researchers used it to create a cylindrical, worm-like soft robot and an artificial bicep. In experiments, the cylindrical soft robot navigated the tight, hairpin curves of a narrow pipe-like environment, and the bicep was able to lift a 500-gram weight 5,000 times in a row without failing.

Because the researchers 3D-printed the body of the soft actuator using a common rubber, the resulting robots cost about $3 in materials, excluding the small motor that drives the actuator's shape change. That sharply contrasts typical stiff, rigid actuators used in robotics, which often cost hundreds to thousands of dollars.

"Roboticists have been motivated by a long-standing goal to make robots safer," said Northwestern's Ryan Truby, who led the study. "If a soft robot hit a person, it would not hurt nearly as much as getting hit with a rigid, hard robot."

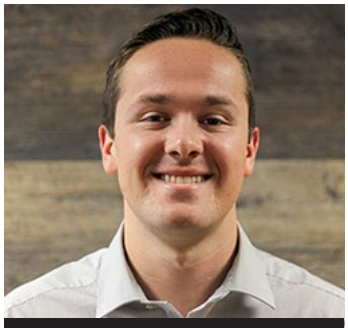
Taekyoung Kim, a postdoctoral scholar in Truby's lab and first author on the paper, led the research. Pranav Kaarthik, a Ph.D. candidate in mechanical engineering, also contributed to the work.

(Source: Northwestern University)



TOP TEN

EDITOR'S PICKS

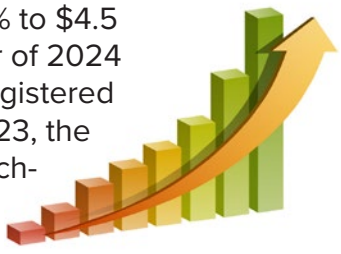


Jake Whipple

Evolution of a Career in Tech

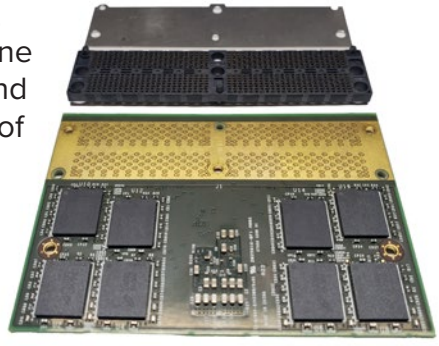
About five years ago, Sunstone Circuits partnered with George Fox University, both based in Oregon. Nolan Johnson worked for Sunstone at the time and helped several students with their capstone projects. We recently met with two of those young professionals, now five years past graduation, to see how their career trajectories have played out. What do they think about working in the industry?

Electronic System Design Industry Posts $4.5 Billion in Revenue in Q1 2024



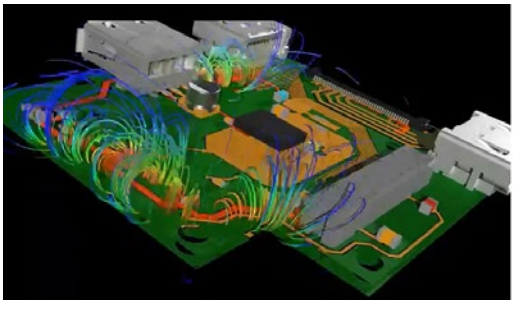
Electronic System Design (ESD) industry revenue increased 14.4% to $4.5 billion in the first quarter of 2024 from the $3.95 billion registered in the first quarter of 2023, the ESD Alliance, a SEMI Technology Community, announced in its latest Electronic Design Market Data (EDMD) report. The four-quarter moving average, which compares the most recent four quarters to the prior four, rose 14.8%.

McCauley Design Group Spreads the CAMM2 Gospel



At PCB East, I met Charlene McCauley and Terrie Duffy of the McCauley Design Group. The duo was leading a class on designing with the new CAMM2 DDR5, a JEDEC specification and standard created by Dell, which is due to replace the aging SO-DIMM in laptops.

Beyond Design: Does Current Deliver the Energy in a Circuit?



The flow of current in a PCB is essential for delivering energy and enabling devices to perform work but does current carry the energy? Why does an alternating current (AC) signal require a thicker conductor to provide higher power if the current is not in the carrier? There are many contradictions as to how energy flows in a circuit. To understand this, one must appreciate the difference between the lumped element view and that of distributed circuits.

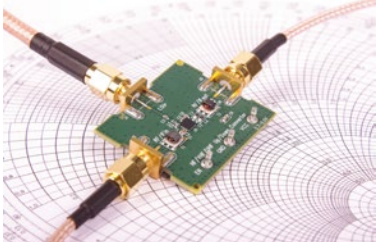
Cadence Reports Q2 2024 Financial Results

"I am pleased with our strong Q2 results. We exceeded our outlook on all key financial metrics, closing Q2 with backlog of approximately $6 billion," said John Wall, senior vice president and chief financial officer. "A good finish to the first half of the year, combined with ongoing demand for our solutions, sets us up for strong growth in the second half of 2024."

Exploring the Interdisciplinary World of Mechatronics

Dylan Nguyen has been exploring his engineering interests through FIRST Robotics programs. We talk to Dylan about his interests and experiences in his engineering studies and how, this exposure has opened his eyes to the possibilities of becoming a PCB designer.

UHDI Fundamentals: UHDI for RF Microwave Applications



Ultra high-density interconnect (UHDI) technology has significant potential for RF (radio frequency) microwave applications. Its advantages lie in its ability to provide high-density routing and integration, which are crucial for complex RF circuits. Here are three key UHDI benefits in RF microwave applications.

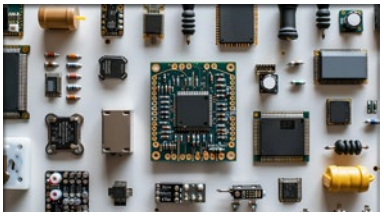
Ultra Librarian, Footprintku AI Partner to Bring DFM to the EDA CAD Library

Ultra Librarian, an Accelerated Designs brand and the world's largest online CAD library with over 16 million parts and counting, is pleased to announce a strategic partnership with Footprintku AI, the leader in DFM-aware CAD library development. This partnership aims to solve one of the largest manufacturing issues plaguing hardware design teams today, CAD library DFM.

A Great Recipe: Collaboration, Motivation, and Design Classes

John Watson, CID, is a professor at Palomar College near San Diego. John teaches a basic PCB design class and an advanced class, and graduates from these classes are ready for their first PCB design job. These appear to be the only classes of their kind in the U.S., and as more designers retire, the demand for classes like this will continue to rise.

Do You Collaborate With Your Component Supplier?



Mention the word "collaboration" to a group of designers, and a few of them might acknowledge working closely with their fab and assembly partners. But how many designers consider their component providers to be true stakeholders in the process and collaborate with them regularly?

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- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
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We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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Career Opportunities

MivaTek Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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