DECEMBER 2023

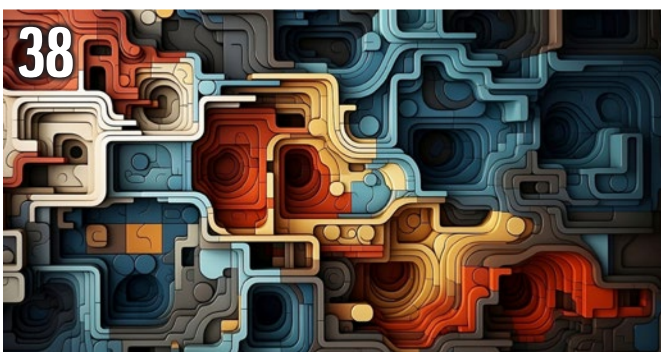
I-Connect007

DESIGN007 MAGAZINE

DESIGN007 MAGAZINE

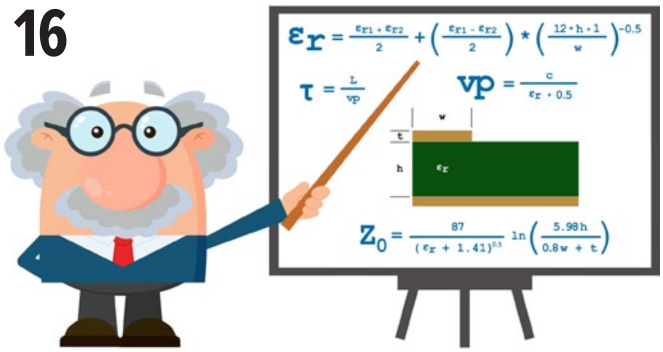
Designing Non-standard Board Shapes

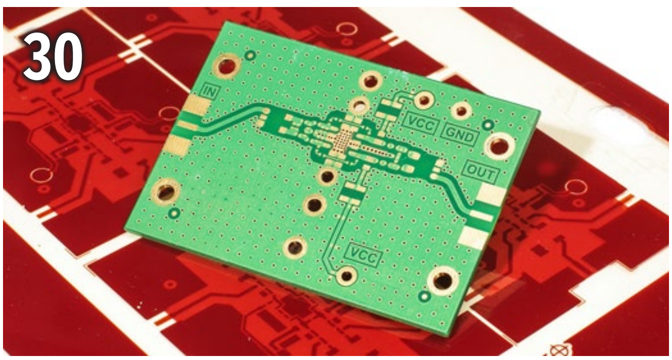
In this issue, we will discuss some of the challenges, pitfalls and mitigations to consider when designing non-standard board geometries. We will share strategies for designing odd-shaped PCBs, including manufacturing trade-offs and considerations required for different segments and perspectives.

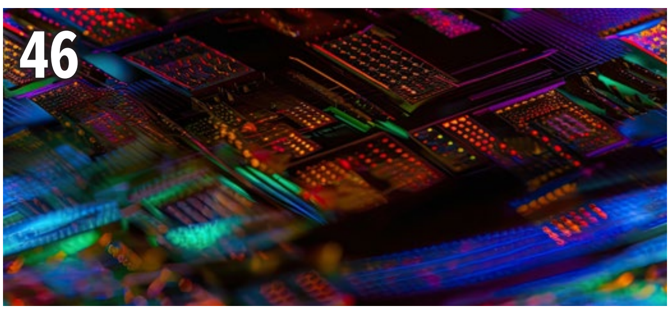


DESIGN007 MAGAZINE

16







COLUMNS

ARTICLES

HIGHLIGHTS

DEPARTMENTS

Trace Oddity

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Remember when PCBs were all shaped like squares and rectangles? Things were so much simpler in the olden days.

Now boards are designed, fabricated and assembled in all shapes, including stars, human hands, octopuses, triangles, and cursive signatures, just to name a few. The wearables and automotive segments are driving the development of PCBs in odd shapes. And there are plenty of circular PCBs being designed for use in products that can reach out and touch bad actors in another part of the world.

Unconventionally shaped circuit boards bring with them a variety of potential missteps, mistakes, and miscues. Signal integrity and EMI can be big issues; strange geometries hamper a designer's ability to lay out matched impedance traces. Understanding manufacturing and environmental tolerances is paramount.

There are also dozens of DFM, DFA, and DFT challenges with oddly shaped boards. Placing components on round boards or boards with a rounded side is a tricky matter,

because some parts must be rotated at crazy angles to follow the curve of the PCB's edge. Most autorouters are not optimized for routing parts at angles other than 90 or 45 degrees. Acute angles are more likely to lead to acid traps when a traditional router encounters pads that are not in the standard orthogonal shape. Odd-shaped boards also pose panelization and depanelization issues.

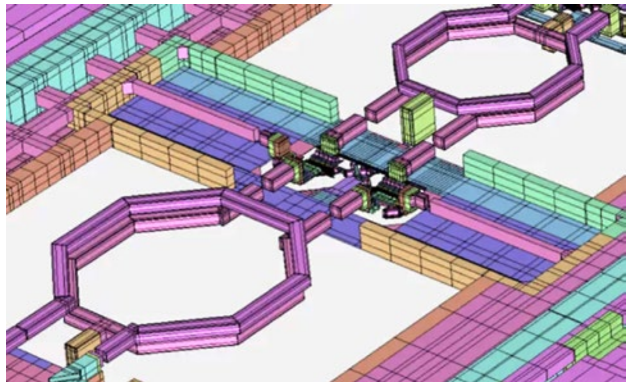
Designing boards in crazy shapes often requires PCB designers to import data from an MCAD tool into their ECAD tools. If you've been designing with 2D ECAD tools for decades, you might have to learn how to work with 3D MCAD tools, which are integrated with most EDA tools.

In this issue, we will discuss some of the challenges, pitfalls, and mitigations to consider when designing non-standard board geometries. We will share strategies for designing odd-shaped PCBs, including manufacturing trade-offs and considerations required for different segments and perspectives.

First, Kris Moyer and Kelly Dack provide an overall look at designing PCBs in unconventional shapes. Then Stephen Chavez explains how EDA tool companies approach the design of oddly shaped boards. John Watson points out the need for designers to focus on physics when designing non-standard boards, and Kelly Dack's column focuses on the need to understand dimensioning and tolerancing when working with offbeat board shapes. We also have columns from Matt Stevenson and Barry Olney, as well as articles by Anaya Vardya and Chris Keirstead.

It's been a busy year. I'll see you in 2024! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 23 years. To read past columns, click here.



Ansys RaptorX™ Certified by Samsung Foundry for High-Speed Design

Samsung Foundry certified Ansys RaptorX™ on-chip electromagnetic (EM) solution for analyzing high-speed products manufactured with Samsung's 8nm (nanometer) LN08LPP Low Power Plus silicon process. The silicon-validated accuracy of RaptorX enables joint customers to harness Samsung's manufacturing process capabilities to achieve greater product reliability and higher performance for 5G, WiFi, automotive, and HPC.

The requirement for EM modeling extends beyond niche applications as chip frequencies continue to increase. The semiconductor industry relies on Electronic Design Automation (EDA) tool certification by foundries as a critical step to ensuring the accuracy and reliability of simulation models, which are essential for developing high-speed products. RaptorX's accuracy was validated across a multitude of demanding layout geometries, including dense dummy-metal fill, and its models correlated very well with silicon measurements. The ability to reliably predict circuit behavior allows designers to optimize their products with confidence knowing that they will behave as expected and meet performance specifications.

"Our customers are designing the next generation of technology products that rely on the higher frequencies made possible by Samsung's advances in manufacturing technology," said John Lee, vice president and general manager of the electronics, semiconductors, and optics business unit at Ansys. "The certification of RaptorX guarantees the required level of accuracy is achieved to ensure that data-intense products meet specifications at all levels." (Source: Ansys)

Unconventional Geometry Design Techniques

Feature Interview by the I-Connect007 Editorial Team

We survey our readers from time to time, and a number of respondents have mentioned that designing boards with odd geometries can be a real challenge. We asked design instructors Kris Moyer and Kelly Dack to discuss the challenges related to designing odd-shaped PCBs, as well as some solutions for designing today's boards that are anything but rectangles. What's the craziest-shaped board you've ever worked with?

Andy Shaughnessy: Kris and Kelly, thanks for joining us. Let's start with Kris. You talk about the challenges of designing odd-shaped geometries in your design classes. Tell me about those challenges.

Kris Moyer: One thing that comes to my mind regarding oddball geometries: To fit in all the parts, you have to learn how to place your parts at oddball rotations, not just 90 or 45 degrees. I don't want to give away any classified stuff, but I was working on the design of a circular board that goes in one direction really, really fast and doesn't come back, ever. The parts were laid out, and all the circuits were laid out like pizza wedges, radially out from the center. This board had very large stacked ceramic caps, the SMPS type, which ended up being over an inch long, but they needed to be normal to the radius—but not on a standard 90- or 45-degree radius angle—with all these different angles.

We had to start rotating the parts so they would follow the curve of the circular board around the diameter without hanging over. We had these parts placed at, say, 12.7 degrees and 33.9 degrees—all these weird angles and

rotations. But the pads were no longer where you could route cleanly into them at the 90- or 45-degrees with standard interactive routing or autorouting because we were doing all these oddball route angles.

Shaughnessy: Is this something you cover in your class?

Moyer: Here's something from my "PCB Design for Advanced Design Concepts" class. Imagine a circular board with a doughnut hole right where a rotary shaft has to go through the center, and all the parts are out from the center. Now, imagine trying to route using standard routing out from, say, the 3 o'clock position around. I don't know of any routers that will do a continuous sweeping arc. Yes, you can do 90- or 45-degree rounded corners with ECAD routers, but they're still trying to draw a straight line.

Kris Moyer

In a circular board, the better routing plan is to just do a continuous arc. I can get the router in 3D modeling tools to do this. But in ECAD tools, I can't say, "I want to start at this point, and I want to follow a continuous arc all the way around, get back into my part, moving from 3 o'clock counterclockwise around to 9 o'clock to make a connection there." Since it's a circular board with a doughnut hole, I can't just go to the center. That's another big challenge you will run into with offbeat shapes.

There's also still a population of board designers who don't know how to import IDF, DXF, or STEP geometries from an MCAD tool. They're used to going to their ECAD tool, drawing a rectangle, and making it their board. That's one of the big things right off the bat is to let the designers know this capability exists, and you might need to know how to import from an MCAD tool into your ECAD tool to set your geometry shapes. With most of our modern software tools, from the "Big Three" EDA companies at least, you can import the 3D STEP model directly and say, "Make that the shape of my board," without needing to go through the intermediary 2D formats of IDF and DXF. All my 3D work is in STEP and I don't have much need for IDF. But the entire design community should know how to work with these various importable MCAD geometries. Kelly, what are your thoughts on this?

Kelly Dack: This is a good discussion because we're coming from different ends of the industry. You're coming from the very complex aerospace and defense end of design, and I work with the very normal, producible volume types of products. I agree with your comments about how routing and component placement is affected by outline geometry, and the way it affects how we address everything within those outlines. I'm coming from the perspective of design for manufacturability because what you're talking about is getting all that copper topology to fit within an outline.

As Kris mentioned, many designers don't know how to import MCAD files. Could you use your ECAD software to replicate a geometric shape defined by your mechanical counterparts? Impossible. So, we have to rely on DXF, STEP, and IDF. Designers need to understand these other file formats, which are really languages.

How do we process board outlines that are even crazier than circular boards? I came from a gaming company that builds slot machines. I designed LED boards that would fit in these things called "toppers" that sit on top of the game, and the LEDs light up to attract people to the game. I've created boards that are in the shape of Batman. I also designed a board in the shape of Frank Sinatra's signature—a strip of cursive writing with LEDs all over the place. So, we can both agree that anything can be done from a board outline standpoint.

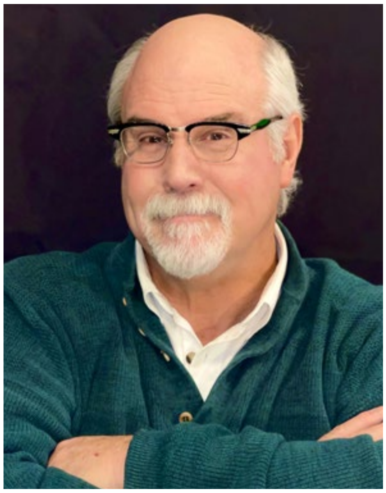
Now, how do we process that and incorporate DFM? There are other fabrication considerations such as excising, because every board, regardless of its shape, has to be nested inside a manufacturing panel for the bare board manufacturer. How do we break an unconventionally shaped board out of a panel?

Moyer: The other big one from a manufacturing point, especially with these smaller and smaller boards, is stackup. Too many engineers and designers now are just leaving a generic note saying, "Make my board out of FR-4," and not considering how fragile this stuff is, the Tg you need, the laminate thicknesses you want, and so on.

Back in the day, boards were 62- or 93-mils thick with four layers, and they were built like a Mack truck. But now we're trying to make Fitbit trackers and you have 20 layers of board in something that's 30-mils thick. It's as thin as paper, flexible, and fragile. There are definitely manufacturing challenges there.

We have to remember one other thing too. Nowadays, the boards are getting so small, with some of these oddball jumpers (like in the wearables market), that you have to assemble them in a pallet array. It means that now die-cutting a bare board out of a panel could change. How do you manage to die cut so it goes around all these components soldered onto the board and not damage them?

Dack: Have you ever rolled out cookies at Christmas? It's like a cookie cutter. You have the sheet of cookie dough and stamp the cutter through. But on an assembled board, you have all the components on there. If I have a big LCD module on my board and I bring a big steel die cutter down, I now have a mechanical interference, and potential damage to my components.


Kelly Dack

Moyer: Typically, good board designers will design the break-off rail or the panel ahead of time in the capital before it ever goes to the fabricator or the assembler. Sometimes if it's still just a small board, you can put a note in that says, "I want this in a 4"x4" assembly pallet array in the panel. The fabricator will stamp out the array for the assembler and then have the appropriate break-off or removal material that the assembler can remove the individual boards from.

It's a designer's job to know where their stuff is going. I tell all my students that if your company is sending the board to an assembly company and letting them subcontract the fabrication, they should say, "That's fine. I still want to know which specific fab company you're using, and I want to know what the panel looks like."

Dack: Kris, I love your fortitude, and I totally agree that's what we should do. However, the feedback is not working for you because nobody knows where their boards will be built. I deal with designers, and it's a hot-button around here. I'm dealing with 20 designs a week, and you would think that the PCB designer didn't know much about anything.

Moyer: I'm changing that with my classes (laughs).

Dack: Telling designers that they must have information about where their designs will be manufactured is a noble concept. But I think we've established from speaking with PCB designers, for the time being, that they usually have no clue. Nobody's telling them, because it's a dynamic situation based on quoting, that your boards can go to India based on one set of pricing, and then suddenly they're in Asia for another set—just because they want to save five cents on a board. Again, it's back to this volume thing.

I do hear what you're saying, and I agree with it. I just don't know if it's valid from a practical standpoint. This leads us back to unconventional board outlines. How do we make these odd board outlines manufacturable, especially if we don't know where our designs are headed? How do we incorporate DFM into board elements?

Shaughnessy: It sounds like unconventionally shaped boards bring their share of DFM and DFA issues.

Moyer: Yes, and design for test (DFT). With a standard rectangular board, you can get all your probes in there, and your flying probe tester is no problem. But how do you test for a one-off board? How do you get a one-off, weird-shaped board into a flying probe tester to do your post-assembly test? You have to say, "Hey, assembly house, don't pull this thing out of the break-off rails until you've completed testing."

Dack: SMTA publishes its TMAG specification on testing, which is widely used and recognized as the definitive explanation. I called SMTA and purchased the TMAG specification, and I've done a presentation on it. This is what many companies are using to design test fixtures to the correct criteria. With a complex shape or geometry, now you have an in-circuit test problem and you have to deal with it a different way.

Moyer: That's right. There is another point I'd like to make. As we move toward 3D-printed board structures, there are huge challenges for the designers because now they have to start thinking like 3D mechanical engineers. It's no longer the same process technologies. It's no longer drill and plate; it's literally composite metal as you're building up. I no longer need a vertical plated through-hole structure. I can have my plated structure from layer one to layer two, just be printed at 9.7 degrees, if that's the angle I want for this weird 3D structure.

Dack: I agree. Design is where it all starts. Kris, we've been talking about CAD data, and generally speaking, CAD data is nominal data. One of my pet peeves is that board designers need to consider tolerancing. What do you think about that? What's your take on the importance of understanding tolerancing on these processes?

Moyer: Understanding those tolerances is essential, especially with these oddball shapes, because a lot of these oddball shapes are going into consumer goods such as gloves or things like that. It's not just fabrication tolerances that must be considered, but environmental tolerance as well. You must understand both your expectation as a designer and your fabricator's capabilities. Talk to your fabricator early and often, as well as your assembler, to make sure you understand their properties.

Here's an example I use in my military design class. You have a board that must fit into an extruded aluminum housing and it's designed for a board that is 39 mm wide by 1.6 mm thick. But if you make that board exactly 39 millimeters wide, and then you expose it to extended operating temperature ranges like the military sees, the board will expand faster than the aluminum, get wedged in, warped, and mucked up in there. Designers need to understand not just the fabricator's capabilities, but what your tolerances are, then consider the environment where you expect your board to be. Is it something that's kept in your home in a controlled environment of 50-80°F? Or will it be for a military product placed in -55°–+105°F? If it's going into outer space, what are the requirements, and what effects do those environments have on the geometries and tolerances and physics of your board?

Shaughnessy: Good stuff. Thanks, Kris and Kelly, for this conversation.

Dack: Thanks, Andy. DESIGN007

Controlled Impedance and Calculations for Microstrip Structures

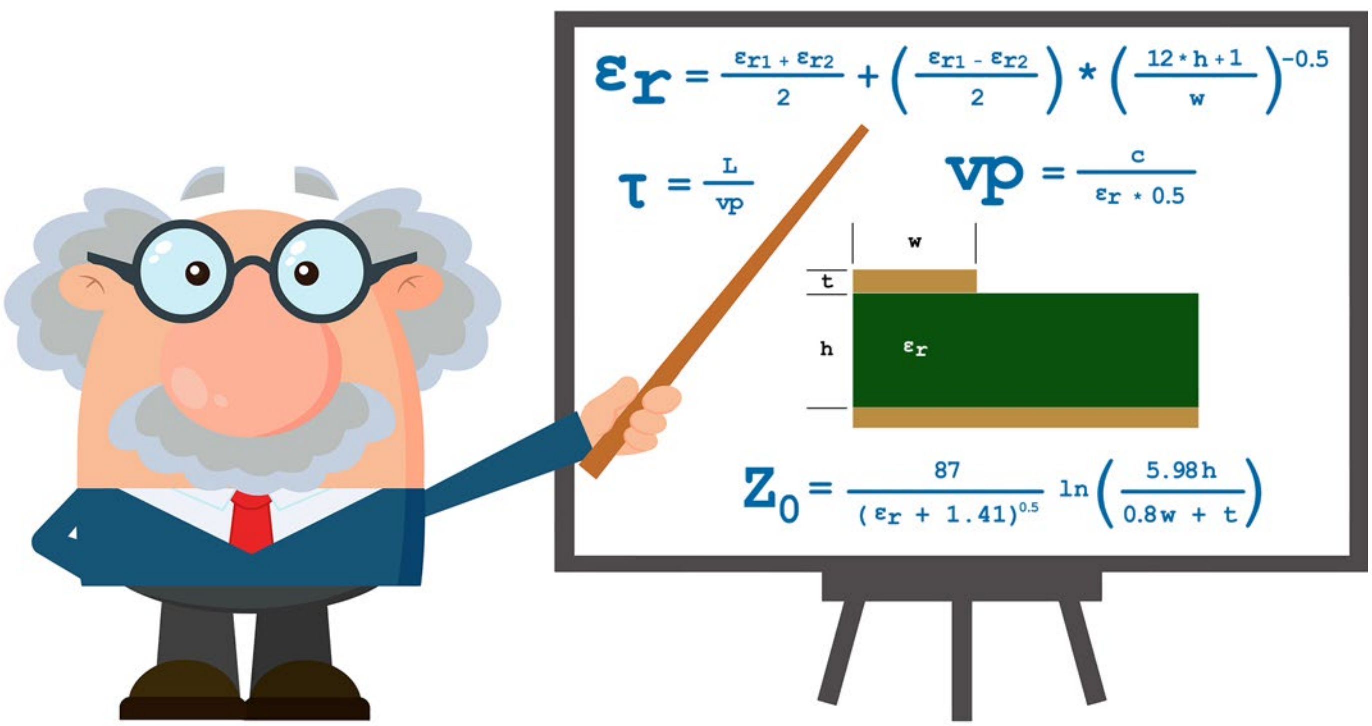
Connect the Dots

by **Matt Stevenson**, SUNSTONE CIRCUITS

Modern high-speed and RF PCB design is an exciting field but it comes with its own set of challenges. Signal integrity, performance, and crosstalk become major concerns. Designers for these types of projects need to learn how to control electromagnetic interference (EMI) and compatibility (EMC), which means utilizing some interesting math and calculations.

These designs rely on controlling impedance to improve signal integrity and reduce EMI. PCB traces are there to conduct signals from one component or device to another, and when the impedance of those traces matches the characteristic impedance of a transmitting device, the maximum signal can be sent. This method limits both signal reflection and interference. However, beyond impedance there are other critical values and calculations that the designer must understand.

An impedance structure refers to physical configuration of components on a PCB, including microstrips, striplines, and coplanar



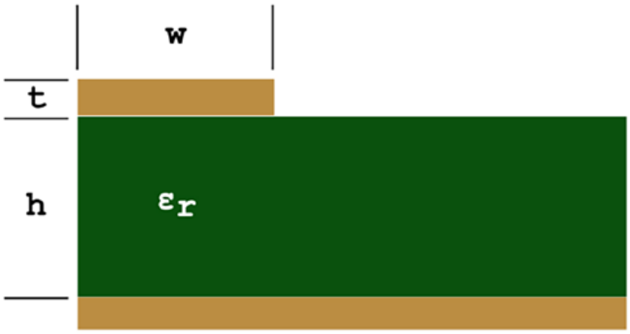


Figure 1: Illustration of a microstrip trace.

waveguides. The microstrip line is the most common type of impedance structure: an external trace separated from a plane layer by a dielectric material. Microstrips are compact, allowing for greater design flexibility. They are also easy to probe and measure, making them suitable for easy fabrication and a wide range of applications.

Figure 1 shows a microstrip trace with width (w) and thickness (t). The dielectric material separating the trace from the plane has an overall thickness of h and a dielectric constant of ε_r.

Key Calculations Involved in Microstrip Design

Incorporating a microstrip line into a PCB requires calculations involving the analysis and design of transmission lines which are widely used in microwave and RF circuits. Characteristic impedance, the effective dielectric constant, and propagation are all critical pieces of information for the designer to understand.

Characteristic Impedance

Characteristic impedance (Z_0) is the ratio of voltage to current in a transmission line and is an important parameter for determining the performance of microstrip circuits (Figure 2).

$$Z_0 = \frac{87}{(\varepsilon_r + 1.41)^{0.5}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

Figure 2: Illustration of characteristic impedance.

The characteristic impedance of a microstrip line can be approximated as:

h is the height of the substrate
w is the width of the trace
t is the thickness of the trace

Effective Dielectric Constant

Effective dielectric constant (ε_r) is the relative permittivity of the substrate material as seen by the signal on the microstrip line (Figure 3). For a microstrip line, the dielectric of the material and the dielectric of the surrounding air are the two values that are used to understand the effective constant.

$$\varepsilon_r = \frac{\varepsilon_{r1} + \varepsilon_{r2}}{2} + \left(\frac{\varepsilon_{r1} - \varepsilon_{r2}}{2}\right) * \left(\frac{12 * h + 1}{w}\right)^{-0.5}$$

Figure 3: Illustration of effective dielectric constant.

εr1 is the permittivity of the substrate
εr2 is the permittivity of the air above the substrate
h is the height of the substrate
w is the width of the trace

Velocity of Propagation

The velocity of propagation (vp) is the speed of a signal as it travels down the microstrip line—or through any transmission line. It is typically expressed as a fraction of the speed of light, due to the effective dielectric constant of the substrate material (Figure 4).

$$vp = \frac{c}{\varepsilon_r * 0.5}$$

Figure 4: Illustration of velocity of propagation.

c is the speed of light in a vacuum: 300 million meters/second

Propagation Delay

Propagation delay (τ) is the time taken for a signal to travel down the microstrip line. This is a relatively straightforward equation using the velocity of propagation and the distance the signal must travel (Figure 5).

$$\tau = \frac{L}{vp}$$

Figure 5: Illustration of propagation delay.

L is the length of the microstrip line

Putting It Into Action

To illustrate how all these equations come together, let us examine how to calculate the numbers around a fairly common design structure: a 50Ω microstrip. For this microstrip configuration, we will use the following values:

Z_0 = 50Ω
h = 0.0146"[1]
t = 0.0024"
ε_{r1} = 4.1
ε_{r2} = 1.00[2]

The first step is to calculate the effective dielectric constant (ε_r) for the external trace using the equation we discussed previously. Make sure you keep track of the output. In our example, we get:

ε_r = 2.808

Next, we must determine the required trace width to meet our 50Ω target. The width of the required trace will depend on the thickness of the copper layer on the PCB (t), the effective dielectric constant (ε_r), and the desired characteristic impedance (Z_0).

We next use the characteristic impedance equation discussed earlier and solve for trace width (w). You might need to use a calculator or equation solver to calculate w[3].

By inputting the values we have calculated already, we find:

w = 0.030" (30 mils)

This requires another look. The resulting 30-mil trace is a little on the wide side for most designs. However, if controlling impedance is critical, then this is the measurement the design must account for. If a 30-mil trace will absolutely not work, other variables can be modified to still achieve the required impedance. For example, both material type and thickness could be altered to meet our target numbers.

For Fun

Since length is such an important part of the equation, it is interesting to calculate the propagation delay for a 3"- and 6"-trace. Here's how the numbers work out:

For 3" trace, $\tau = 4.2 \times 10^{-10}$ seconds
For 6" trace, $\tau = 8.5 \times 10^{-10}$ seconds

Design Tips

Trace Thickness (t): The thickness of the trace should be at least 1-ounce copper (0.0014") to ensure good current handling capability. In this example, we used 1-ounce copper (0.0014") plated to 0.0024".

Trace Spacing Calculation: To minimize crosstalk between traces, make sure the spacing between those traces is at least three times the height of the dielectric substrate.

Tying It All Together

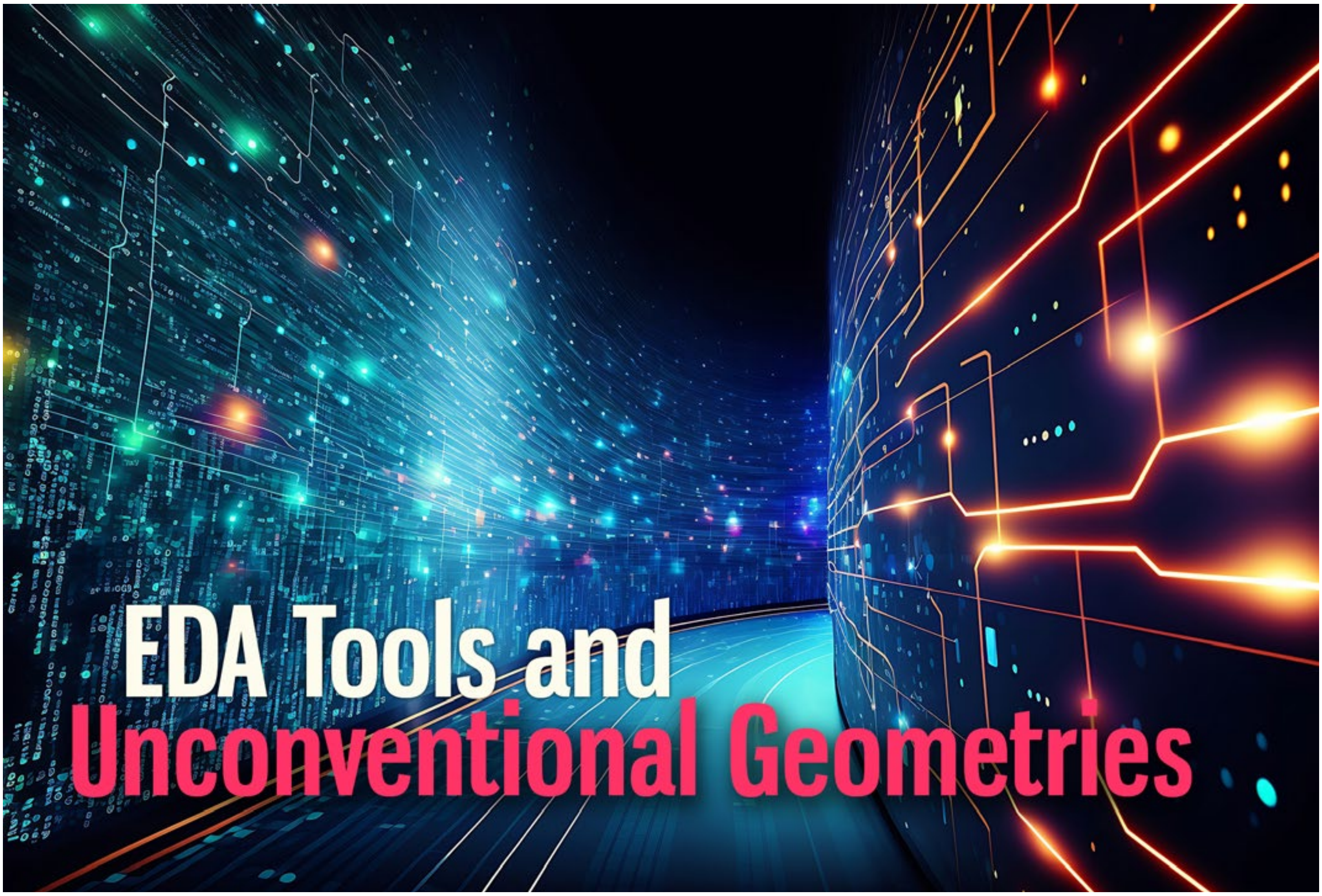
These calculations will help you create 50Ω traces for high-speed and RF PCBs that provide good signal integrity and minimize loss. In addition, with these equations in your toolkit, you are ready for any variation in impedance control. However, remember that PCB substrate quality and manufacturing process accuracy will have a big impact on the performance of the transmission lines in RF circuits.

We look forward to seeing what you will design next. DESIGN007

References

1. This is the standard dielectric thickness of some manufacturers' 6-layer stackup.
2. Don't forget to account for air.
3. It's time to dust off those rules for manipulating natural logs.

Matt Stevenson is vice president at Sunstone Circuits, a division of American Standard Circuits. To read past columns, click here.



EDA Tools and Unconventional Geometries

Feature Interview by Andy Shaughnessy
I-CONNECT007

Designing PCBs with embedded components has never been a simple task, and traditional EDA tools required designers to employ a variety of workarounds. Fortunately, the EDA software tools of today are much better equipped to work with embedded components than previous design tools.

We asked Stephen Chavez, senior product marketing manager with Siemens, to discuss the company's approach to designing embedded components. He also explains how designers can take advantage of today's ECAD tools, which feature greater integration with the MCAD tool environment.

Andy Shaughnessy: From an EDA tool company viewpoint, what are some of the biggest challenges your customers have in designing PCBs with odd or unconventional geometries?

Stephen Chavez: Today's EDA PCB tools have come a long way in their capabilities of handling odd or unconventional geometries. Some handle this better than others in addressing issues such as:

- Board outlines with true arcs integrated
- Odd-shaped holes/cavities that go part-way or all the way through a board
- Any angle placement on any layer
- True-arc and odd-angle traces
- Rigid-flex nonuniform stackups

In general, and throughout the industry, the biggest challenges arise when engineers who are still following legacy design methodologies toss unverified or unvalidated designs over the wall to fabrication and "hope for the best." Then they wonder why they are hit with so many technical queries, or worse, are told by

their fabricator that their PCB design is impossible to build without making significant manufacturing-related modifications.

PCB fabricators are tuned to standard uniform boards that make manufacturing relatively easier than when they are not uniform. This does not mean that fabricators can't handle odd or unconventional geometries, because most can. Addressing the board handling and NC drill files for odd board outline geometries or contours and slots are just a few things that can potentially add to the complexities PCB fabricators are forced to deal with today.

Just know that odd or unconventional geometries potentially have additional costs, lower yields, increase risks, and lengthen lead times with regard to manufacturing preparation and execution when dealing with anything outside the industry norm (i.e., nonuniform PCBs).

This, however, is not an issue for the EDA tools offered by Siemens. Our solutions, including our MCAD-ECAD co-design tools, can easily handle simple to extremely odd or unconventional, complex geometries. This includes dealing with the multiple board outlines, stackup zones, and constraint regions typically found in today's complex PCBs and rigid-flex designs. We highly recommend the industry best practice of consulting your PCB fabricator from the very beginning of the design cycle so that all potential issues and concerns, from design to fabrication, are addressed or mitigated.

Some round PCBs have components that need to be placed at odd angles, like 33 degrees. How does Siemens approach this sort of task?

As stated earlier, our solutions can easily handle simple to extremely odd or unconventional complex geometries. This includes component placement orientations such as the assembly of off-45-degree components. No matter what degree of component orientation is required for a design regarding placement, our solutions and approach in addressing odd-angle component orientation are not an issue for us and are implemented no differently than placing and rotating per the industry norm. Again, we highly recommend the industry best practice of consulting with your fabrication and assembly supplier(s) as early as possible in the design process and well before the design is finalized. That way all concerns and issues can be addressed up front, yielding the best potential for a successful design-for-manufacturing PCB.

Stephen Chavez

Some designers say that even today, PCB design software tools don't do a good job with 360-degree arc routing on the edge of a circular PCB. But Siemens seems to have this capability. What should designers do differently when routing circular boards?

Siemens addressed the issue of 360-degree arc routing on the edge of circular PCBs many years ago. The key is a solid and seamless MCAD-ECAD integration and collaboration that includes bi-directional data exchange and communication. Tight ECAD-MCAD integration passes on complex geometries as designed

in MCAD, not some degraded variant (e.g., fragmented arcs). When routing, you can mirror the outline, maximizing space and simplifying routing. This tight integration between these two disciplines is the key to ensuring downstream success. Designers should consult with and maintain constant communication with their PCB fabricator, especially when dealing with odd or unconventional, complex board geometries.

A lot of these PCBs in odd geometries begin life in MCAD software. What do designers need to know about importing IDF, DXF, or STEP files into the ECAD world?

The data exchanged from MCAD to ECAD must cover all physical perspectives, including beyond the realm of the 2D perspective. It's a 3D problem. Collaborating on an accurate digital twin (e.g., ensuring that ECAD and MCAD see the same thing) is about more than the board outline. Consideration of critical features such as mounting holes, heatsinks, slots, contours, and components at any angle or location, as well as height constraints zones, are examples of information that must be addressed cohesively between the two disciplines and their respective worlds. The key is a solid and seamless MCAD-ECAD integration and collaboration that includes bi-directional data exchange and communication.

Designers should consult with and maintain constant communication with their PCB fabricator, especially when dealing with odd or unconventional, complex board geometries.

We highly recommend the industry best practice of using the Interdomain Design Xchange (IDX) when passing data between the MCAD and ECAD disciplines and their respective domains, which is easily done within the solutions offered by Siemens. IDX is the industry's latest and greatest design exchange format. The two older exchange formats, DXF (Drawing Interchange Format) and IDF (Intermediate Data Format), can represent only parts of the required data. STEP (standard for the exchange of product model data) does yield a true 3D representation of design data and can be used for PCBs, components, mechanical assemblies/housings, and any other design files which may be collaborated on by multiple designers using different programs, but it has no functionality for true collaboration and requires manual checking by each designer to ensure design data is correct and up to date. Therefore, the legacy formats are enhanced by the IDX XML schema for the best potential for successful MCAD-ECAD co-design.

What advice would you give designers who are moving into designing PCBs in odd-shaped geometries?

Fully understand the basics of PCB design, master your EDA tools, and implement industry best practices by following industry guidelines and standards when designing odd or unconventional geometries. Seamless integration and collaboration for MCAD-ECAD co-design, along with the use of the IDX data format, and constant communication with both your PCB fabrication and assembly suppliers starting as early as possible, are key for achieving PCB design success of odd or unconventional geometries.

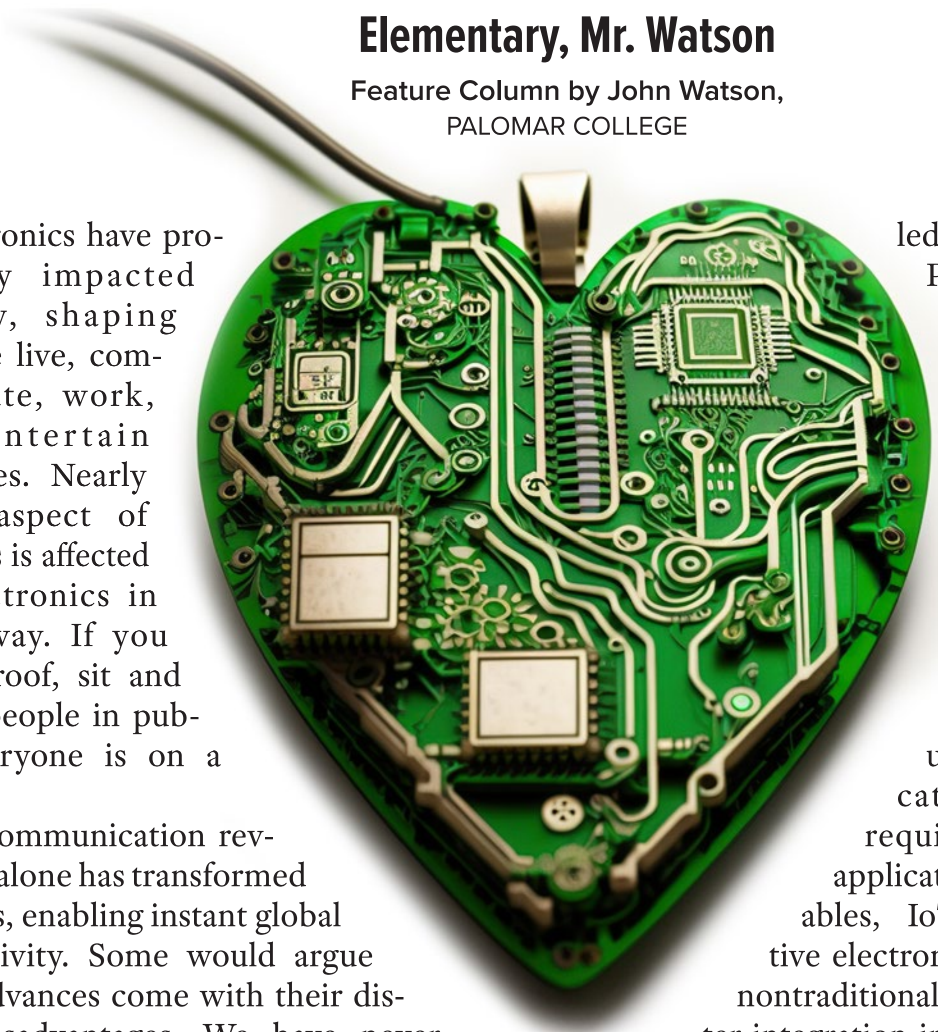
Thanks for your insight, Steph.

Thank you, Andy. Always a pleasure. **DESIGN007**

Consider Physics When Designing Non-traditional Geometries

Elementary, Mr. Watson

Feature Column by John Watson,
PALOMAR COLLEGE



Electronics have profoundly impacted society, shaping how we live, communicate, work, and entertain ourselves. Nearly every aspect of our lives is affected by electronics in some way. If you want proof, sit and watch people in public; everyone is on a screen.

The communication revolution alone has transformed our lives, enabling instant global connectivity. Some would argue these advances come with their distinct disadvantages. We have never been more connected but more isolated without face-to-face conversations. Smartphones, the internet, social media platforms, and email have transformed how we interact, share information, and conduct business worldwide.

In this realm of modern innovation, PCBs have undergone a profound evolution in their functionality, shapes, and materials. The increasing demands for smaller, more powerful, and more efficient electronic devices have led to a paradigm shift in PCB design and manufacturing.

One of the significant impacts of innovation on PCB shapes is the move away from conventional rectangular and square boards toward more customized and irregular shapes. These unconventional shapes cater to the specific requirements of diverse applications, such as wearables, IoT devices, automotive electronics, and more. These nontraditional shapes allow for better integration into the final product's form factor, enabling designers to maximize space utilization within the device.

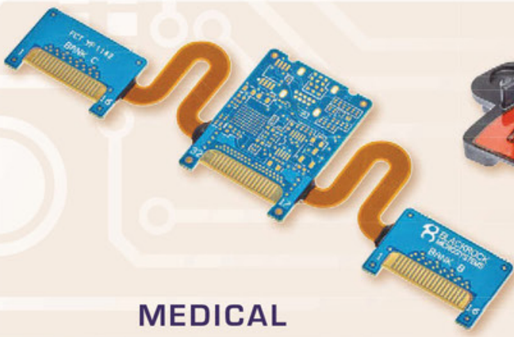
But there is something that is much more important here. Yes, PCBs are the foundational backbone of every modern electronic device, and they're composed of relatively simple fiberglass, copper, and dielectric materials. Every PCB has two purposes: First, to provide a method of placing components, and second, to make all the required interconnections between those components. That, in its

PREMIER GLOBAL SUPPLIER of **FLEXIBLE CIRCUITS**

FLEXIBLE CIRCUITS | EMS/ASSEMBLY | CONTRACT MANUFACTURING

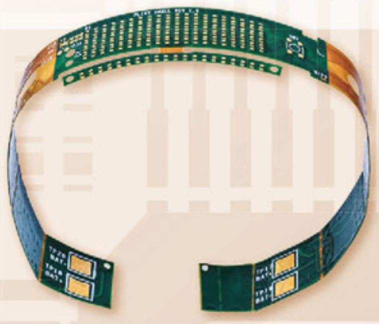
Superior design consultation & support
Flexible Circuits
Rigid Flex
Flexible Heaters
Flex/Rigid Flex Assemblies
Membrane Switches
Plastic Moldings
Specialized EMS/Assembly
Product Module to Complete Box Builds

EXPLORE the POSSIBILITIES!



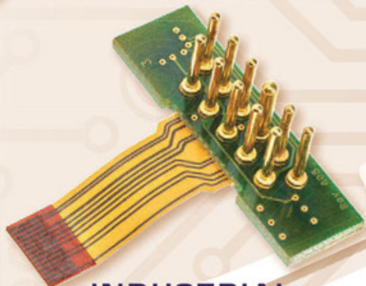
MEDICAL

AUTOMOTIVE

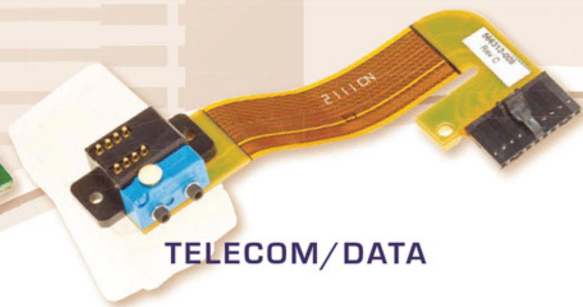


CONSUMER PRODUCTS

WEARABLES



INDUSTRIAL



TELECOM/DATA

FLEXIBLE CIRCUIT Technologies®

Flexible Circuit Technologies
9850 51st Ave. N. | Plymouth, MN 55442
www.flexiblecircuit.com | +1-763-545-3333

most basic terms, is a PCB. These purposes extend beyond mere mechanical support; they're the intricate conductors that orchestrate the symphony of electrical signals within a device. So, at their core, PCBs provide a structured framework, and, I would add, a controlled environment by arranging these components on a board and linking them with conductive pathways (traces). PCBs facilitate the flow of electricity precisely where needed, ensuring proper functionality.

Some novices believe that PCB design is just "connecting dots" in the schematic and routing in the PCB, but design encompasses so much more. A PCB is a controlled environment. Our PCB refers to the deliberate design and engineering practices implemented to regulate various factors influencing electron flow and electrical performance. This controlled environment ensures reliability, stability, and optimized functionality within an electronic system.

Each electronic component on the PCB is like a musician, playing a unique part in the composition.

With the ever-increasing demand for smaller electronic devices, which in turn means higher-density PCBs, the PCB design process cannot be done in a vacuum. Looking at only one aspect, such as the board shape, without looking at everything else, sets us up for failure. There is a balance and what I would refer to as a symbiotic relationship within the entire PCB—the flow of electrons in copper and how it interrelates to the fiberglass and other copper areas. Any change in one of these factors will affect the physics of the PCB. Any changes in the "platform" (especially the board shape) further impact the design's physics, such as controlled impedance, signal Integrity, and EMC/EMI consideration. Throughout the PCB design, with any changes, there are documented trade-offs for changes; some are improvements, and others are not. Know these trade-offs and know if implementing a change would cause more problems.

I have heard various analogies to describe a PCB design, including a city with the buildings being components, and the streets being routing. But one of my favorites is considering a complex orchestra performance where various musicians with distinct instruments come together to play a symphony. In this analogy, the PCB represents the stage where this intricate performance unfolds.

Each electronic component on the PCB is like a musician, playing a unique part in the composition. The conductive pathways on the board act as musical scores, guiding the flow of electrons like musical notes flowing through the air. Just as in an orchestra, where timing, coordination, and harmony are crucial, the PCB maintains a delicate balance. The precise arrangement of components and traces mirrors the musicians' seating arrangement and sheet music, ensuring that every electron (note) reaches its destination at the right time and in the correct sequence.

As a conductor guides and coordinates a diverse group of musicians, the controlled environment of the PCB orchestrates the electron flow. It carefully manages impedance, signal integrity, and interference, ensuring each musician plays in tune and at the right tempo, preventing overlaps or disruptions.

Just as an orchestra requires a well-designed stage and acoustics to produce a flawless performance, a well-engineered PCB provides the environment for electrons to move efficiently, harmoniously, and flawlessly through an electronic system, producing the symphony of functionality that powers modern technology.

Let me demonstrate my point. Consider the 62-mil PCB in Figure 1. It features a four-layer stackup of two signal layers on the outside and a ground and power plane on the two internal layers. A differential pair was routed on the top layer with the internal ground plane as its ref-

#	Name	Material	Type	Thickness	Dk	Df	Weight
	Top Overlay		Overlay				
	Top Solder	SM-001	Solder Mask	1 mil	4	0.03	
	Top Surface Finish		Surface Finish	0.787 mil			
1	Top Layer	CF-004	Signal	1.378 mil			1oz
	Dielectric 1	PP-0017	Prepreg	5.1 mil	4.3	0.02	
	Dielectric 1	PP-0017	Prepreg	5.1 mil	4.3	0.02	
2	Int1 (GND)	CF-004	Plane	1.378 mil			1oz
	Dielectric 3	Core-040	Core	31 mil	4.6	0.02	
3	Int2 (PWR)	CF-004	Plane	1.378 mil			1oz
	Dielectric 4	PP-0017	Prepreg	5.1 mil	4.3	0.02	
	Dielectric 5	PP-0017	Prepreg	5.1 mil	4.3	0.02	
4	Bottom Layer	CF-004	Signal	1.378 mil			1oz
	Bottom Surface Finish		Surface Finish	0.787 mil			
	Bottom Solder	SM-001	Solder Mask	1 mil	4	0.03	
	Bottom Overlay		Overlay				

Figure 1: Details of a 62-mil PCB stackup that had to be reduced to 32 mils, potentially causing a variety of snafus.

erence, with a distance of 10.2 mils. The trace width required to obtain a 100-ohm impedance matched pair is 6.41 mils. If everything works fine, the environment will be considered controlled.

Because of a lack of planning, mechanical changes are required to make the product smaller and sleeker. The PCB stackup width must be cut in half—down to 32 mils. These are the sort of changes that keep PCB designers up at night. A relatively simple change causes considerable problems in the design, especially in how these differential pairs work. Not making any changes in the PCB in terms of material, with the new thickness on the PCB, means that the trace width cannot exceed 4.226 mils. This change may also affect the required distance between the two traces to allow the correct coupling of the energy wave of each trace to allow them to work correctly and cancel any noise.

In conclusion, meticulous considerations are vital when altering the PCB's physical aspects and impacting its physics. Validate material changes for their electrical properties, ensuring compatibility with signal propagation and impedance requirements. Evaluate the impact of shape modifications on electromagnetic interference (EMI) and signal integrity, conducting simulations or analyses to anticipate disruptions. Assess thermal properties to prevent overheating or impedance variations due to alterations. Follow industry standards and guidelines to maintain desired characteristics. Collaborate with electrical engineers and utilize simulation tools to predict and mitigate potential changes in impedance, signal loss, or EMI. Test prototypes rigorously to validate alterations before final implementation.

Do not decide to change the shape of the PCB without considering how those changes will impact your overall PCB design, the pros and cons, and whether you are opening the proverbial can of worms. **DESIGN007**

John Watson is a professor at Palomar College, San Marcos, California. To read previous columns, click here.

Return Path Optimization

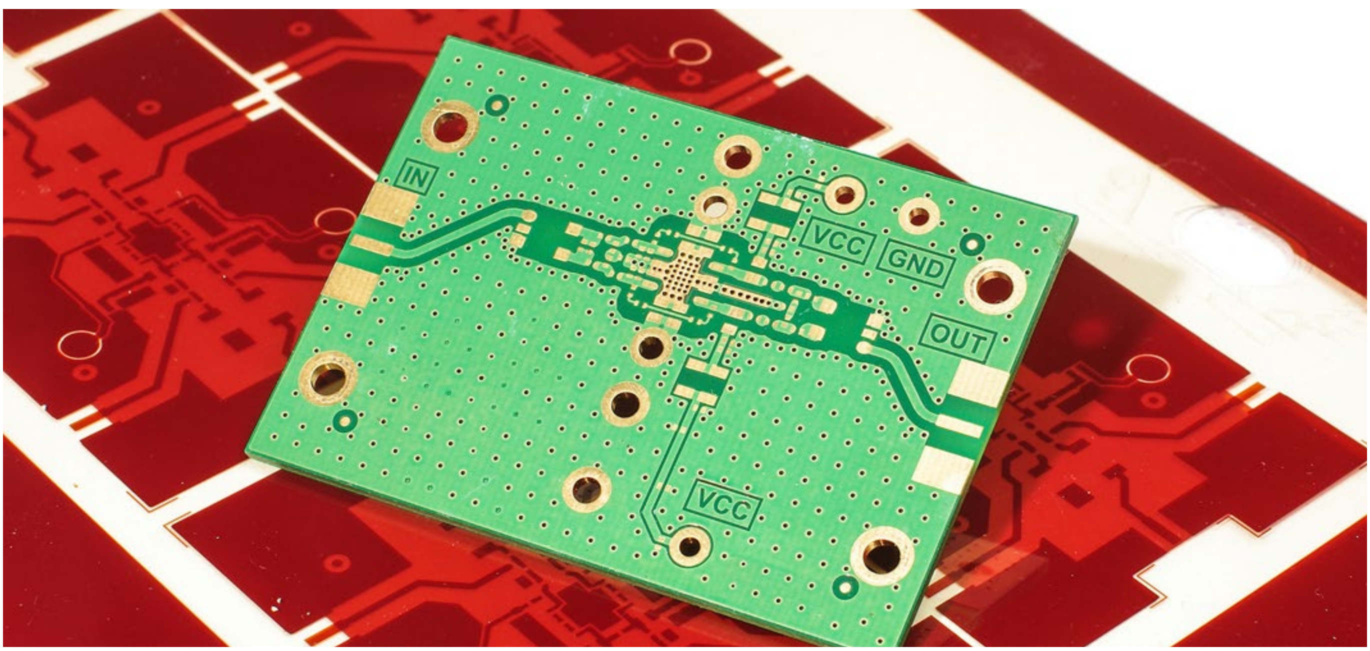
Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

High-speed PCB design is not as simple as sending a signal from the driver to the receiver over a transmission line. One should also consider the presence and interaction of the power distribution network (PDN) and how and where the return current flows. A logic schematic diagram masks detail crucial to the operation of unintentional signal pathways vital to the understanding of signal performance, crosstalk, and electromagnetic emissions. The PCB designer needs to be able to visualize the connectivity of the return current flow to avoid large loop areas that increase series inductance, degrade signal integrity, and increase crosstalk and electromagnetic radiation.

We think of a copper plane as a thick, solid plate of copper that can basically handle any amount of current we sink into it. It also serves to make the circuit layout easier, allowing the PCB designer to ground anything anywhere without having to run multiple tracks. That may well be the case with DC or very low-frequency analog circuits, but certainly not in the case of high-speed design. The return displacement current takes the path of least inductance in the nearest plane(s). Returning signal currents tend to stay near their signal conductors, falling off in intensity with the square of increasing distance.

Ground impedance is at the root of virtually all signal and power integrity problems; low ground impedance is mandatory for both. This is readily achieved with a continuous ground reference plane but becomes increasingly




We are dedicated
to excellence through
innovation,
technology
and most importantly,
service.
COMMERCIAL • MILITARY • MEDICAL • BAREBOARD
U.S.C.
U.S. CIRCUIT
www.uscircuit.com
ISO
9001 CERTIFIED
DEPARTMENT OF DEFENSE
UNITED STATES OF AMERICA
ITAR

difficult with the addition of more and more plane layers on a multilayer PCB. A ground plane serves well as a signal return, provided the ground is continuous under the signal path. But even with a continuous return path, there may be enough voltage drop across the plane to generate a common mode voltage.

If left unchecked, it may escape as electromagnetic emissions via the signal or power/ground conductors. Return path discontinuities have a huge impact on supply bounce of single-ended signals. Fortunately, differential signaling dramatically reduces this effect. Serial interfaces also significantly reduce the number of interconnects, which is another advantage over the use of parallel buses for high-speed design.

Small discontinuities, such as vias and non-uniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems. These produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel-to-channel noise, and may promote mode conversion. In the case of differential pairs, the transformation from differential-mode to common-mode typically takes place on bends and non-symmetrical routing near via and pin obstructions, but can also be caused by small changes in impedance due to return path issues.

One must also understand the importance of referencing and how to control the return displacement current flow of a signal. Each signal layer should be adjacent to, and closely coupled to, a reference plane, which creates a clear, uninterrupted return path and eliminates broadside crosstalk. As the layer count increases, this concept becomes easier to implement but decisions regarding return current paths become more challenging.

Although power planes can be used as reference planes, ground is more effective as local stitching vias can be used for the return current transitions, rather than stitching decoupling capacitors

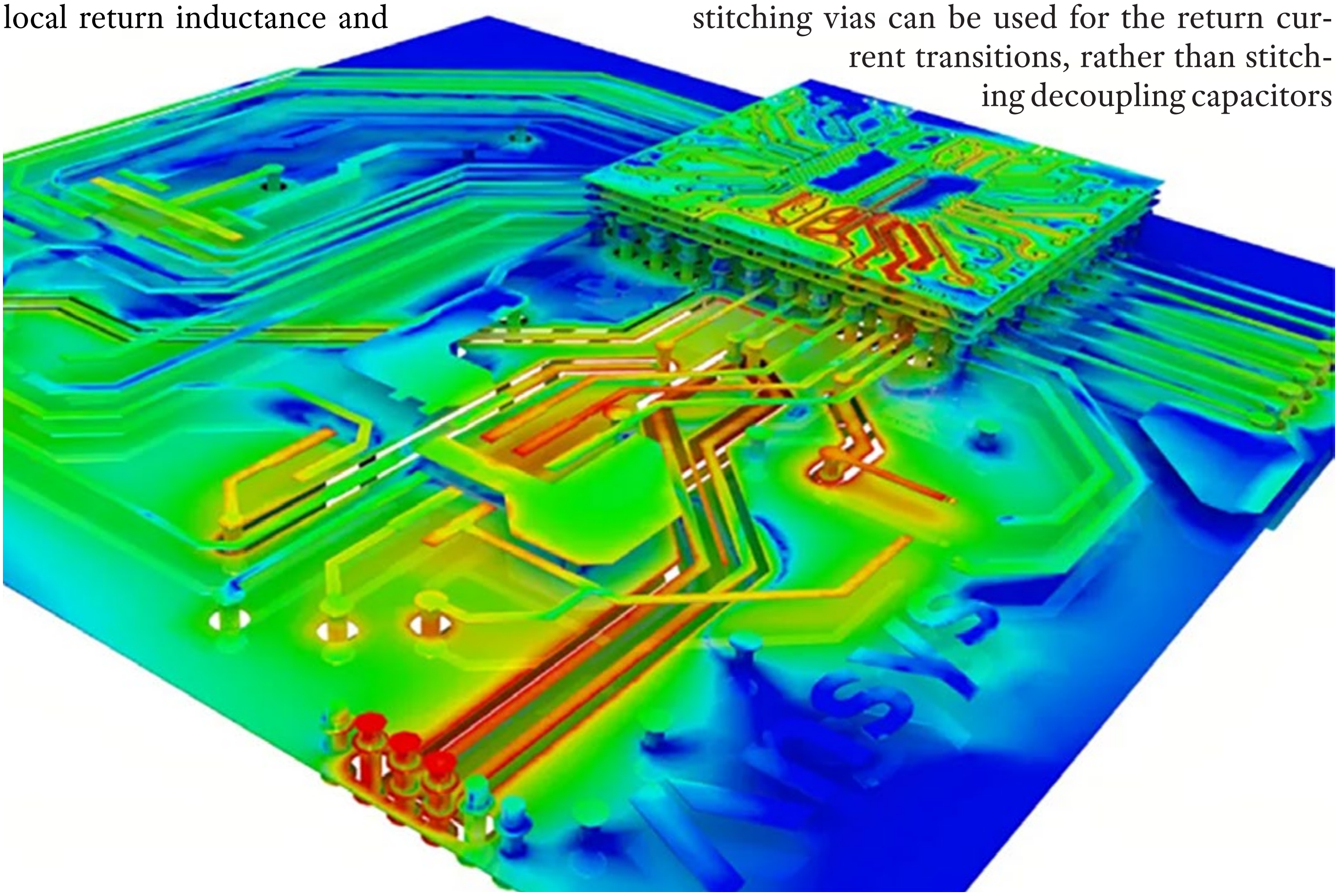


Figure 1: HFSS simulation of return paths. (Source: Ansys)

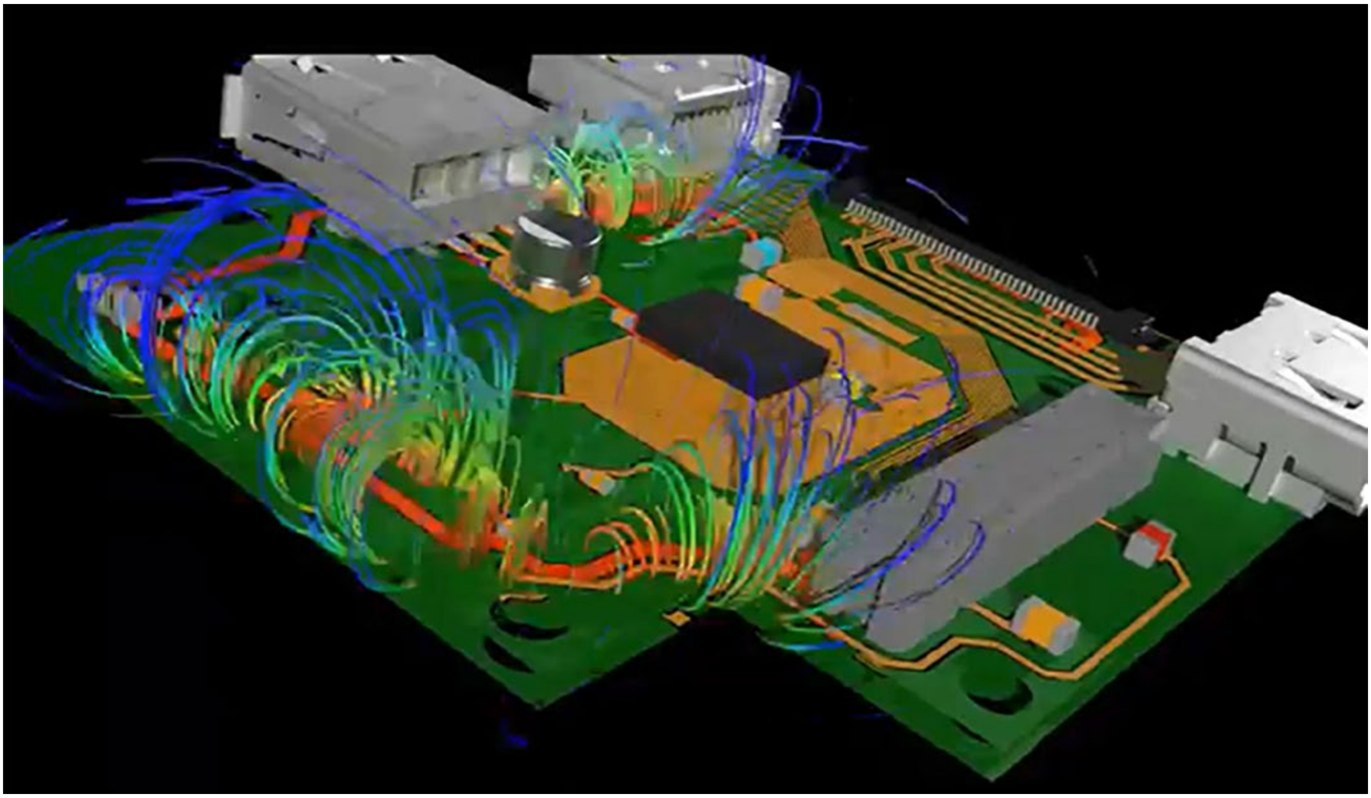


Figure 2: HFSS simulation of electromagnetic energy in microstrip. (Source: Juliano Mologni)

which add inductance. This keeps the loop area small and reduces radiation. As the stackup layer count increases, so does the number of possible combinations of the structure. But if one sticks to the basic rules then the best-performing configurations are obvious.

Figure 2 shows the electromagnetic fields emanating from signal traces in a microstrip configuration. Electric fields terminate when they come into contact with a solid plane but will radiate into the surrounding volume while magnetic fields tend to radiate unless they are shielded by the planes. But in a stripline configuration, the fringing fields still radiate from the board edges.

The return current of a high-speed, fast-rise time digital signal will always follow the path of least inductance, which is directly beneath the signal path. However, discontinuities tend to divert the return current increasing the loop area, inductance, and delay, which is not desirable. The best way to identify the discontinuities is to follow the signal path and imagine the return path closely coupled on the nearest plane. If there are multiple planes present in the layer stack, then the displacement current will still take the path of least inductance and follow closely coupled to the signal trace. If a discontinuity interrupts this return flow, then the return current will be forced into a distant plane where it has a clear run, creating increased inductance.

A via that provides the connection between signal traces, referenced to different planes, creates discontinuities. In other words, the return current has to jump between the planes to close the current loop, which in turn increases the inductance of the current loop, affecting the signal integrity. This return current also excites the parallel plate mode, causing significant EMI. If the reference planes are at the same DC potential, then they can be connected by stitching vias near the signal via transition to provide shorter paths for return currents. However, if the planes are at different DC potentials, then decoupling capacitors must be connected across the planes at these points. In addition, some of the return current flows through the interplane capacitance to close the loop.

To avoid these issues, there are fundamental rules to follow such as:

- Never allow a high-speed signal to cross a gap or split in the plane. This creates a large return path loop area and tends to radiate.
- Never route a high-speed signal near the edge of the reference plane. The fringing fields may wrap around the edge of the board and radiate.
- Never place an IC over a split plane (with the exception of DAC/ADC). The IC substrate is like a miniature multilayer PCB and may rely on a solid plane placed beneath the IC to provide a continuous return path.
- Each signal layer should be adjacent to, and closely coupled to, a reference plane, which creates a clear, uninterrupted return path and eliminates broadside crosstalk.
- A ground via needs to be placed close to every layer transition to provide a clear path for the return current.

Unfortunately, discontinuities can never be totally eliminated but we can take steps to significantly minimize the effects. As with PDN planning, it is all about inductance. If the return path loop area is increased in any way, then the inductance will also increase.

Key Points

- A logic schematic diagram masks detail crucial to the operation of unintentional signal pathways.
- The PCB designer needs to be able to visualize the connectivity of the return current flow in order to avoid large loop areas.
- The return displacement current takes the path of least inductance in the nearest plane(s).
- Ground impedance is at the root of virtually all signal and power integrity problems; low ground impedance is mandatory for both.
- A ground plane serves well as a signal return, provided the ground is continuous under the signal path.
- Return path discontinuities have a huge impact on supply bounce of single-ended signals.
- Small discontinuities, such as vias and non-uniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems.
- One must also understand the importance of referencing and how to control the return displacement current flow of a signal.
- As the stackup layer count increases, so does the number of possible combinations of the structure.
- Discontinuities tend to divert the return current increasing the loop area, inductance, and delay. DESIGN007

Resources

1. Beyond Design: "The Dark Side-Return of the Signal," "Return Path Discontinuities," by Barry Olney.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.

MilAero007 Highlights

BAE Systems to Develop Custom Microelectronics for Next-generation Radar, Electronic Warfare, and Communication Applications ▸

The Office of Naval Research (ONR) has awarded BAE Systems' FAST Labs research and development organization a $5 million contract for the COALESCE (Common-architecture Amplifier for Low-cost, Efficient, SWaP-Constrained Environments) program. BAE program's objective is to develop the world's highest efficiency high power amplifier module in its frequency band.

Terran Orbital Releases Enhanced Versions of Enterprise Bus ▸

Terran Orbital Corporation, a global leader in satellite-based solutions primarily serving the aerospace and defense industries, announced two additional configurations of its largest platform offered in the standard product line the Company initially announced in September: Enterprise. The Enterprise-class bus is the point of departure for flat packing requirements carrying up to 24 satellites per launch.

Viasat Deutsche Telekom Commit Long-Term to Deliver Inflight Connectivity ▸

Viasat, Deutsche Telekom Commit Long-term to Deliver Inflight Connectivity via the European Aviation Network, announced a new, long-term agreement that cements the companies' commitment to providing in-flight connectivity (IFC) solutions to airline partners across the European Aviation Network (EAN). EAN allows travelers in Europe to benefit from broadband services that support high bandwidth-demanding applications such as streaming.

Early Production Continues on Advanced Upper Stage for NASA Moon Rocket ▸

Technicians at NASA's Michoud Assembly Facility in New Orleans have completed a major portion of a weld confidence article for the advanced upper stage of NASA's SLS (Space Launch System) rocket. The hardware was rotated to a horizontal position and moved to another part of the facility Oct. 24.

Aalyria to Study Ultra-High-Speed Earth-Aircraft Optical Communication ▸

This collaborative study launched with Airbus aims to achieve two distinct objectives: to advance air-to-ground and air-to-air free-space optical communications technologies to improve their compatibility with terrestrial fiber networks, and to develop network traffic engineering and orchestration techniques to meet the needs of future air- and spaceborne networks.

CACI Awarded NASA Contract for Human Spaceflight Systems, Simulation and Software Technology III ▸

CACI International Inc has been awarded a four-year single-award, indefinite delivery indefinite quantity expertise contract worth up to $150 million to continue its support of spaceflight systems, simulation, and software for NASA Johnson Space Center (JSC). The program provides advanced aerospace engineering for crewed spacecraft systems, development of simulation and Virtual Reality (VR) applications, and software in support of human space flight. This award builds on more than three decades of CACI's dedicated support for JSC's mission.

Designing Unconventional Geometries

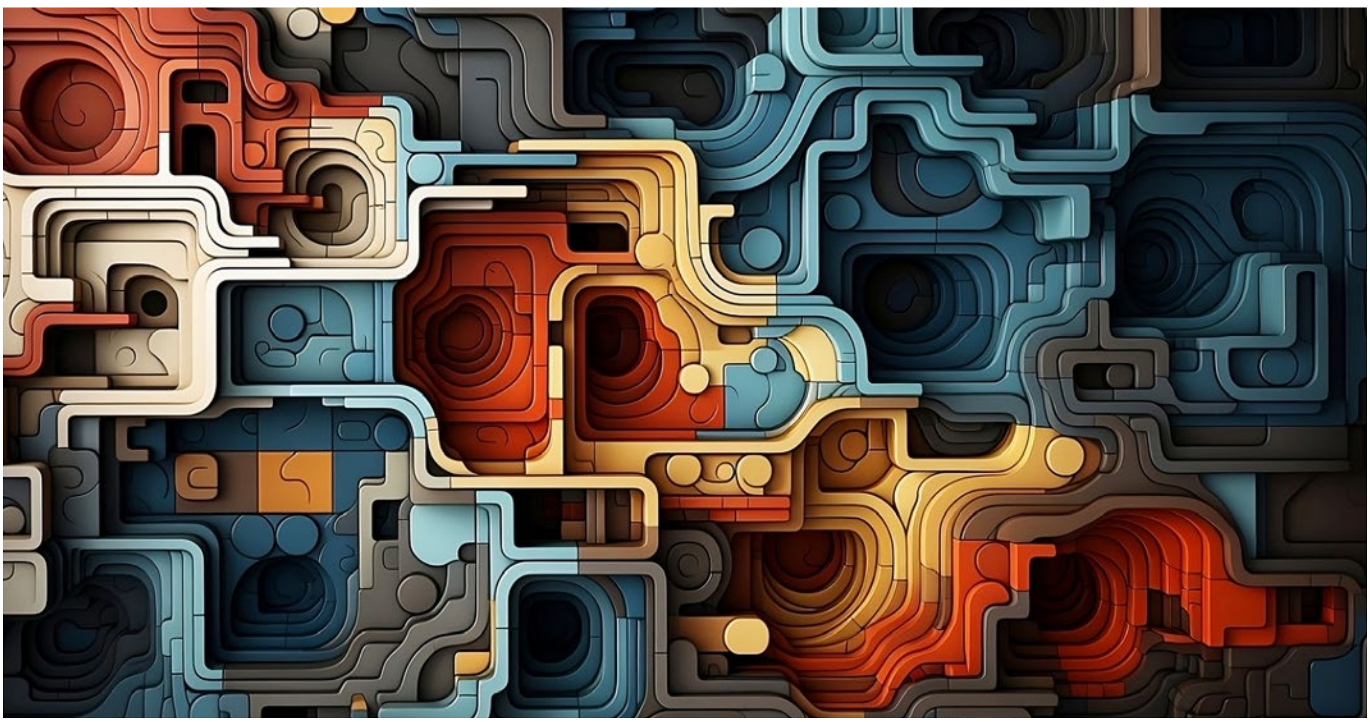
Target Condition

Feature Column by Kelly Dack, CIT, CID+

Geometric interference: *In terms of a PCB design, this is a condition in which a mechanical feature on a finished PCB could come into unwanted contact with a significant counterpart, thereby affecting further assembly or electromechanical performance.*

Geometric dimensioning and tolerancing (GDT), as covered in the pages of ASME Y14.5 and IPC-2615, is easy to understand if you speak the language. So is Mandarin. However, there is a void in the PCB design industry when it comes to conveying what is required on fabrication drawings for PCB outlines. It seems that those who speak and document PCB dimensioning and tolerancing have little patience for those who do not. The apparent state of PCB dimensioning and tolerancing knowledge in the industry is likened to the state of the city of Babel where the language is confused. There is an elephant in our industry's inspection room, and it is not backed up against three mutually perpendicular datum planes.

There are dozens of process steps a PCB goes through before completion. One of the final steps is to de-panel or excise a PCB assembly from its supporting panel structure so it can move on to its next assembly level where it must fit well. Can you imagine building and shipping a thousand simple PCB assemblies to a final assembly plant and getting a message



that PCB outlines are interfering with other parts? Now what? Rejection, return, rework, reshipping, and reinstall are profit-killers.

Conversely, imagine a PCB manufacturer put in the position of meeting an incredibly tight tolerance of ±0.005" (0.13 mm) on a PCB design that is 36" (914.40 mm) long. Challenging design constraints do not help a manufacturer's PCBs to fall neatly off the assembly line. When overly complex design specification challenges a supplier's ability to interpret manufacturing capability, expensive inspection and quality assurance process phases need to be added, requiring the expertise of additional project stakeholders.

I review hundreds of PCB designs, and I see many PCB designers wasting the valuable time of their PCB project stakeholder counterparts by misunderstanding or misusing the power of dimensioning and tolerancing techniques. PCB dimensioning and tolerancing is a language requiring a sender and a receiver. If there is a mismatch on a PCB fab drawing, failure soon follows. I see that many designers could use some help simplifying their understanding of dimensioning and tolerancing as well as language skills to better convey the performance requirements of their PCB outlines.

PCB outlines are usually defined by our mechanical engineering stakeholders who commonly provide the outline parameters in the formats of IDF, DXF, or STEP.

Unless PCB designers are designing for a "snap fit" board edge requirement or must match a complex enclosure profile—perhaps meant to seal in some potting compound or reduce the leakage of photons in a bright LED display—most PCB design outlines are given ample clearance from other parts. In fact, I think we could get most PCB designers to agree that most PCB design edge surfaces worldwide interface with relatively vast amounts of air (or space in a vacuum). If we can agree, then what can we do to enhance our dimensioning and tolerancing language skills to lower process rejection rates or reduce time wasted inspecting for needlessly wide tolerance specification at PCB fabrication and assembly facilities?

Consider these four tips:

1 Select a next assembly interface point such as a mounting hole for the design layout origin. Documenting the X0, Y0 origin is a simple way of establishing a locational datum point for the entire hole pattern which is processed in the beginning stages of manufacturing with minimal steps. A hole is a powerful datum feature to reference because it shows up on every single process layer.

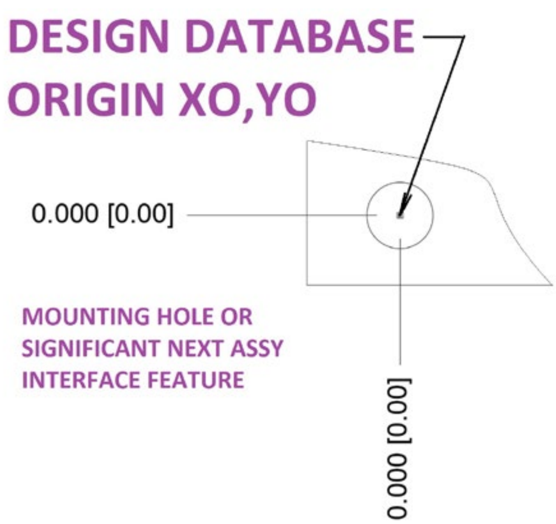


Figure 1: Image showing the origin X0, Y0.

2 Use X and Y dimensions to simply locate the PCB outline with a relative tolerance to the hole pattern. Remember, these two geometric features (the holes and outlines) are

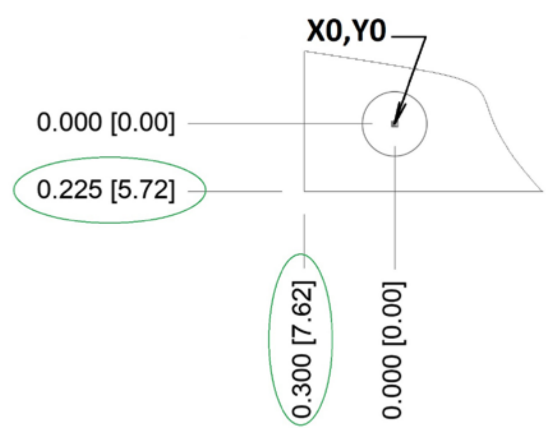


Figure 2: The X and Y locate the board outline with relative tolerance to the hole pattern.

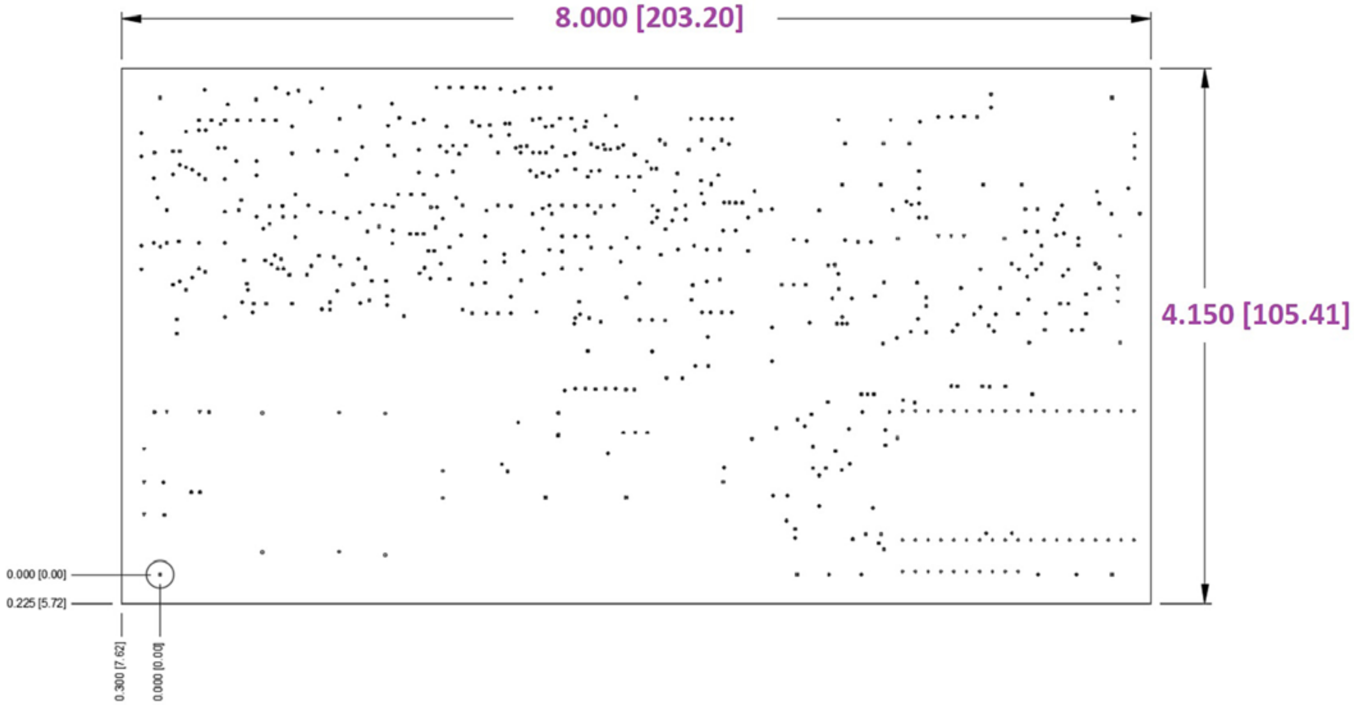


Figure 3: Overall dimensions for PCB outline.

created during entirely different phases of the production cycle. Holes are drilled toward the beginning stages, but board edges are cut or processed as part of the last. These dimensions and their respective tolerances will definitely be inspected for quality because the dimensions are present.

3 Add overall dimensions to the PCB outline. These dimensions convey more than some PCB designers think. The dimensions need to be present in order to establish a tolerance zone for the entire PCB. The dimensions are nominal values to which a zone of acceptability must be communicated. What are the board outline limits below if the tolerance is identified at ±0.005" (0.13 mm)?

What if the board outline itself is not so simple? I've worked on some LED light board designs with very complex geometry, particularly in my days designing boards for the gaming industry. How would a PCB designer dimension the outline for a PCB shaped like Batman's silhouette? How about another large PCB in the shape of the cursive signature of Frank Sinatra? Hitting the "auto-dimension" button on a design with so many arc origins and spline features would surely yield catastrophic documentation. To keep things simple, we should consider adding dimensions only to critical, next assembly interface points in order to define tolerance zones to define areas of acceptability.

PCB edges which hang aimlessly out in air or space may be considered noncritical. Do their complex arcs and spline really need dozens of dimensions? Remember, nominal data for cutting the features will be provided in the form of CAM data. If there is little chance for interference, or if the feature will end up suspended in air or space, a generally wide title block tolerance may suffice. Designers need to understand that overall dimensions are not there to tell a manufacturer how to program a routing operation—the CAD data does that—but are there for overall reference to the stakeholders who will be quoting and planning. Final inspection stakeholders have other ways to inspect the cutter's work if the designer offers the option in the form of a fabrication note.

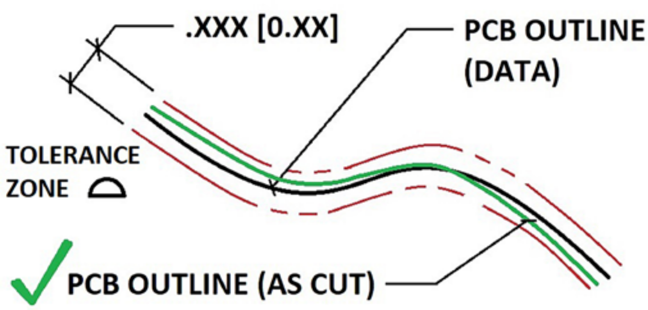


Figure 4: Board edge profile shall conform to supplied Gerber data within 0.XXX" (0.XX mm).

4 Add a simple note to specify outline profile to be inspected within 0.XXX" of design data. PCB designers and their project stakeholders can benefit from a simple technique which draws from the GDT concept of "profile of a surface." Using this technique helps eliminate countless dimensions from the fabrication print. All that is required is that the PCB designer determine an acceptable range of tolerance. Ask yourself, "If this board edge shrinks or grows by a certain amount, what are the effects?" The tolerance zone created by a profile callout automatically applies to the zone around the PCB profile regardless of its complex shape.

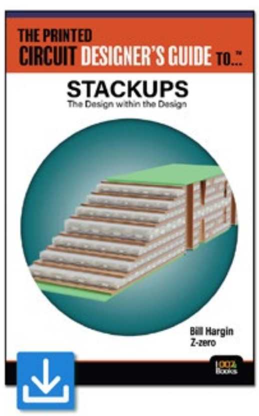
Take a hint from Batman: "Zap" these four steps into your design workflow. Your PCB will "zing" through the manufacturing and inspection phases. Your PCB stakeholder counterparts will love you and your PCB edges suspended in air will be none the worse until you go back and ask that mechanical engineer why you can't lop off Batman's pointy ear so you can fit another image on the manufacturing panel. DESIGN007

Kelly Dack, CIT, CID+, provides DFX-centered PCB design and manufacturing liaison expertise for an EMS provider in the Pacific Northwest while also serving as an IPC design certification instructor (CID) for EPTAC. To read past columns, click here.

BOOK EXCERPT

The Printed Circuit Designer's Guide to... Stackups—The Design within the Design

by Bill Hargin, Z-zero



Chapter 7: Rigid-Flex Materials

For most of my career, I worked exclusively with rigid PCBs. Rigid-flex boards were those things in my cellphone. Then, about six years ago, while working in the laminate space, I started getting requests for low-flow prepregs and getting pulled into rheology testing. Since then, I have learned a lot more about rigid-flex stackups and included rigid-flex support in our stackup-software solution. This chapter shares some of the lessons I learned along the way.

Flex and rigid-flex designs refer to a PCB that is partially or entirely constructed using dynamic, flexible substrates instead of being exclusively made of rigid substrates. Flexible materials allow for denser designs because components and traces can be placed and routed in three dimensions, eliminating physical connectors. This reduces cost and impedance discontinuities while increasing reliability. Rigid-flex designs also have improved electromechanical functionality, including dynamic bending, vibration and shock tolerance, heat resistance, and weight reduction.

Their increased shock and vibration tolerance makes flexible designs popular within medical, automotive, military, and aerospace applications that necessitate dependable field operation. The ability to bend portions of the circuitry facilitates dense constructions, leading to widespread use in flat panel displays and cellular devices, while also making wearable technology possible.

Continue reading...

UHDI FUNDAMENTALS:

Talking UHDI With John Johnson, Part 2

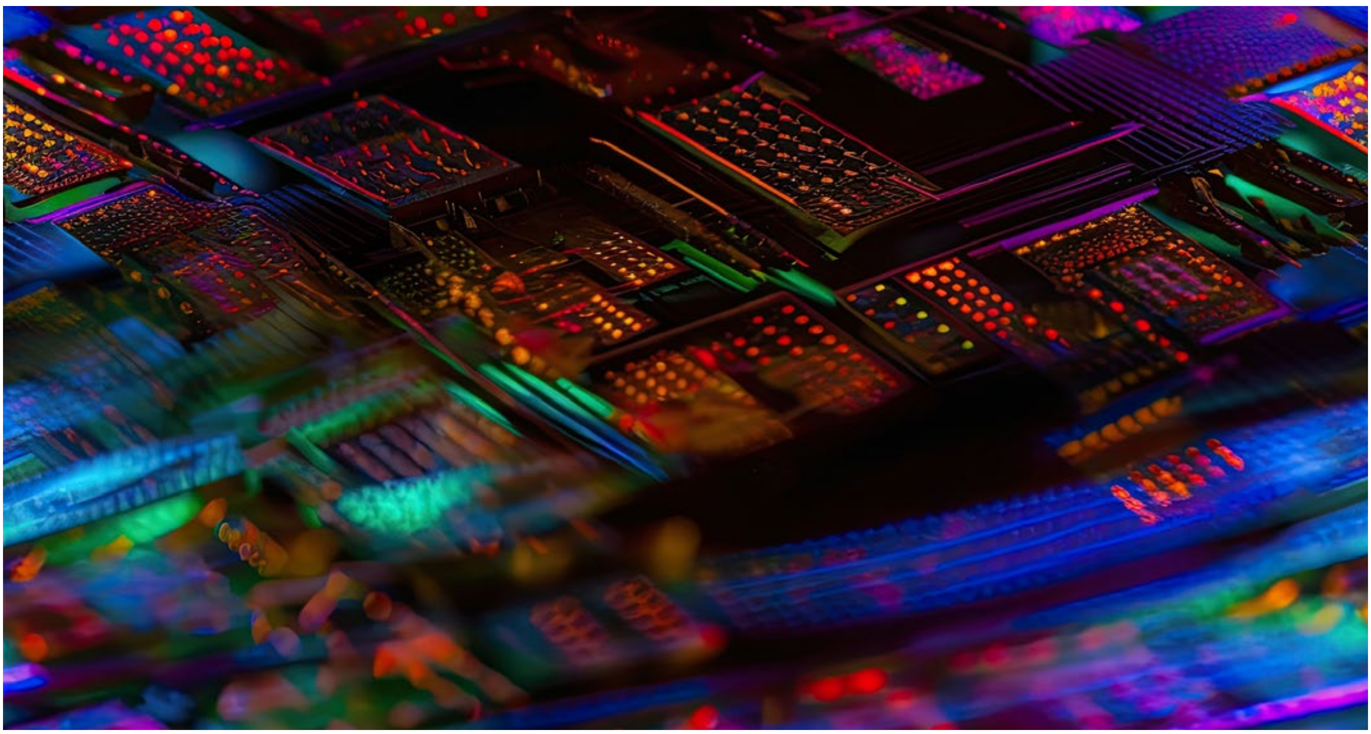
Interview by Steve Williams
FOR ASC

Editor's note: This is the second of a three-part interview. To read Part 1, click here.

American Standard Circuits is an early adopter of Averatek's A-SAP™ process for its ultra high definition interconnect (UHDI) products. I had the opportunity to sit down with industry veteran John Johnson to discuss this. John previously worked at Averatek and is now vice president of business development at American Standard Circuits where he oversees quality. In the spirit of full disclosure, we will be discussing and sharing photos, slides, and materials with permission from both ASC and Averatek.

Steve Williams: John, American Standard Circuits is a big RF manufacturer. Is there a big application for UHDI in that niche?

John Johnson: Yes, absolutely. From a signal integrity side and getting that straight sidewall, it benefits a lot. But this technology works very well to produce very, very low surface profiles, and that's an additional benefit. When you look at just building boards with controlled impedance, you can get to a much tighter tolerance. We talk in the industry of typically ±10%, but we can do 5%, so this can get you down to a much tighter tolerance the first time out of the box because you're building right to the design. Your trace will be right there, and since you're



plating up a trench—that little trench gets filled up—and that's exactly at the width the designer intended, so it's a lot easier to hit the impedance requirements.

Also, this technology has a lot of potential in the medical industry. You can make biocompatible circuit boards because A-SAP does not have any copper or nickel in the construction—which are toxic to the body. You can do traces that are all noble metals like palladium and gold, and that's a big improvement.


John Johnson

Are you doing anything biocompatible?

We are. We've built a couple of programs here with more to come.

One of the foundations of the process is liquid metal ink (LMI™). Tell me about that.

LMI is a patented Averatek chemistry for putting down a very, very thin coating of palladium on the surface. It's very dense—basically several levels deep of atoms touching atoms. It's just a few nanometers thick. That density really helps in getting plating down into all the small crevices and small vias that need to be plated. The liquid metal ink is a non-aqueous base, so that wets very well in all the little nooks and crannies that you'll see in drilled holes. You can metallize these holes much easier than standard plating chemistry. Now, bear in mind we still do use electrolytes from a variety of manufacturers, so this doesn't replace electrolytes. It creates that catalyst level that you need to get the plating accomplished, and it works with different metals. The properties of liquid metal ink could be with gold or silver as well; it's not just for palladium in this case.

That's pretty interesting. When you look at the comparison between the LMI and the standard process, it's striking.

Figure 1 illustrates what happens in a standard process when you have palladium deposited out of an aqueous solution that is dispersed. The copper tends to build slower and it's less dense during the early stages of plating. Over time it will build up a thickness dense enough that will support an electrolytic copper plating. Whereas with the LMI technique, you have a very dense level of palladium, as you see illustrated. You can plate electroless copper in a very thin deposition that will be able to conduct electricity for electroplate. That's the key differences. In the SEM image on the right of Figure 1, it shows the electroless deposition, not the palladium, which is so fine that you need a transmission electron microscope to see it. When you look, you'll see how fine the electroless deposition is, and how it has followed the topography of the copper foil that was there beforehand. That helps to give very good adhesion to that surface.

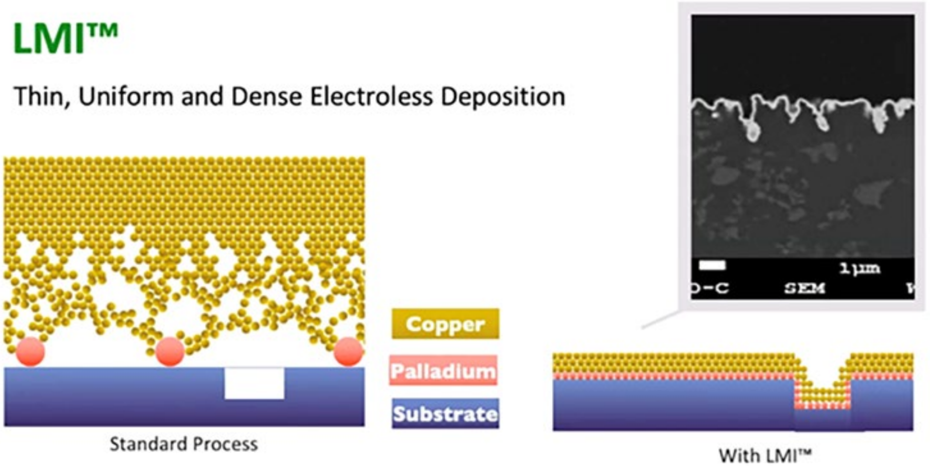


Figure 1: This is what happens in a standard process when you have palladium deposited out of an aqueous solution that is dispersed.


IPC BUILD ELECTRONICS BETTER
Community
MAGAZINE
FALL 2023
LOOK INSIDE
IPC
BUILD
ELECTRONICS
BETTER
Contact us to
become an advertiser

Is it a special process? Can board shops use their existing processing equipment and tanks, or do they have to put anything special in place?

That's the interesting thing with this technology; there are very few tanks put in place to get it set up, and very few additional lines to be run. You can use existing lines for flash etching. For example, we use our inner layer clean line—with a micro etch—to do the flash and it functions quite well. But the whole process is just using different photoresists that have the resolution capability down in the 25-micron range. As long as you have something that can resolve to that range and make the narrow lines, you're golden.

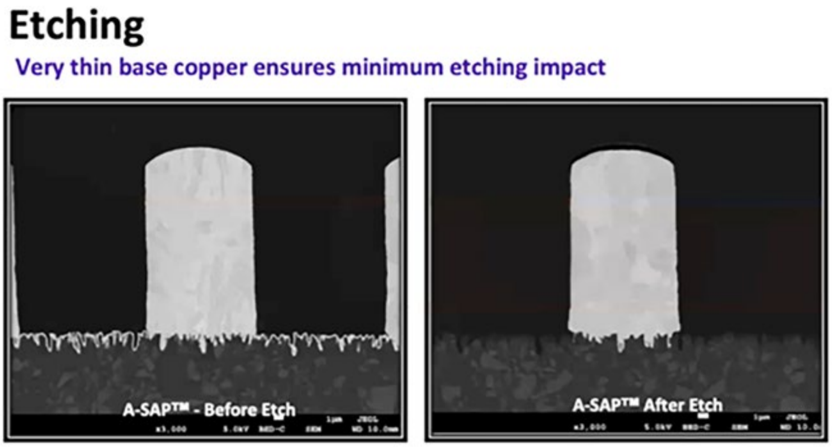


Figure 2: A comparison between the A-SAP traces before and after etching.

So, it's not quite a drop-in, but pretty close?

Yes, it's pretty close. In fact, we have some examples of product we put in for the U.S. Navy, which has been one of the early adopters. Within two weeks we were running panels there that had 25-micron line and space, and the capability with their photolithography to get down further. A few weeks after that, we were running 15-micron, down to 12.5-micron (0.5 mil) line and space. Let me tell you, as someone who has been in this industry a long time, it brought tears to my eyes. It's just beautiful; that spiral pattern was just awesome. It was zero shorts and zero opens. It's just a really good process.

In Figure 2, we have a comparison between the A-SAP process and the ultra-thin foil processes that are sometimes called mSAP in Asia. The older mSAP processes started out with a 5-micron foil, an eighth-ounce copper as we would call it in the older days. Now there are foils that are 2-micron and even as thin as a 1.5-micron. So, even with these copper weights, you're still dealing with a fairly thick base foil that you have to etch. But when you etch something that is only two-tenths of a micron base, it etches very quickly and doesn't touch the electroplated sidewalls.

Please talk about your straight edges. This is incredible. It's really staggering to look at how straight those trace sidewalls are.

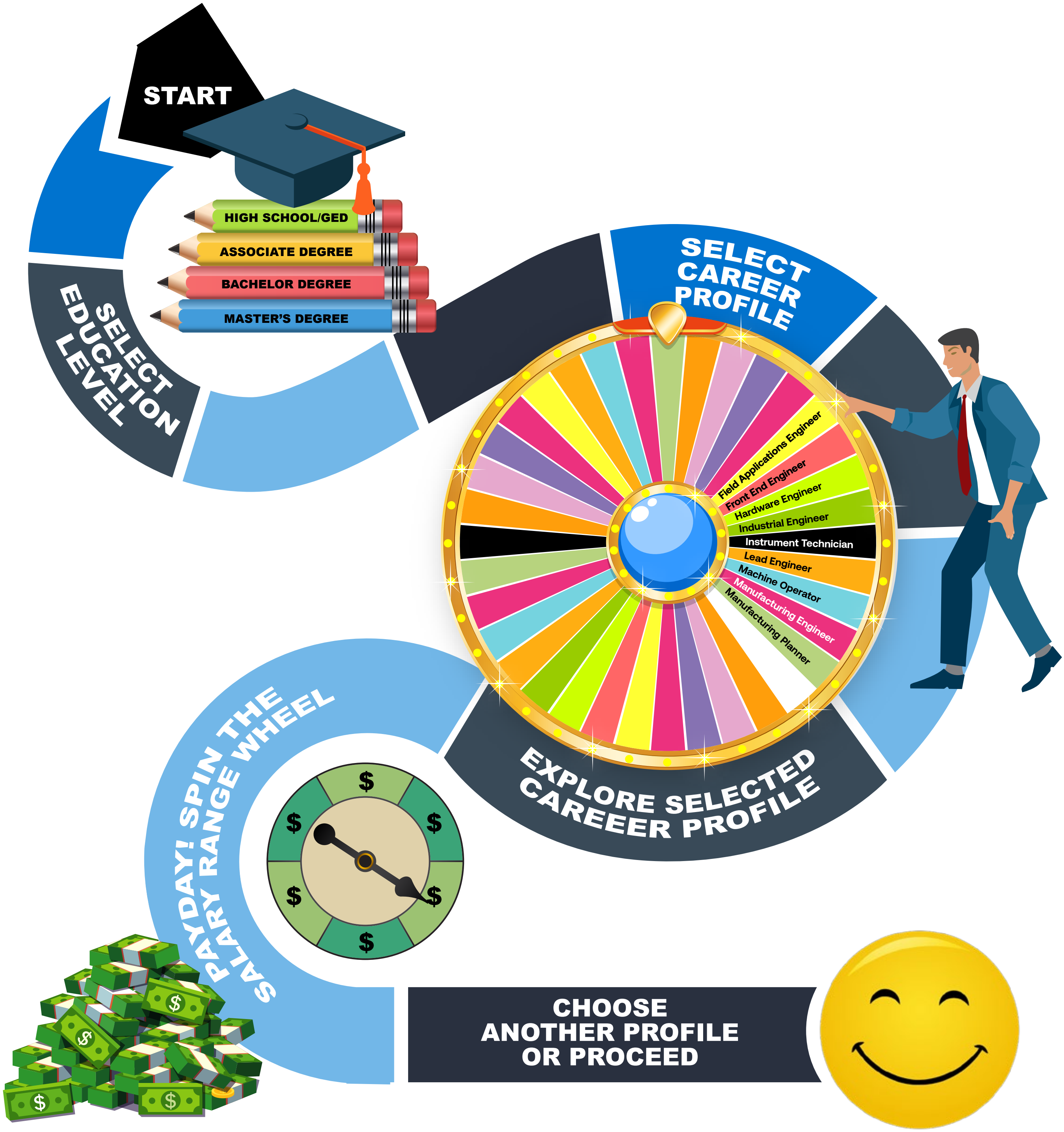
On the left, you see the trace that's been plated. It still shows the electroless down at the base and you can see how thin it is. This trace here is 11 microns wide and it's about 27 microns high, I believe. When you do the flash etch, you look at that trace and it's like it hasn't been touched. It's really amazing; it's hard to beat that sidewall.

That's just phenomenal. All those rules from way back are now out the door with aspect ratio and surface-to-hole plating. This really is a game changer.

Look for Part 3 of this interview in the January 2024 issue of *Design007 Magazine.* DESIGN007

Steve Williams is president of The Right Approach Consulting. He is also an independent certified coach, trainer, and speaker with the John Maxwell team. To read past columns, click here.

Take a spin to find your career in electronics



careers in ELECTRONICS

Flex007 Highlights

OE-A Business Climate Survey—Mixed Feelings Despite Positive Expectations ▸

"The forecast for the Printed Electronics Industry remains positive and stable. We are slightly less optimistic than in the spring survey in March of this year, with an expected sales increase of 16 percent for 2023. Nevertheless, a promising 18 percent increase is projected for 2024," says Dr. Klaus Hecker, OE-A managing director, about the results of the latest business climate survey.

Flexible Thinking: The Simplest Way Is the Best Way ▸

Interconnection substrate technologies (PCBs, flex and rigid-flex circuits, and IC packaging substrates) have made possible the steady advance of electronic products for more than seven decades. They are foundational structures for electronics and arguably the backbone of modern electronics. However, their design and manufacture has become increasingly challenging over the years.

Würth Elektronik Launches Research Project HyPerStripes ▸

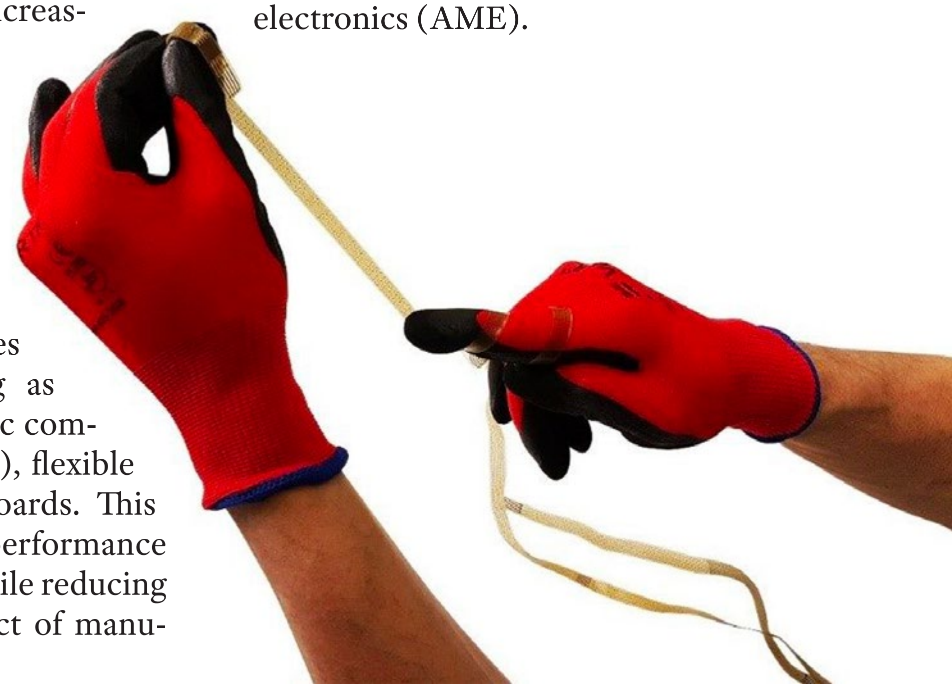
HyPerStripes project partners will create a technology platform including manufacturing techniques for roll-to-roll (R2R) processing as well as the integration of electronic components onto very long ("endless"), flexible and stretchable printed circuit boards. This will pave the way to higher-performance products and new applications, while reducing the cost and environmental impact of manufacturing.

Eltek Receives Five Purchase Orders Totaling $3.8 Million ▸

Eltek Ltd., a global manufacturer and supplier of technologically advanced solutions in the field of printed circuit boards, announced that it has received five purchase orders in a total amount of $3.8 million. The orders are in connection with two projects for a customer. Most of the orders will be supplied by Eltek during 2024.

Nano Dimension Announces Breakthrough in Materials Critical for Additively Manufactured Electronics ▸

Nano Dimension Ltd., a leading supplier of Additively Manufactured Electronics and multi-dimensional polymer, metal & ceramic Additive Manufacturing 3D printing solutions, announced a breakthrough in the development of a material that is a critical enabler for the advancement of additively manufactured electronics (AME).



Flexible Printed Circuits: A Design Primer

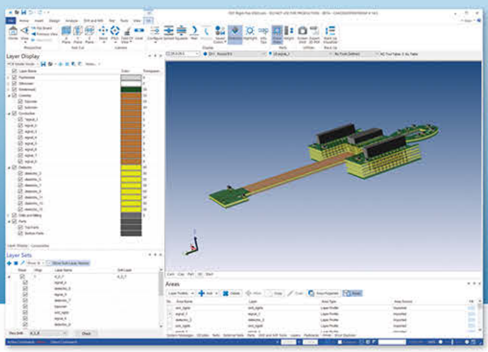
Article by Chris Keirstead
PFC FLEXIBLE CIRCUITS

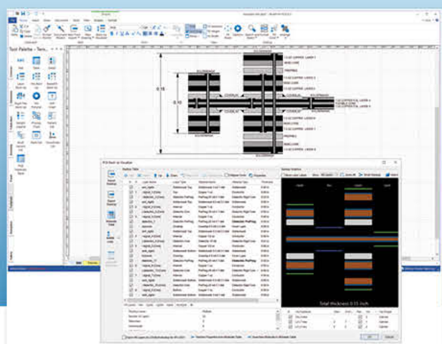
Flexible circuits consist of conductive strips in a sandwich of insulating or dielectric material. They resist moisture and contamination and are insulated from external shorts, with holes or contact surfaces for interconnection.

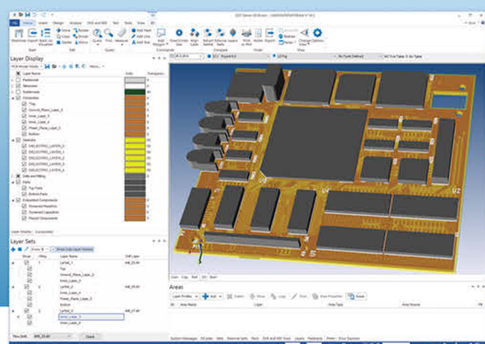
Understanding a package's electrical requirements and not over-designing permits means taking full advantage of a flexible circuit's potential compared to conventional wiring. Among the benefits are weight and bulk reduction, shorter assembly time and fewer errors, reproducible electrical characteristics, custom shielding, improved reliability, ability to interconnect moving parts, and an engineered appearance.

The mechanical and electrical characteristics of flexible circuits determine what type should be used. Total installed cost, including inspection, interconnection, fixturing and testing, must be weighed against the advantages of each:

- Single-sided flexible circuits have one layer of copper on dielectric.
- Double-sided flexible circuits have copper on both sides.
- Sculptured circuits are single- or double-sided circuits created from thick copper that allows connections such as fingers and pads to be relatively thick and very rigid extensions of the flexible conductors.
- Multilayer flexible circuits have several layers that are registered to each other and are separated by a cured layer of adhesive during lamination, with interlayer connections via plated through-holes.
- Multilayer rigid-flex is the combination of flex within and extending from rigid sections of the PCB.







There are two general areas of application that may take the designer down different paths. The first is a circuit that will be bent or formed into a rigid package during assembly. The second is where the circuit will be flexed continuously or intermittently during operation.

Insulating Materials

The choice of material must take into consideration conditions of operation and manufacture, electrical characteristics, mechanical requirements, and cost. Some materials have qualities that may make them more suitable for certain applications, but they may not be universally useful.

Kapton® is perhaps the most widely used material, dimensionally stable, and compatible with all PCB processes. It does not support combustion. It is flexible and adherable, has a high tensile strength, and about the same coefficient of expansion as copper. It does, however, absorb significant amounts of moisture.

Mylar is inexpensive, flexible, adherable, and dimensionally stable, but is sensitive to some chemicals used in PCB processing and to soldering heat.

Teflon® FEP is an excellent dielectric, does not absorb water, and is flexible and adherable, but it's not dimensionally stable and it's expensive.

Nomex® is dimensionally stable, flexible, and adherable, has high tensile strength, and resists soldering temperatures. However, Nomex reacts to processing chemicals and absorbs water.

Design Procedures

If the actual unit to use the circuit is unavailable, construct a full-size model from cardboard, sheet metal, or wood. Open the model to lay flat and place or sketch components in their required positions. Make a "paper doll" out of the circuit shape that will provide all connections and conductor runs in a size that fits the packaging constraints (Figure 1).

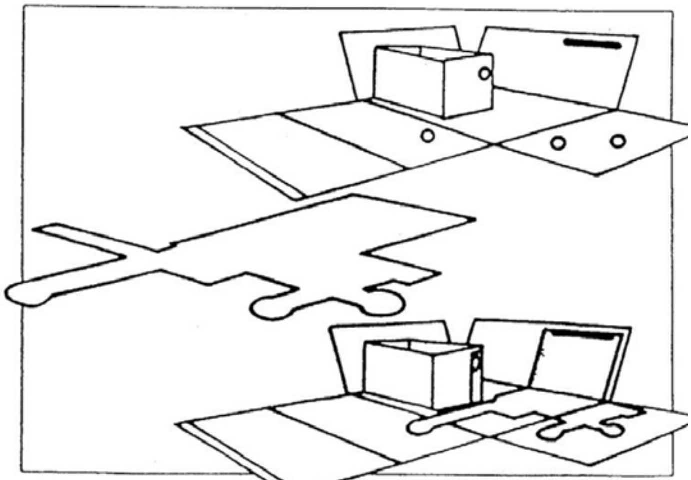


Figure 1: The physical model of the circuit and package.

Prepare a single-entry wire list showing each conductor in a continuous run to every termination point. Establish current-carrying capacity and resistivity requirements and determine copper conductor width and thickness required for current capacity and voltage drops.

Next, condense the wiring list and determine the best layout of conductor runs to minimize the required circuit layers and the circuit's mechanical area. Separate analog and digital signals to minimize crosstalk by placing them on opposite sides of the circuit or on different layers. Shielding may be necessary. With these preliminary steps completed, begin generation of specific artwork for circuit production.

Spacing between conductors is determined by the voltage between conductors (DC or AC peak volts) and ranges from a minimum of 0.005" for 15v or less to 0.020" for up to 500v. A general rule of thumb is 0.00012"/volt. Larger than minimum spacing is preferred. Routing of conductors should be as direct as possible with no nonessential overlaps that create the need for additional layers. Prepare a detailed drawing with all dimensions specified and all components positioned. Specify terminal areas without assigning pin addresses when possible. Keep edge distance as large as possible; 0.050" is recommended.

Prepare a dimensionally accurate layout. Work oversize (i.e., 4:1) for clarity. With drafting accuracy of 0.010", the 1:1 should be 0.003" or less. Leave radii for bends or folds equal to 10 to 12 times the total circuit thickness.

Use 10:1 layouts of close tolerance areas (i.e., conductor pin clusters) and reduce to layout scale. Make multiple copies of the master layout (1:1 scale) for subsequent finetuning of the layout.

The metal most commonly used in flexible circuits is rolled annealed (RA) copper with greater than 99% purity. Other materials may be used for special applications. Copper thickness is usually specified by weight per square foot, but may also be specified in linear measurements. For example: 1 oz./ft^2 = 0.0014" and 2 oz./ft^2 = 0.0028".

The resistance and current-carrying capacity of conductors are interrelated. Resistance of flat flexible conductors depends, as is the case of round wires, on cross-sectional area. Specify the final width and thickness by the desired current carrying capacity and voltage drop.

Allow for adequate heat dissipation. Flat copper conductors will dissipate heat more rapidly than round wire. The thin dielectric film of a flexible circuit results in less heat build-up than conventional wire coatings.

A range of 1-, 2-, or 3-ounce copper is typical. For 2-ounce copper, use 0.015" widths before etching for unspecified (or signal) conductors. Allow for etch loss contraction of flexible circuit layer of 1 mil/side for 1-ounce copper and 2-mil/side for 2-ounce copper (Figure 2).

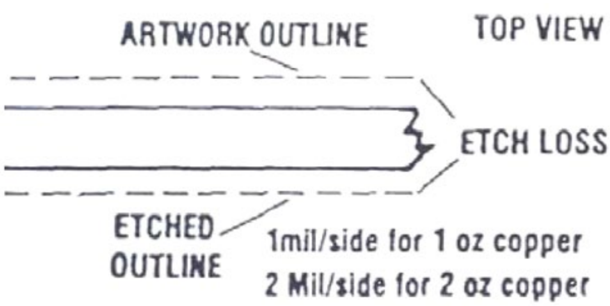


Figure 2: Etching loss allowances.

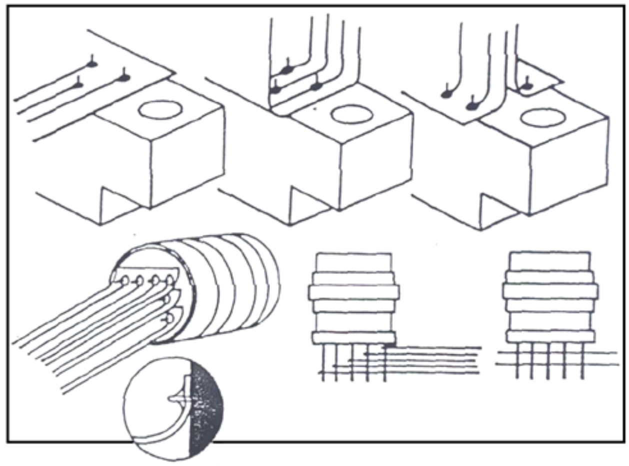


Figure 3: Methods of addressing connectors and other components.

Use 0.015" to 0.020" for conductor spacing unless the circuit requires tighter conductor packaging or uses components with high density pin clusters. Spacing of 0.005" can be produced with good artwork. To avoid conductor stresses, don't lay them over each other at bend areas and don't put them on the bias in bend areas.

Figure 3 shows some of the recommended methods of addressing components:

- Right-angle address to multi-row rectangular connectors with single layer requiring conductors to pass between pins
- Inverted, bilateral address to multi-row rectangular connectors
- Inverted address to circular connectors with straight rows
- Right-angle address to circular connectors with straight rows
- Right-angle multilayer approach to a circular connector with radial rows

Make pads as large as possible, at least twice the size of the hole for the component lead, to avoid manufacturing yield problems. If circuit densities force smaller pads, consider internal vias for sequential layers. Allow 0.008" to 0.010" clearance between the maximum pin diameter and the minimum finished hole size. Design all pads with fillets and tiedown ears to protect against pads lifting during component soldering (avoid potential shorts). The

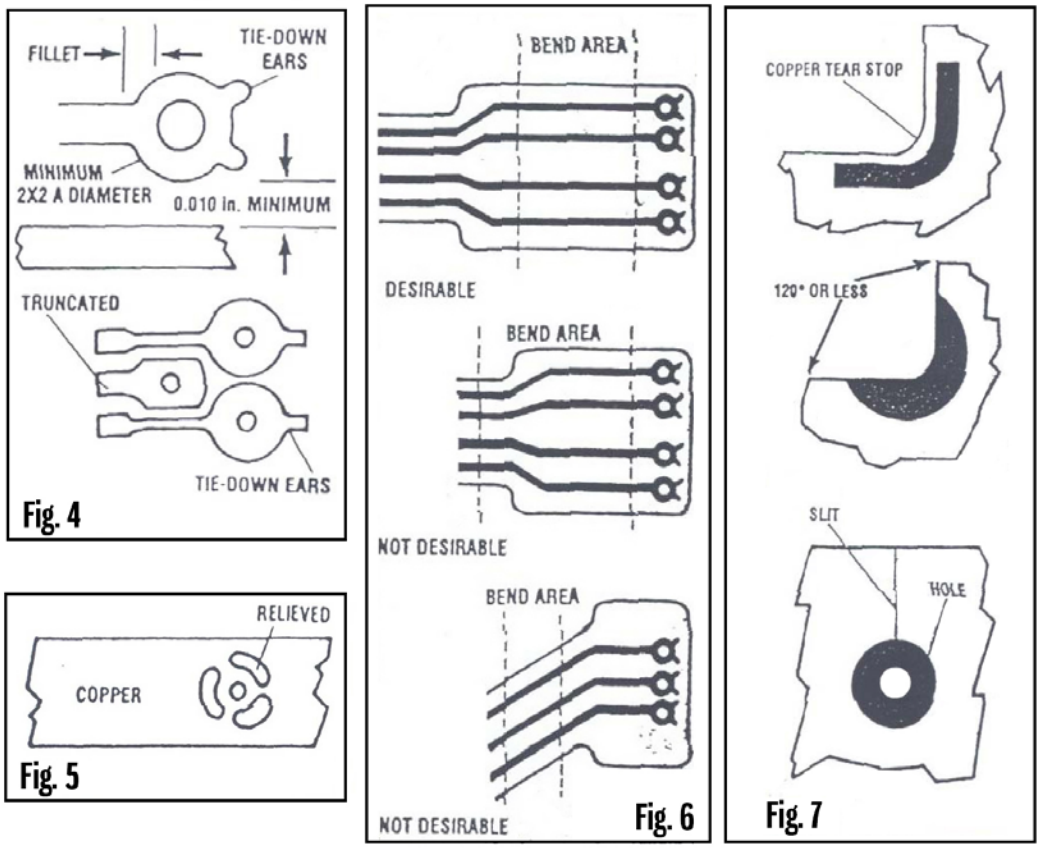


Figure 4: Pad geometry standards. Figure 5: Pad relief geometry.
Figure 6: Bend and fold geometry. Figure 7: Tear stops.

increases in pad area will reduce the chance of hole breakout, prevent stress build-up from drilling, and prevent possible conductor-to-pad interface cracks. Apply minimum spacing requirements to adjacent conductors and pads. Maintain a minimum of 0.050" from the edge of a trace to a conductor or pad and allow 0.020" for required outline tolerances, material misregistration and process tolerance buildup.

In connector areas where small center-to-center spacing between pads is used, it may be necessary to stab or truncate pads to run conductors through the pattern. Elongated pads may be used to increase solderable pad area in at least two directions and give the ability to capture the pads with the cover layer (Figure 4).

Terminal pads associated with large conductor areas (ground planes, voltage planes, heat sinks, etc.) should be relieved locally to facilitate soldering (Figure 5). Specify hole sizes with standard drill tolerances. Do not specify hole-to-pad concentricity; specify annular pad. Minimum annular on single-sided circuits (unsupported pad) should be 0.015".

The radius of a bend in a one-layer flexible circuit should not be less than 10 times the circuit thickness. Conductors should run perpendicular to fold lines. Keep them neat and uniform and add extra copper (space permitting) to help hold their folded shape (Figure 6).

Kapton tensile strength is typically 25,000 pounds for 1-mil material, but tear strength is low. Copper reinforced areas (tear stops) should be used for corners of 120 degrees or less to restrict possible damage during assembly. Glass cloth tape and FEP Teflon can be used (Figure 7).

When pads cannot have tabs or fillets, the cover-coat should lap onto the pad at least 0.005" for 270 degrees. Use slots or irregular shapes as a last resort only. Adhesives will

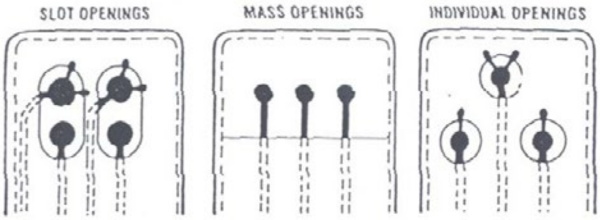


Figure 8: Coverlayer pad openings.

extrude 0.003" to 0.010" around the cover-coat opening.

A very tight hole-to-pad ratio may cause problems meeting specifications. Terminal pad baring can be done by combination but stop on individual pads. When individual pads access holes are used, their diameter should be larger than the pad diameter. Avoid reverse pad baring if possible, to reduce labor and processing costs (Figure 8). For circuits to be plated with a special finish only on the pads, all plated areas must be run to a common bus outside the circuit. This connection is severed in finishing operations.

Final refinement of conductor runs should result in tolerances and dimensions within the following parameters to result in the most economical and functional flexible circuit.

- Minimum edge distance 0.030". Design for 0.050" if space is available. Pad diameter should be at least twice through-hole diameter. Through-hole should be 0.008" to 0.010" larger than component lead diameter.
- Minimum trace-to-trace and trace-to-hole spacing of 0.010"
- Minimum conductor width of 0.010"
- Offset conductors from one side to the other to avoid an I-beam effect in fold areas

Reinforcement in key areas often is desirable to facilitate component insertion, assure mechanical strength, or obtain the selective stiffness required in some applications. Any standard board material may be used (FR-4, G10, polyamide glass). Added thickness of dielectric film will provide some stiffening and wear resistance; glass cloth tape also can be used as a stiffener. Hole diameters in reinforcement materials should be at least 0.020" larger than through-holes. Adhesives for bonding reinforcements can be the same as used in the main circuit or transfer tape can be used. A strain-relief material should be used to form a radius between the flexible circuit and stiffener materials in any sections subject to flexing (Figure 9).

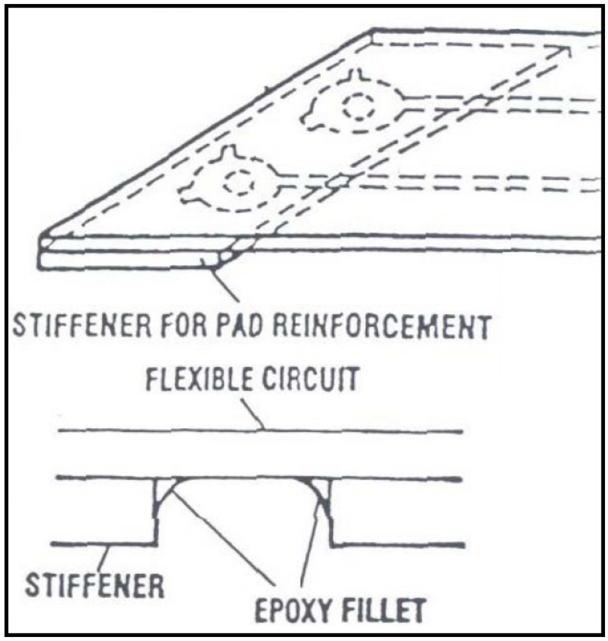


Figure 9: Stiffeners and backers.

Flexible circuits can be adapted to any connector design. Provide exact dimensional data for all connector types. Components can be soldered directly to a bared pad in the flexible circuit. Pins can be soldered into flex for direct board plug-in or for wire wraparound. Exact dimensional data is required including pin diameter, length, and spacing relative to the conductor's center. Insulation displacement terminals penetrate the insulation and are rolled over to mechanically grip the conductor. External shells plug into the crimp-on pins to serve as connectors. Wires can be wired through circuit pads or lap-soldered to circuit fingers. Gold pressure contacts or sculptured posts have limited application.

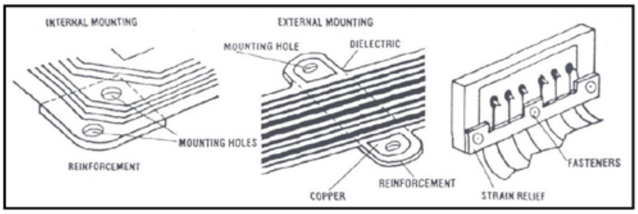


Figure 10: Mounting provisions.

Terminal areas do not normally require reinforcement since the laminated construction divides stress among all terminations. If additional strain relief is required, additional rigid areas or mounting holes for mechanical fasteners can be provided. FR-4 and G10 stiffeners can be bonded to the circuit. Terminal areas also can be potted for strain relief and environmental protection. Pinheads can be potted or covered with a laminated Kapton strip, and pin-headers can be furnished to help position fingers for easy assembly.

If necessary, secure the circuit within its package to prevent flopping and provide vibration resistance. Mounting holes can be built into the circuit for internal or external mounting (Figure 10).

For dynamic flexing 1-ounce copper is the best metal thickness. Use uniform dielectric layers, top and bottom. Provide largest possible flex radius, at least 0.25" for extended life. Flex life in excess of 1 million cycles is attainable.

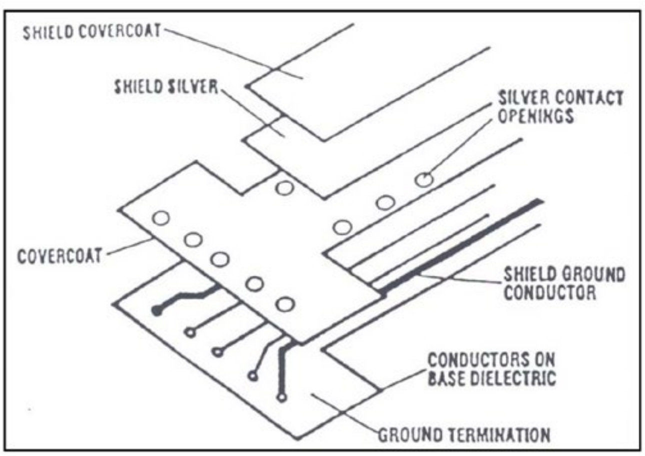


Figure 11: Sheilding techniques.

Shielding and EMI

Since flexible circuit conductors are location-fixed, designing sensitive conductors away from radiating lines can avoid the need for shielding. Grounded guard conductors can also isolate sensitive circuits and eliminate crosstalk. Thin copper foil, copper mesh foil, or silver epoxy compound are the most used materials for shielding. Limit shield use to minimize cost and maintain flexibility. Copper shields are recommended for reliability. A crosshatch pattern in artwork will increase flexibility.

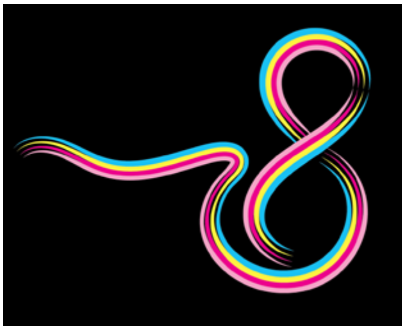
Silver epoxy, applied by spraying or silk screening is used for cost reduction and flexibility. It can terminate many points simultaneously and has excellent isolation capability. Its poor bond strength, however, limits it to outer surfaces only. Another method of shielding is copper foil with a pressure sensitive electrically conductive adhesive. Designate any areas requiring flexing.

Adding inner layer shields to multilayer circuits will increase the bend radius and reduce flexibility (Figure 11). In cases of high RF energy, video signals and digital pulses, a full 360-degree shield may be required. This can be achieved by incorporating guard conductors on the edge of the circuit. The guard conductors are exposed in the cover-layer and base dielectric at specified increments. Silver epoxy is then applied to the circuit's top and bottom, making contact at the exposed areas. The same result can be achieved with copper shields using plated through-holes to make connections to guard conductors. **DESIGN007**

Chris Keirstead is a sales manager with PFC Flexible Circuits.

TOP TEN

EDITOR'S PICKS



8 Simple Rules for Streamlining Your Design

There are many ways, dozens to be sure, and most likely many more, to streamline a PCB design. My goal here is to pick a single-digit number of rules to abide by, that can be reasonably adhered to, and provide some bang for the buck. These rules are meant to reduce design scope creep, avoid PCB respins, and improve production yields.

Dana on Data: Simplify PCB Documentation


Dana Korf

November's issue of *Design007 Magazine* had an excellent theme that evolved around design simplification. There were exceptionally good articles about how to reduce over-constrained or needlessly complex designs. One significant time-consuming category is the creation of many design files and drawings which lead to lengthy creation and interpretation time along with the considerable time to resolve conflicting or erroneous information.

The Pulse: Simplest Stackups Specified

Einstein advocated for describing complex theory in the simplest way possible, but not so simplified that key information is lost. We often see this when the media is criticised for "dumbing down" information. However, from an engineering perspective, if a design can be engineered to perform the required application in a simpler or more economical way, then simplification is truly a valuable goal.

Cadence, Autodesk Collaborate on Smart Product Design

Cadence Design Systems, Inc. announced a collaboration with Autodesk to provide solutions that accelerate intelligent system design leveraging Autodesk Fusion and Cadence® PCB solutions. This new integration offers customers seamless collaboration between electronic and mechanical engineering to accelerate the development of smart products through efficient co-design.

Avnet's Design Hub Makes Reference Designs More Accessible to Engineers

Avnet has made thousands of customizable reference designs easily accessible to engineers in the Americas in its new self-service online tool Design Hub. Design Hub is powered by AVAIL, Avnet's engineering tool with a vast reference design library that helps designers develop system-level solutions quickly and easily any time of day. The tool leverages more than 70,000 solutions to common design problems. These solutions are automatically loaded into the engineer's design based on their specific requirements.

Kris Moyer: Simplifying Your Design

It's safe to say that millions of dollars, not to mention man-hours, are wasted each year because of over-constrained, overly complicated PCB designs. Much of this is due to the increase in signal speeds and rise times, even in "mature" PCBs, and the extra cost is already part of the budget.

Insulectro: Education Begins with the Designer

During PCB West, Insulectro held an educational showcase at its office in San Jose that focused on flexible, printed electronics, and advanced materials. After the courses concluded, I spoke with Chris Hunrath, VP of technology, about the company's efforts to educate PCB designers, and the variety of material options available for customers who want to push the envelope of innovation.

PCB Carolina 2023 Breaks Attendance, Exhibitor Records

This year, PCB Carolina drew 1,200 attendees and so many exhibitors that some "overflow" booths had to be set up in a classroom near the show floor, as well as in the registration area. There was no down time on the show floor, even when classes were in session, and whenever classes would end, there was a flood of people onto the show floor. Many of the classes focused on AI, with Cadence's Taylor Hogan presenting the keynote on AI's role in PCB design.

New Materials Simplify Fab and Design Processes

During PCB West, Andy Shaughnessy and Kelly Dack met with Paul Cooke, senior director of business development, Ventec International Group. In this interview, Paul discusses some of the global trends he's seeing in new materials that address the issue of stacked microvia failure, and his drive to educate North American designers about the use of pure resin and no-flow materials.

Target Condition: What the Heck? A PCB Tech Spec Check

In 1972, I learned the adage "Measure twice, cut once" from my seventh-grade woodshop teacher, Mr. Fenoglio. To this day, I hear his voice every time I use a pencil to mark a piece of wood that I'm ready to cut. I mark it and then re-measure the edge to which it will join before sawing or drilling.

Career Opportunities

Technical Sales Manager

Gen3, based in Farnborough, UK, who designs, manufactures and distributes test equipment to minimize risk of failure in the field, has an exciting opportunity for a Technical Sales Manager to join its team to drive growth in the southern half of the UK.

Responsibilities & Experience

- Promote Gen3's and its principles' equipment.
- Identify opportunities in existing and new customers.
- Report all commercial developments related to the activity of Gen3's customers, actively seeking the specification of Gen3's products, into new projects.
- Be fully familiar with all Gen3's products, technology, USPs, features, benefits and international standards.
- Follow up all enquiries for products and services; convert them into contracts/orders.
- Provide technical support – remotely and onsite.
- Be widely recognised and acknowledged as an "Industry Expert."
- Technical Sales and Account Management skills from an electronics background is desirable.
- Excellent sales, customer service, communication, presentation and negotiation skills.
- Recognised qualification in Electronics Engineering or related field.
- Knowledge of the electronics/SMT assembly process.
- Excellent written and verbal communication skills in English.
- Competent user of Microsoft Office applications.
- Ideally living in the Southern half of the UK.
- Willing and able to travel within and outside UK.
- A full, clean UK driving license is essential.

To apply, please contact John Barraclough at john.barraclough@gen3systems.com or by using the link below.

apply now

Senior Sales Representative

Ventec Central Europe

Location: Kirchheimbolanden, Germany/Remote

We are looking for a self-motivated Senior Sales Representative—Ventec Central Europe, ideally with experience in the PCB industry. This position requires significant selling experience (15+ years) in the electronics and PCB industries. Candidates must possess a proven & consistent history of proactive sales growth with OEM customers. Most notably, they must be able to connect with OEM contacts that have decision-making capabilities.

Key Responsibilities

- Promote, sell, and close business for all Ventec product lines with focus on key OEM and PCB manufacturing customers.
- Track projects and submit monthly updates to management.
- Coordinate cross-functional resources when applicable.
- Assist in coordination and set-up of relevant trade show events.
- Assist in strategic planning initiatives.
- Assist in market and customer intelligence gathering.
- Recommend pricing strategies.

Job Requirements

- Entrepreneurial spirit, positive, high energy, and desire to win.
- Proactive and self-motivated work strategy to develop and win business for all business units.
- Excellent written and oral communication skills in German and English
- Excellent computer skills (Microsoft Office, especially Excel).
- Proven track record securing new business at OEM accounts.

Please apply in the strictest confidence, enclosing your CV, to: accountingde@ventec-europe.com

apply now

Career Opportunities

Technical Support Engineer

USA Region

ViTrox aims to be the world's most trusted technology company in providing innovative, advanced, and cost-effective automated Machine Vision Inspection Solutions for the semiconductor and electronics packaging industries. Located in Hayward, California, ViTrox Americas Inc. is actively looking for talent to join our expanding team.

Key Responsibilities:

- Delivering excellent and creative problem-solving skills for servicing, maintaining, machine buy-off, and troubleshooting advanced vision inspection machines at customer sites. Providing remote customer support to minimize machine downtime.
- Cultivating strong customer relationships and ensuring comprehensive customer service to drive repeat orders and support business development in machine evaluation.
- Proactively understanding customer needs and feedback to drive continuous improvement in existing technologies and new product development.

Qualifications & Requirements:

- A recognized diploma/advanced diploma/degree in Science and Engineering, preferably in Electrical & Electronics/Computer Science/Computer Studies or equivalent.
- 3+ years of relevant experience in servicing automated inspection equipment (SPI, AOI, and AXI).
- Strong communication and troubleshooting skills.
- Willingness to travel extensively across the USA.
- Positive attitude and flexibility to accommodate conference calls with headquarters.
- Applicants from the USA and Canada are welcome to apply.
- Training will be provided at our headquarters in Penang, Malaysia.

apply now

The Test Connection, Inc.

Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/ Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

apply now

Career Opportunities

TAIYO AMERICA

Europe Technical Sales Engineer

Taiyo is the world leader in solder mask products and inkjet technology, offering specialty dielectric inks and via filling inks for use with microvia and build-up technologies, as well as thermal-cure and UV-cure solder masks and inkjet and packaging inks.

PRIMARY FUNCTION:

1. To promote, demonstrate, sell, and service Taiyo's products
2. Assist colleagues with quotes for new customers from a technical perspective
3. Serve as primary technical point of contact to customers providing both pre- and post-sales advice
4. Interact regularly with other Taiyo team members, such as: Product design, development, production, purchasing, quality, and senior company managers from Taiyo group of companies

ESSENTIAL DUTIES:

1. Maintain existing business and pursue new business to meet the sales goals
2. Build strong relationships with existing and new customers
3. Troubleshoot customer problems
4. Provide consultative sales solutions to customer's technical issues
5. Write monthly reports
6. Conduct technical audits
7. Conduct product evaluations

QUALIFICATIONS / SKILLS:

1. College degree preferred, with solid knowledge of chemistry
2. Five years' technical sales experience, preferably in the PCB industry
3. Computer knowledge
4. Sales skills
5. Good interpersonal relationship skills
6. Bilingual (German/English) preferred

To apply, email: BobW@Taiyo-america.com with a subject line of "Application for Technical Sales Engineer".

apply now

BLACKFOX
Premier Training & Certification

IPC Instructor

Longmont, CO

This position is responsible for delivering effective electronics manufacturing training, including IPC certification, to adult students from the electronics manufacturing industry. IPC Instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC certification programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will primarily conduct training at our public training center in Longmont, Colo., or will travel directly to the customer's facility. It is highly preferred that the candidate be willing to travel 25–50% of the time. Several IPC certification courses can be taught remotely and require no travel or in-person training.

Required: A minimum of 5 years' experience in electronics manufacturing and familiarity with IPC standards. Candidate with current IPC CIS or CIT Trainer Specialist certifications are highly preferred.

Salary: Starting at $30 per hour depending on experience

Benefits:

- 401k and 401k matching
- Dental and Vision Insurance
- Employee Assistance Program
- Flexible Spending Account
- Health Insurance
- Health Savings Account
- Life Insurance
- Paid Time Off

Schedule: Monday thru Friday, 8–5

Experience: Electronics Manufacturing: 5+ years (Required)

License/Certification: IPC Certification–Preferred, Not Required

Willingness to travel: 25% (Required)

apply now

Career Opportunities

Prototron Circuits

Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB manufacturer located in Tucson, AZ, is looking for sales representatives for the Utah/Colorado, and Northern California territories. With 35+ years of experience, our PCB manufacturing capabilities reach far beyond that of your typical fabricator.

Reasons you should work with Prototron:

- Solid reputation for on-time delivery (98+% on-time)
- Capacity for growth
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- 5-day standard lead time
- RF/microwave and special materials
- AS9100D
- MIL-PRF- 31032
- ITAR
- Global sourcing option (Taiwan)
- Engineering consultation, impedance modeling
- Completely customer focused team

Interested? Please contact Russ Adams at (206) 351-0281 or russa@prototron.com.

apply now

KYZEN

Where Science and Care Converge.

Regional Manager

Southwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the Southwest Region. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deploy-ment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
  - Reviews progress of sales performance
  - Provides quarterly results assessments of sales reps' performance
  - Works with sales reps to identify and contact decision-makers
  - Setting growth targets for sales reps
  - Educates sales reps by conducting programs/seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

apply now

Career Opportunities

Career Opportunities

KOH YOUNG AMERICA

Technical Service & Applications Engineer

Full-Time — Flexible Location

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement-based inspection technology for electronics manufacturing. Located in Duluth, GA, Koh Young America has been serving its partners since 2010 and is expanding the team with an Applications Engineer to provide helpdesk support by delivering guidance on operation, maintenance, and programming remotely or on-site.

Responsibilities

- Provide support, preventive and corrective maintenance, process audits, and related services
- Train users on proper operation, maintenance, programming, and best practices
- Recommend and oversee operational, process, or other performance improvements
- Effectively troubleshoot and resolve machine, system, and process issues

Skills and Qualifications

- Bachelor's in a technical discipline, relevant Associate's, or equivalent vocational or military training
- Knowledge of electronics manufacturing, robotics, PCB assembly, and/or AI; 2-4 years of experience
- SPI/AOI programming, operation, and maintenance experience preferred
- 75% domestic and international travel (valid U.S. or Canadian passport, required)
- Able to work effectively and independently with minimal supervision
- Able to readily understand and interpret detailed documents, drawings, and specifications

Benefits

- Health/Dental/Vision/Life Insurance with no employee premium (including dependent coverage)
- 401K retirement plan
- Generous PTO and paid holidays

apply now

ARLON ELECTRONIC MATERIALS

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- Engineering
- Quality
- Various Manufacturing

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

apply now

Career Opportunities

Career Opportunities

eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

apply now

American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

apply now

Career Opportunities

APCT
Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

apply now

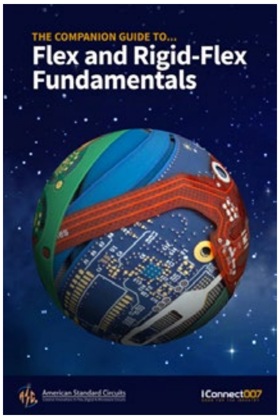
YOUR JOB AD HERE

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (PACIFIC)

I-Connect007
GOOD FOR THE INDUSTRY

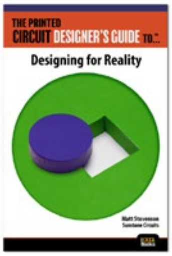
Educational Resources

THE COMPANION GUIDE TO... FLEX AND RIGID FLEX FUNDAMENTALS



I-Connect007 and American Standard Circuits are proud to announce the launch of the companion guide to the immensely popular *The Printed Circuit Designer's Guide to... Flex and Rigid-flex Fundamentals.* This short guide, written by topic experts at American Standard Circuits, is designed to provide additional insights and best practices for those who design or utilize flexible and/or rigid-flex circuit boards. Topics covered include trace routing options, guidelines for process optimization, dynamic flexing applications, rigid-to-flex transition and more. Visit I-007ebooks.com to download your copy.

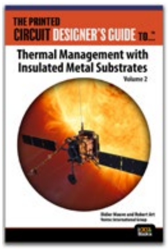
I-007eBooks The Printed Circuit Designer's Guide to...



Designing for Reality

by Matt Stevenson, Sunstone Circuits

Based on the wisdom of 50 years of PCB manufacturing at Sunstone Circuits, this book is a must-have reference for designers seeking to understand the PCB manufacturing process as it relates to their design. Designing for manufacturability requires understanding the production process fundamentals and factors within the process. **Read it now!**



Thermal Management with Insulated Metal Substrates, Vol. 2

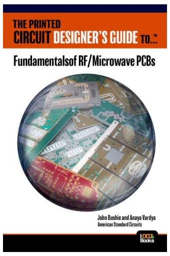
by Didier Mauve and Robert Art, Ventec International Group

This book covers the latest developments in the field of thermal management, particularly in insulated metal substrates, using state-of-the-art products as examples and focusing on specific solutions and enhanced properties of IMS. **Add this essential book to your library.**

High Performance Materials

by Michael Gay, Isola

This book provides the reader with a clearer picture of what to know when selecting which material is most desirable for their upcoming products and a solid base for making material selection decisions. **Get your copy now!**



Fundamentals of RF/Microwave PCBs

by Anaya Vardya and John Bushie, American Standard Circuits

Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.

Our library is open 24/7/365. Visit us at: I-007eBooks.com

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

EDITOR | COLUMNIST COORDINATOR: **MICHELLE TE**
michelle@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **DAN FEINBERG**
baer@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **HAPPY HOLDEN**
(616) 741-9213; happy@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 365-1727; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

ART DIRECTOR/PRODUCTION MGR. **SHELLY STEIN**
shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA, TOBEY MARSICOVETERE**

TECHNOLOGY SPECIALIST: **BRYSON MATTIES**

COVER DESIGN: **SHELLY STEIN**

COVER IMAGE: **ADOBE STOCK © CHAOTICDESIGNSTUDIO**

DESIGN007 MAGAZINE

DESIGN007 MAGAZINE®
is published by IPC Publishing Group, Inc.
3000 Lakeside Dr., Suite 105N, Bannockburn, IL 60015

December 2023, Volume 12, Number 12
DESIGN007 MAGAZINE is published monthly
by IPC Publishing Group, Inc., dba I-Connect007

ADVERTISER INDEX

Problems solved!
PCB007 MAGAZINE
SEPTEMBER 2023
FINDING ULTRA
PCB007 MAGAZINE
OCTOBER 2023
PCB007 MAGAZINE
Registration Sweet Spot
DESIGN007 MAGAZINE
OCTOBER 2023
DESIGN007 MAGAZINE
NOVEMBER 2023
DESIGN007 MAGAZINE
DECEMBER 2023
ODD GEOMETRIES
OCTOBER 2023
SMT007 MAGAZINE
NOVEMBER 2023
ATTRACTING NEW TALENT
SMT007 MAGAZINE
DECEMBER 2023
ECONOMIC HEADWINDS
SUBSCRIBE NOW