I-Connect007

DECEMBER 2024

DESIGN007 MAGAZINE

Advanced Packaging and Stackup

Kris Moyer
Instructor, IPC

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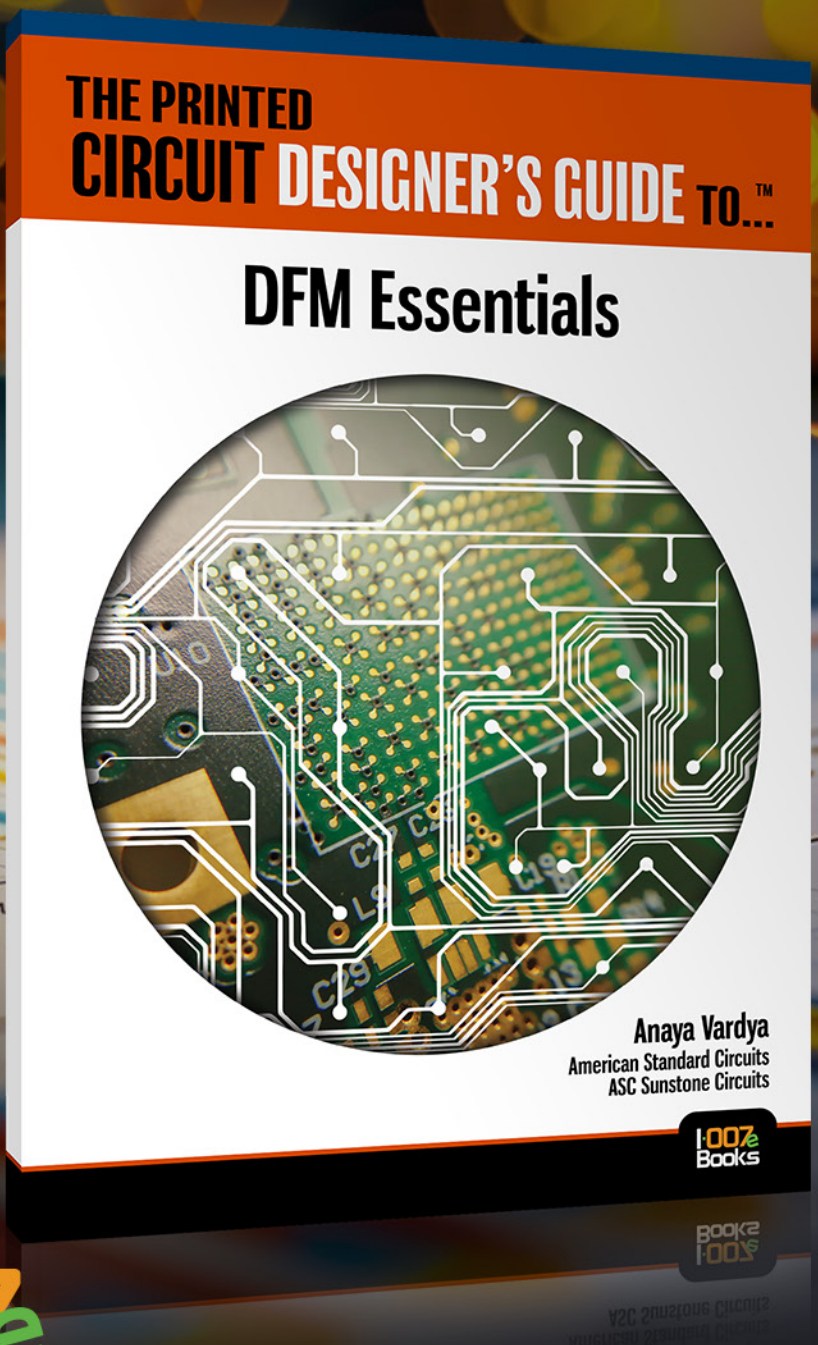

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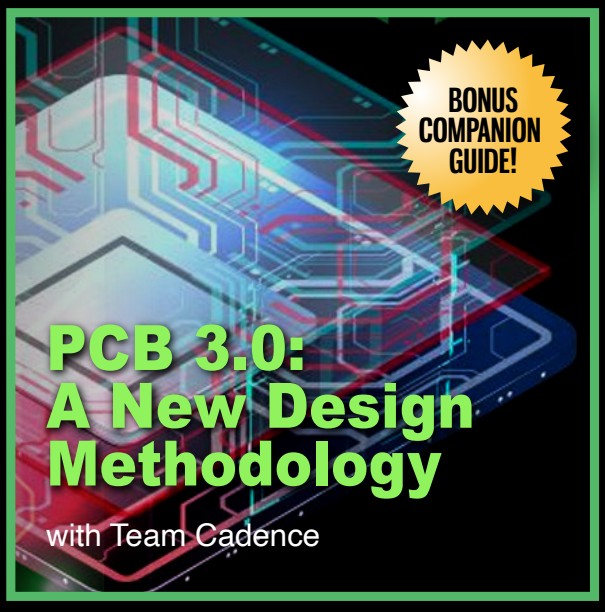

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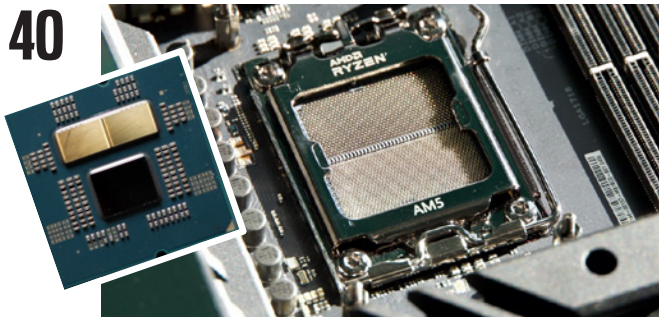
DESIGN007 MAGAZINE

Advanced Packaging and Stackup Design

This month, expert contributors discuss the impact of advanced packaging and stackup design—from SI and DFM challenges through the variety of material tradeoffs that designers must contend with in HDI and UHDI. We learn that with a little research, planning, and collaboration with the fabricator, any seasoned PCB designer can utilize advanced packaging.



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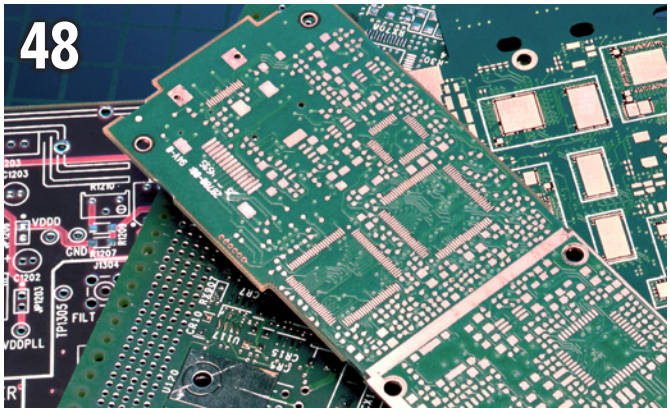

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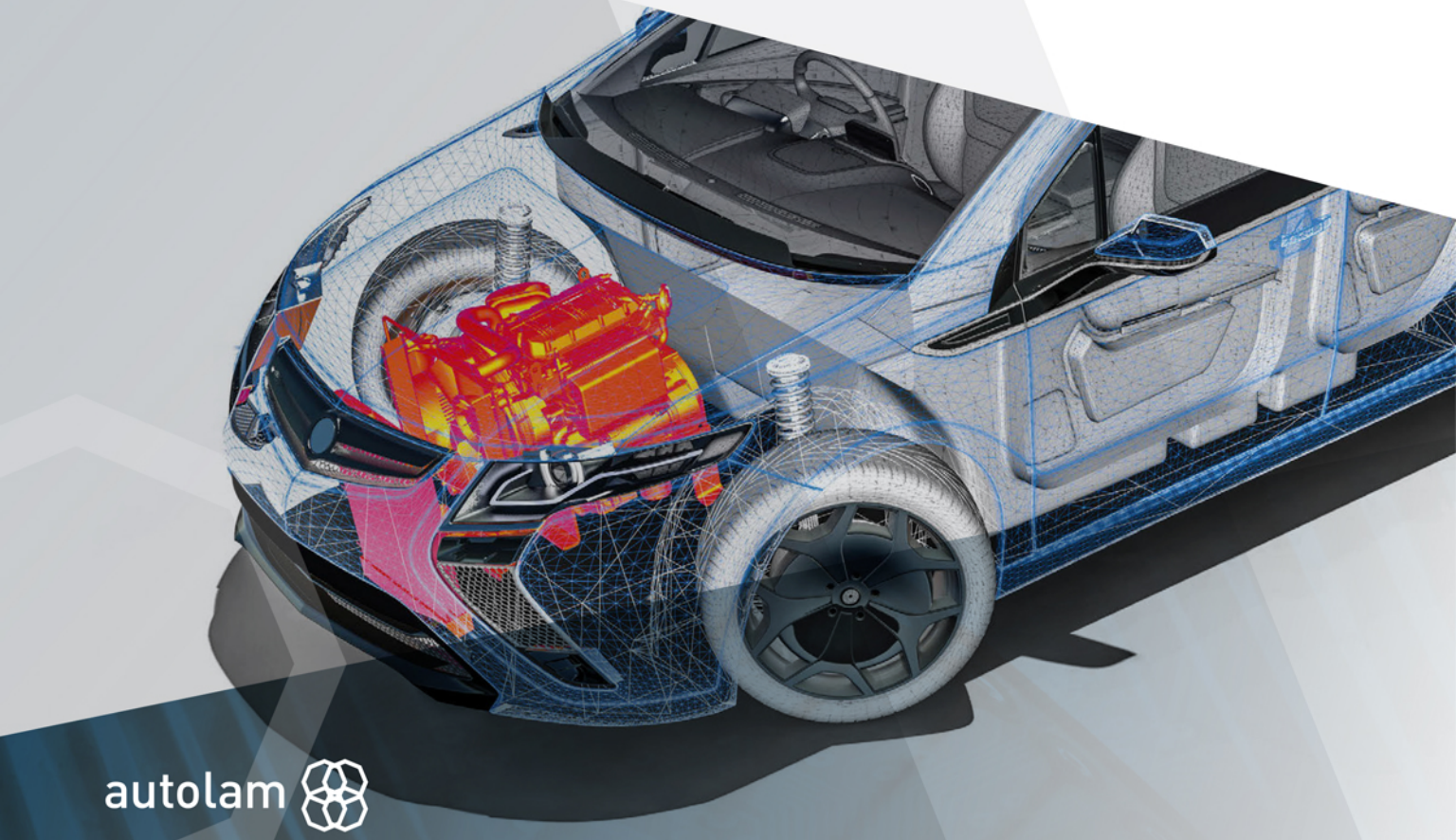

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A Stack of Advanced Packaging Info

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

It's holiday time again. Where did the year go? I actually have a jump on decorating—I never took the mistletoe off my mantel.

So it's only fitting that this issue on advanced packaging and stackup features a "stackup" of "packages" on the cover. There's certainly a lot to "unpack" in this issue. (Okay, I'll stop.)

As advanced packaging moves further into the mainstream of PCB design, more PCB designers and design engineers are realizing this isn't a plug-and-play technology. As we see in this issue, advanced packaging can have an impact on the entire design—the stackup in particular.

Advanced packages usually require HDI or UHDI technology, which demands sequential lamination. When designing boards with advanced packages, designers must choose materials that can withstand multiple lamination thermal cycles. These high-speed materials are ultra-thin and without reinforcement, which can lead to challenges with layer-to-layer misregistration. Sequential lamination requires plating on the inner layers. It all adds up to more potential DFM issues during fabrication.

But with a little research, planning, and collaboration with the fabricator, any seasoned

PCB designer can utilize this technology. With the constant demand for ever-smaller electronic devices, advanced packaging might be exactly what designers need.

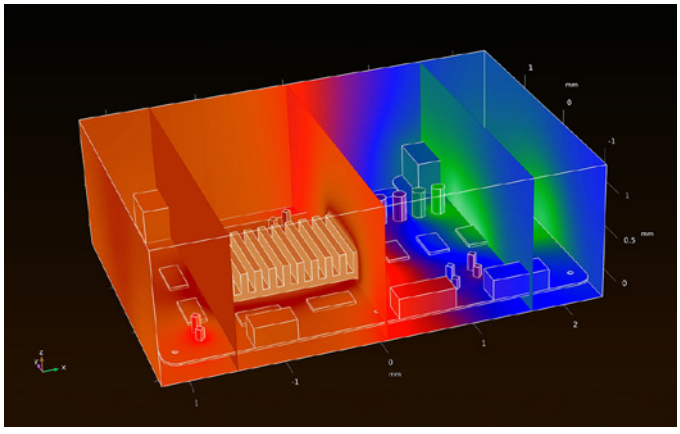
This month, we asked our expert contributors to discuss the impact of advanced packaging and stackup design—from SI and DFM challenges through the variety of material tradeoffs that designers must contend with in HDI and UHDI. Kris Moyer kicks us off with a conversation about the complex interrelationship between advanced packaging and stackup design. Cherie Litson explains why many old rules no longer apply, particularly regarding stackup, HDI, and UHDI.

Columnist Barry Olney covers an interesting idea: AI-driven inverse stackup optimization. Columnist Kelly Dack discusses advanced packaging through the view of the Gartner Hype Cycle methodology; that's a new one for me. Columnist Vern Solberg takes a deep dive into the current and emerging semiconductor and material technologies that can affect stackup design.

We also have an interview with IPC's Peter Tranitz, who discusses the new Pan-European Electronics Design Conference, set for Vienna, Austria in January. Anaya Vardya brings us part two of his series on UHDI bleeding-edge manufacturing applications, and we have columns from our regular contributors Matt Stevenson and Joe Fjelstad.

I hope you all get to spend time with your families during the holidays. You deserve some time off. **DESIGN007**

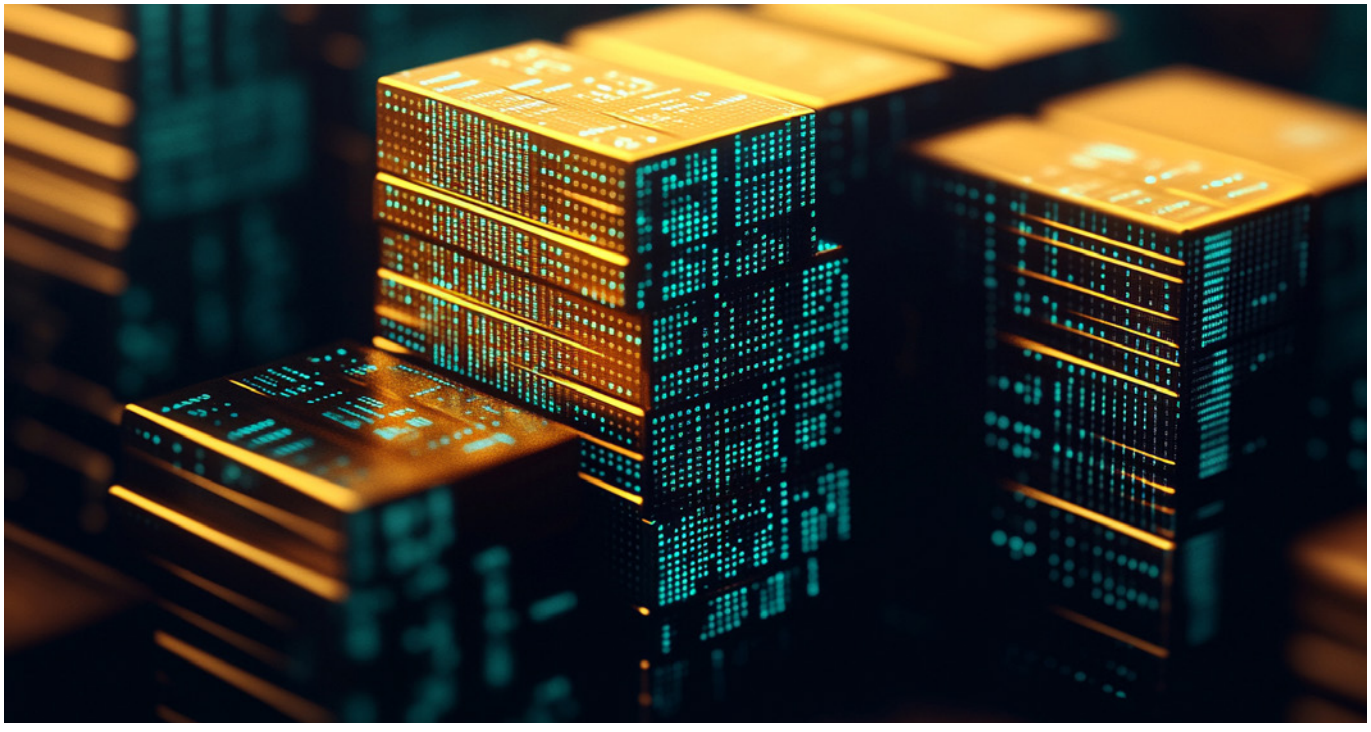
Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 23 years. To read past columns, click here.



Dana on Data: Merging 2D Electrical, 3D Mechanical Worlds

Imagine the day when placing components and routing signal traces and power planes are not constrained by 2D PCB fabrication processes and materials. Astronauts working on the space station have equipment mounted on all axes. They are not constrained by having to stand on a flat surface. They already have a 3D printer at the space station. Why can't we create PCBs in a 3D space?

With additive manufactured electronics (AME) and printed electronic (PE) technologies, reviewing the schematic and component placement routing strategies can utilize all three X, Y, and Z axes. Components can be additively formed using the interconnect materials. Traces and power distribution can be configured with unique shapes and routes on any angle, with the cross-section varying along its path, if required. Die and packaged components could conceptually be mounted on or under non-planar surfaces. Multiple conductor and dielectric materials are simultaneously being deposited to create the PCB. There are several additive manufacturing (AM) generic processes available and a multitude of potential hybrid approaches. New techniques are developed every year, being driven by 3D-minded designers and researchers...continue reading.



Effects of Advanced Packaging and Stackup Design

Feature Q&A with Kris Moyer

Kris Moyer teaches several PCB design classes for IPC and Sacramento State, including advanced PCB design. His advanced design classes take on some really interesting topics, including the impact of a designer's choice of advanced packaging upon the design of the layer stackup.

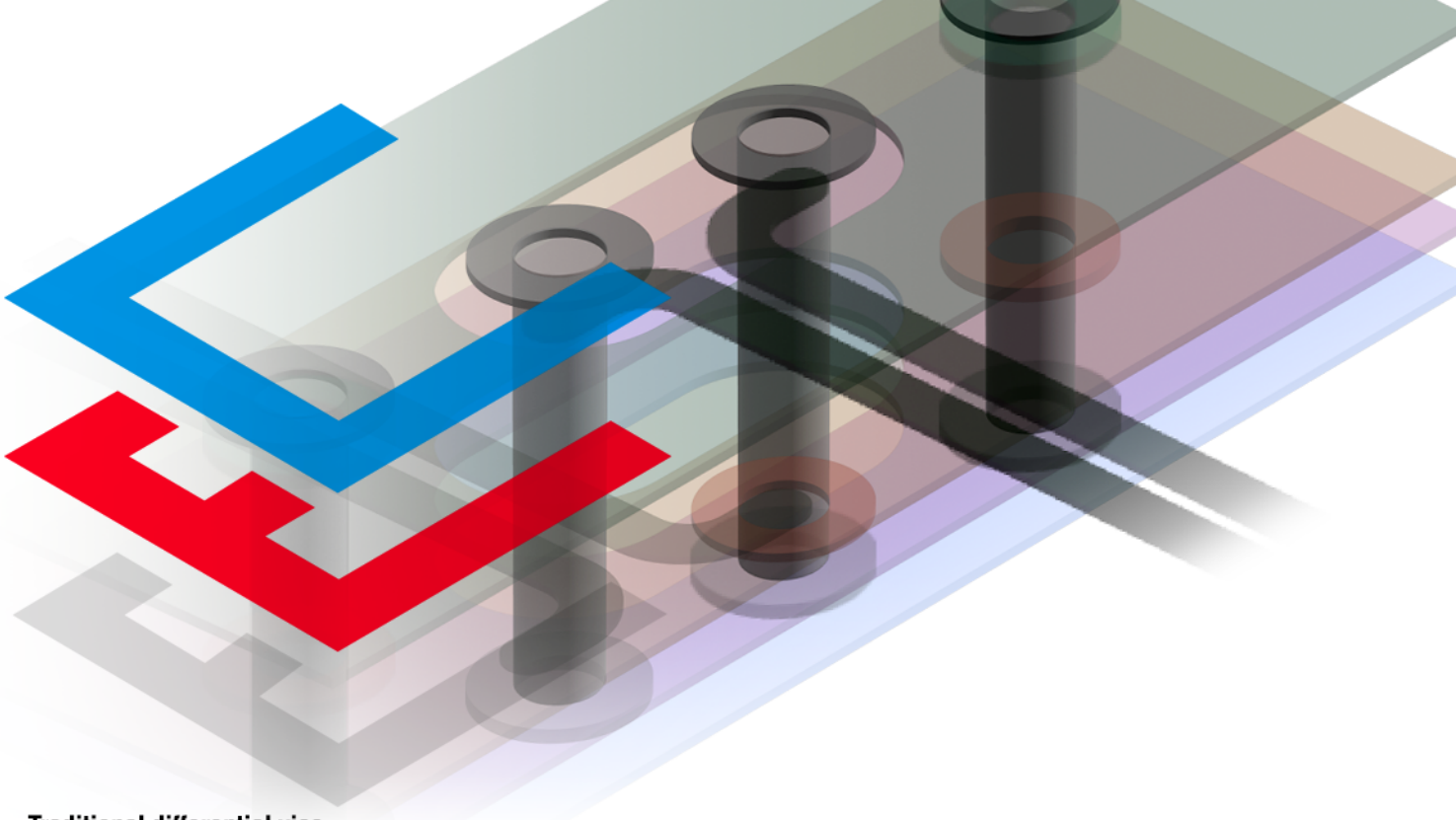
Kris shares his thoughts on the relationship between packaging and stackup, what PCB designers need to know, and why he believes, "The rules we used to live by are no longer valid."

Kris, tell us how advanced packaging can impact stackup design. What challenges do designers need to be aware of?

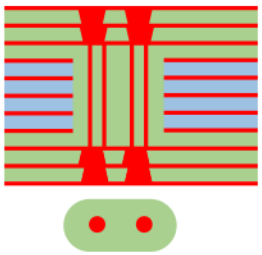
Kris Moyer: With advanced packaging you usually need to use HDI or UHDI technology. This usually means sequential lamination. With sequential lamination you need to select materials that can survive multiple lamination thermal cycles.

When we were discussing advanced packaging and stackup design recently, you said, "The rules we used to live by are no longer valid." Expand on that a little bit.

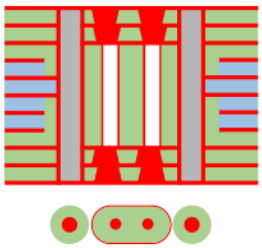
As I mentioned, your selection of materials is now further restricted by the need for materials that survive multiple lamination cycles. Additionally, since we are adding layers one at a time and need plating on all layers, not just the outer layers, the copper design is now more difficult. Also, since we are adding layers one at a time, we can now have some select



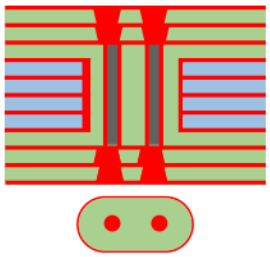
Traditional differential vias



Standard coaxial differential vias



Coaxial differential vias to overcome signal issues of buried vias



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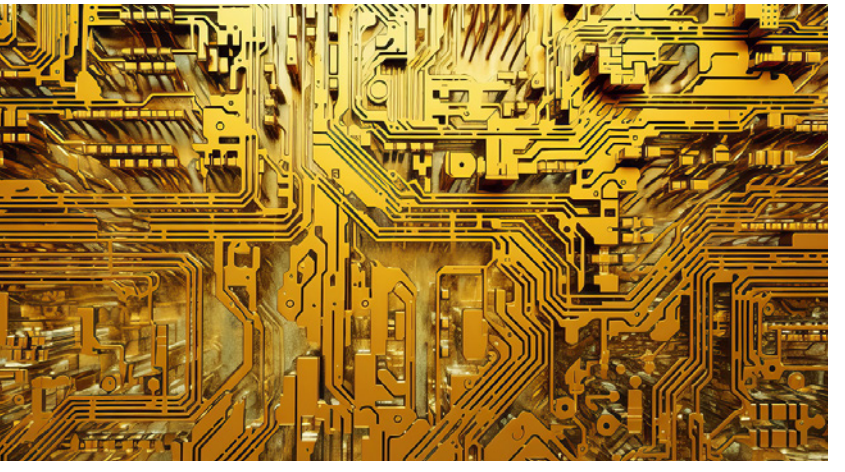
instances of unbalanced Z-axis and still meet bow and twist constraints. Furthermore, many of the ultra-thin dielectric layers used in HDI/UHDI are just resin-coated copper without any reinforcement, so CTE/FA can be more of an issue.

What are some of the trade-offs—DFM, SI, materials, etc.—that designers need to navigate when designing a stackup with advanced packages?

I touched on this in the last question. When it comes to DFM, since the layers are added one at a time and often those layers don't have reinforcement materials, there is the potential for more layer-to-layer misregistration during lamination. From an SI point of view, there is now plating on all layers and the tolerance on the plating will need to be considered on impedance calculations.



How does our choice of via construction come into play?

The various via types all have their own trade-offs. Stacked vias, for example, take up less board space but require the extra process steps of plug, cap, and planarize in order to make the layer-to-layer connection. Staggered vias, on the other hand, do not require the extra process steps but may have entrapped contaminants in air voids that could lead to other issues during assembly if there is not enough resin in the layer to fully fill the via during lamination.

As chip packages shrink, they create all sorts of follow-on issues such as energy concentration, smaller vias, etc. What other challenges does this create?

The biggest challenge with very small package sizes is the need to use much thinner copper to fabricate the necessary feature sizes. This creates a snowball effect; when the same surface finish used for thick coppers is used on thin coppers, this can lead to increased impact on skin effect for signal propagation. Decreased adhesion if surface roughness is reduced and less margin for over current/thermal issues is another issue that happens with the use of thinner coppers. These are just a few of the issues faced.

What DFM issues are fabricators looking for in this situation, and what can designers do to stay ahead of the game?

As I mentioned, the need for thin coppers and microvias puts the fabricator on the lookout for several issues. First, has the stackup and increased layer-to-layer misregistration been considered? Second, using very thin coppers limits the amount of oxide treatment/surface roughness that can be added to the copper, so the resin-to-copper adhesion will not be as robust. Third, has the designer accounted for plating on the inner layers needed for sequential lamination? Fourth, has the stackup/material selection accounted for the need for multiple lamination cycles? These are just some of the big hitters that fabricators are looking for with HDI/UHDI designs.

Is there anything else you'd like to add?

While the challenges presented here do make HDI/UHDI a bit more complex than traditional designs, the benefits of reduced package/product size, increased design capability, and need to use smaller package sizes makes the reward worth the risk. With the proper knowledge, training, and partnership with your fabricator, any designer can create a successful, robust HDI/UHDI PCB design. **DESIGN007**

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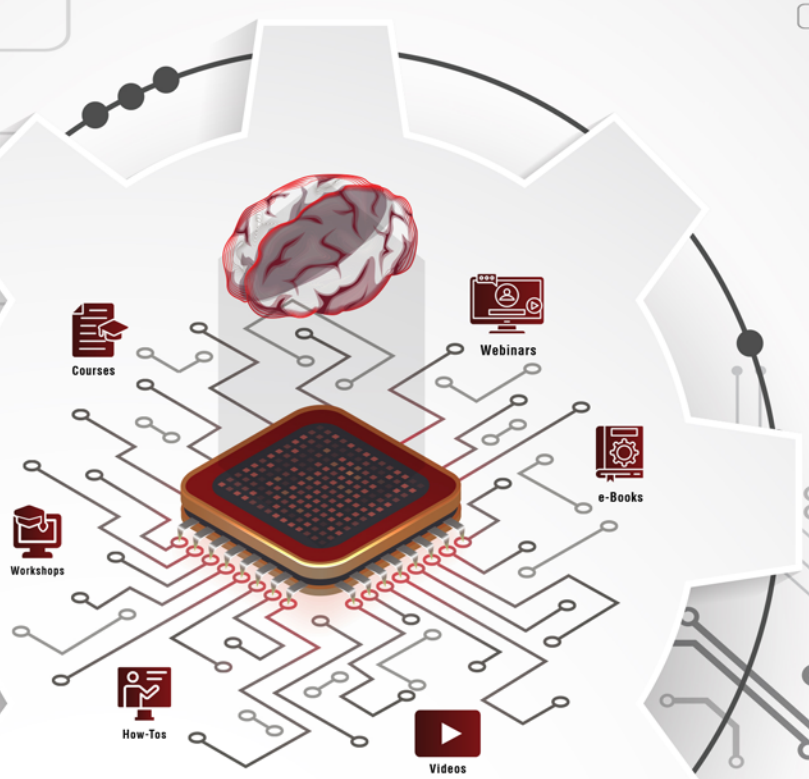

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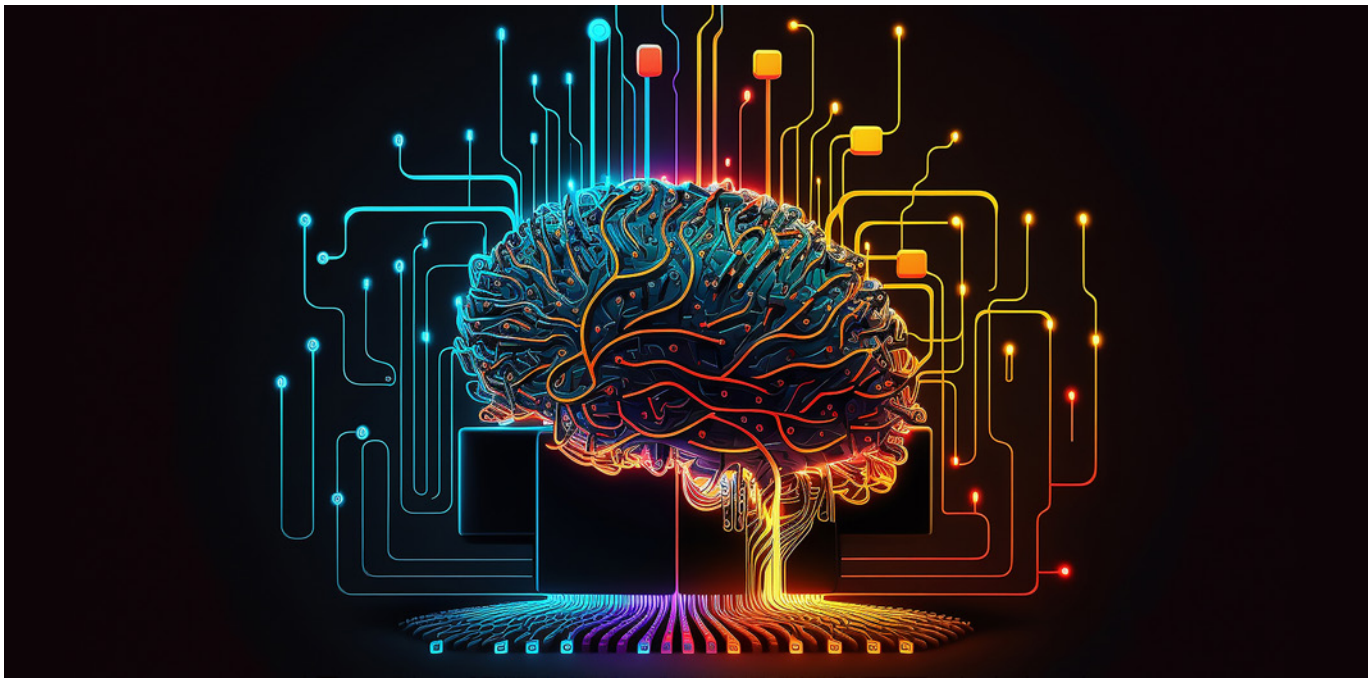

Are Our Stackup Rules No Longer Valid?

Feature Article by Cherie Litson
EPTAC MIT CID/CID+

Are the stackup rules we used to follow no longer valid? It depends on what you're designing. Electrical rules change depending on your circuit. Fabrication rules change depending on which fabricator you're working with. Today, we just have more options, and sometimes, cost is a bigger rule than anything else.

If you search online for information about layer stackups, trace widths, and hole sizes in PCBs, you'll find a variety of resources. The trick is to first define your electrical and mechanical requirements, then work with your fabricator to find the savings (i.e., profits) for both the customer and fabricator.

So, how do you navigate all the rules? First, keep learning. Get certified through the CID and CID+ exams. Go to conferences such as IPC APEX EXPO, SMTAI, and PCB West. Stay up to date through trade publications, such as *Design007* and *PCB007 Magazine*.

If cost is not an issue, and you have an in-house fabrication and assembly shop, you can experiment with all kinds of options. Just be sure to research the physics so you don't hurt yourself or others.

If cost is a factor (as it is for most of us) and you are sending the design out to find the lowest cost for fab and assembly, you may need to follow the guidelines a bit more diligently. You can still be creative but understand the tradeoffs for what you want to do. Work with the fabricator(s) you select and find out what's possible within your budget. Use the IPC-1730 and IPC-1720 specifications to be sure you've

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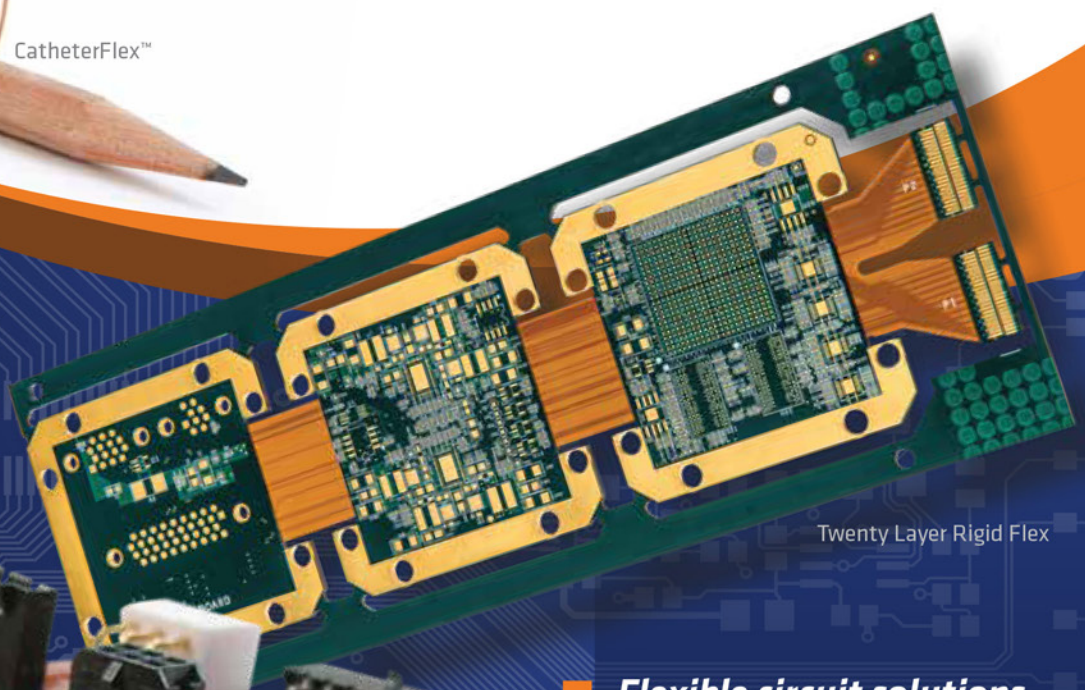

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asked the fabricator and assembler all the right questions. The things that are called out are somewhat customizable per fabricator, and using these specs will help you get consistent answers and fabrication price quotes.

Hole sizes and aspect ratios, component pin spacing, and product sizes are getting smaller all the time. How can we navigate the demands of these conditions with the existing manufacturing processes that exist out there?

Speaking of rules, more and more people are using AI as a starting point for their ideas, so I asked AI for an overview for PCB stackups. As you might guess, AI doesn't get everything right. I've listed the AI rules (in italics) followed by my comments and corrections along with a few other tidbits:

Sequential layer arrangement: *Alternate layers of signal, ground, and power planes to reduce electromagnetic interference (EMI).*

EMI is noise. So, this is a good start. However, many designs don't have a power plane due to the multiple power levels in the same IC. If you find there is one power level that is common to all ICs, then use that as a power plane. Otherwise:

- Convert one or more signal layers into a power puddle layer.
- Take a little time to group components with similar power levels in the same general areas.
- Really look at all signal return paths. The power puddle layer(s) cannot be used as a return path. It's now a signal layer.
- Add more GND layers if needed.
- Flood ground on the signal layers and add stitching vias.

Signal layer placement: *Place signal layers below the ground plane for tight coupling. Keep high-speed signals close to the ground plane to reduce noise.*

This is not quite right. It really doesn't matter if the signal is above or below the ground plane, just keep the distance as close as possible to reduce noise (EMI). In a four-layer board, keep the planes close to the signals, not each other. You won't get enough capacitance from them anyway. Use them to dampen the EMI.

Power and ground planes: *Maintain a minimum distance between power and ground planes. Don't split the power plane.*

Yes, this is true in any situation. If you have to split the power plane, don't use it for a signal return layer, or don't run your signal across the split on an adjacent layer.

Symmetry: *Build a symmetrical stackup of the top and bottom layers.*

This is not quite right. The more accurate statement would be to build a symmetrical stack-up from the center of the stackup toward the top and bottom of the board.

Sometimes this is not possible due to the electrical requirements. For uneven stackups,

be prepared for bow and twist (physics) at assembly, as an uneven stackup will create CTE stresses during the assembly process. You may need to factor in a stiffener, special fixtures, and handling at assembly as in the case of the boards getting hot during normal function.

***Layer thickness:** The thickness of each signal layer is a crucial factor.*

Again, this is not quite right. Instead, it should be: "When specific impedance is required for the signals, the layer thickness between the signal and its return path becomes an important factor." Be sure to communicate all impedance needs to your fabricator in your documentation.

Layer thicknesses also affect aspect ratios of blind and buried vias.

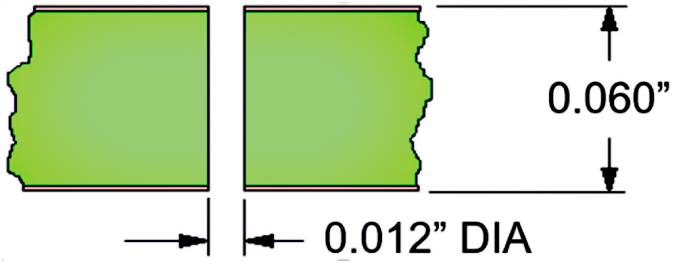
***Material:** The material of the layers affects the dielectric constant and loss tangent.*

Yes, it does. There are three parts to the material that create changes: resin, reinforcement, and metal (mostly copper). There are many great programs for engineers and designers used to calculate these factors. Some are from the material suppliers themselves. That said, don't be too specific with your fabricator. There are a couple of things to remember about specifying materials for your board:

- Is this material that your fabricator stocks or will they need to special order it?
- Have they successfully used this type of material before?
- Many material specifications change slightly from batch to batch.
- Will the material influence the assembly of the board? If so, in what way?

***Drill size and aspect ratio:** The selection of drill size and aspect ratio affects the layer count, routing density, and mechanical stability of the board.*

This is not quite right. Aspect ratio is the drill size divided by the thickness the drill has to travel: Aspect ratio: 0.060"/0.012" = 5:1



Calculating aspect ratio.

Layer count doesn't come into play unless it makes the board thicker.

Drill sizes can affect routing density, as you must go around each of the vias.

Mechanical stability of the board material is affected by placing the drilled holes too close to each other. This cuts through the reinforcement of the material.

Signal return efficiency is compromised by creating slots in the planes due to the density of the vias.

***Number of layers:** The total number of layers required for a given design depends on the complexity of the design.*

Let's redefine "complexity" to "density." The following will get you an estimate of the number of layers you'll need for the design:

Part placement density:

- Find the total area needed to place the components (CP).
- Use the "courtyard area" for each component, not the body size or footprint size.
- How much "useable" board area do you have on both surfaces of the board. (AB)
- Remove all mounting areas, keep-out areas, and unusable tab areas.
- Divide AB by CP. [AB/CP]

Routing density:

- How many total signal pins do you have to connect? (SP)
- How many power and ground pins do you have to connect? (PP)
- What size vias will you use for these? (V)
- What is the smallest trace needed to carry the currents in the circuit?

- Use the smallest trace width as a "grid" setting for trace and space. (G)
- Approximate space you'll need to route the board:

[(G)•(# SP)] + [(V)•(# PP)] = Approximate routing space needed (RS)

Number of layers needed for routing:

(RS) / (AB/2) = Approximate number of internal layers

Spacing between layers: *The space between layers can be either core or prepreg.*

No, the spacing between layers of copper will contain resin and reinforcement. These are determined by the layer stack requirements to attain the electrical specifications needed for the design. Either core or prepreg is used as needed.

By definition, core material usually has copper on both sides, and the resin is fully cured, often referred to as copper-clad laminate (CCL). Prepreg has no copper, and the resin is partially cured.

Stacked vias: *Avoid stacked vias if possible and choose staggered instead.*

Yes, this is true. Each time you add a stacked via to the center core of a board (1, 2, 3, or more), it is the equivalent of starting the fabrication process from the beginning. Resin slips a bit each time you heat and press the layers together. Alignment of the vias is very difficult to accomplish.

There are new processes that have been explored in 3D printing that will allow better alignment of these types of vias. There are very few companies right now who can do it and it's not cheap.

There are many more design rules than what has been covered here. They continue to expand to include newer "rules" for developing our PCB designs. What is today's bleeding-edge technology will become standard sometime in the not-too-distant future. Therefore, it is imperative that designers keep up with what's happening. **DESIGN007**

Cherie Litson, MIT CID/CID+, is the founder of Litson1 Consulting and an instructor at EPTAC and Everett Community College. She has more than 30 years of design experience and has been an instructor since 2003.

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AI-driven Inverse Stackup Optimization

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Artificial intelligence (AI) is transforming how we conceptualize and design everything from satellites to PCBs. Traditionally, stackup planning is a manual process that can be multifaceted and relies heavily on the designer's expertise. Despite having best practices and various field solvers to optimize parameters, stackup planning remains challenging for complex designs with advanced packaging, several layers, multiple power pours, and controlled impedance requirements.

This month, I explore inverse stackup optimization (ISOP), a machine learning-assisted framework that automates the stackup design process for advanced package design.

ISOP changes the game by using machine learning to efficiently search for the best stackup design parameters that meet target

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Figure 1: The goal-seeking algorithm solves the impedance for distinct technology rules within the same layer. (Source: iCD Stackup Planner)

specifications and optimize performance. The inverse PCB stackup optimization process searches for design parameters that meet the system specifications while optimizing a user-defined figure of merits (FoM). In physics, an inverse problem involves estimating the unknown parameters in reverse through measurements. Similarly, this optimization scheme searches for valid stackup design parameters by obtaining information about the target performance measurements. This optimization process is then accelerated by applying a machine language-based surrogate model.

Today, we essentially plan a stackup by examining the required target characteristic and differential impedance for each technology on each signal layer, then select the best fit from our dielectric materials library to meet our needs (Figure 1). The iCD Stackup Planner, for instance, has a goal-seeking algorithm built into the stackup list view that automatically fine-tunes the parameters.

Impedance goal-seeking algorithms help match trace width and clearance to achieve the desired characteristic or differential impedance. By entering the desired impedance value, multiple passes of the field solver automatically hone the variables to obtain the desired target impedance. This approach helps refine the parameters. However, while it essentially provides a close approximation, it does not determine the stackup structure or the dielectric material.

Alternatively, the inverse stackup optimization framework solves the PCB stackup optimization by incorporating a discrete domain hyper-parameter optimization (HPO), which searches for the best set of parameters in an optimization problem. HPO has been used to tune parameters in the design flow for very large-scale integration (VLSI) and field-programmable gate arrays (FPGA). It can also be used to optimize the hyper-parameters for individual stages, such as component placement and via spans. Besides parameter tuning, HPO also helps address the analog device sizing problem. The automated analog sizing methods work on the inverse design problem. Given target specifications, automatic analog sizing treats design parameters, such as transistor width, as hyper-parameters (configurable variables) and applies HPO to find the solution. HPO can be applied to automate the stackup design to adjust the

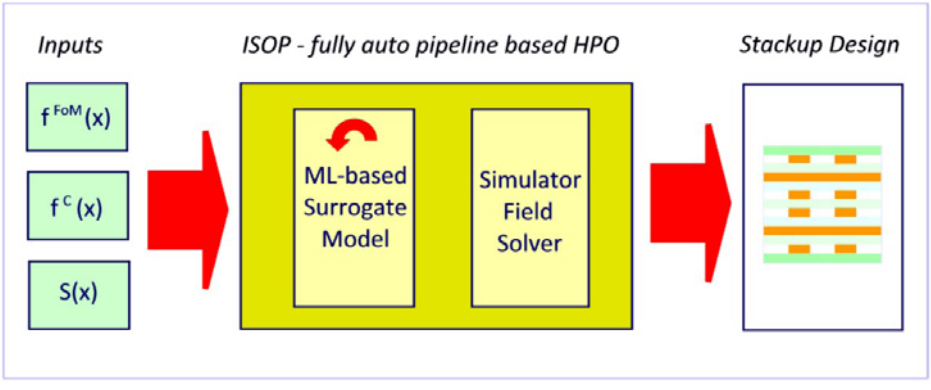


Figure 2: Overall process flow of ISOP framework.

trace width, clearance, and dielectric properties in inverse optimization.

The inverse stackup design optimization aims to find the optimal set of design parameters for each signal layer of a PCB stackup simultaneously. The final stackup design must meet performance specifications and optimize a specified performance FoM objective function. Both the constraints and FoM are from performance metrics and are non-trivial to evaluate. The traditional manual design flow relies on a designer's experience and a trial-and-error approach using multiple simulations. However, ISOP offers a more efficient and automated alternative. The ISOP framework solves the inverse PCB stackup optimization by incorporating a discrete domain HPO. Figure 2 shows an illustration of the overall process flow.

The HPO process begins with a user-defined function, a set of performance constraints, and parameter search spaces as inputs, then generates the stackup design parameters. It consists of two stages:

Early search exploration

Globally, sampling parameters in the first stage allow for the exploration of the search space. Instead of relying on time-consuming EM simulations, it uses performance metrics from a machine learning (ML) surrogate model (approximation model). This approach allows for more samples to be evaluated and a rapid reduction of the search space, albeit with some accuracy trade-offs. This method is akin to reducing the simulation time of a 2D BEM field solver by narrowing the solution space to expedite impedance calculations. A machine learning model termed the "learner" then identifies a limited set of candidates within the input design space whose predicted outputs closely align with desired outcomes.

Candidate roll-out

The second stage selects the final stackup design based on the initial results. The HPO then evaluates the designs with accurate EM simulations and selects the final solution based on the objective function. If specified by the user, ISOP can generate multiple design candidates ranked by FoM in the roll-out stage. A separate surrogate model, functioning as an "evaluator" assesses the reduced candidate space generated in the first stage. This evaluation process eliminates inaccurate and uncertain solutions guided by a user-defined coverage level.

The key innovation of this process lies in the successful integration of conformal inference (predictions), enabling seamless interactions between two machine-learning surrogates. One surrogate acts as a forward problem proxy, identifying promising solutions, while the other plays an advisory role, effectively eliminating inaccurate or uncertain outcomes.

The advantages of this framework over traditional single-stage inverse problems are twofold. First, it circumvents the need for intensive hyper-parameter optimization, as the evaluator model filters out undesired solutions in the second stage. Second, the framework exhibits remarkable applicability across a wide range of problems, owing to conformal inference's minimal distributional and model assumptions. By integrating conformal inference with any standard regression model, the framework readily provides prediction intervals, making it versatile and readily adaptable.

"The inverse stackup design optimization aims to find the optimal set of design parameters for each signal layer of a PCB stackup simultaneously."

Another promising research focus involves designing advanced protocols that enable more than two machine learning surrogates to

collaborate. This approach has the potential to eliminate even more undesired solutions from inverse problems. Evaluating the trade-offs between computational efficiency and accuracy improvements is essential in assessing the feasibility and effectiveness of such protocols.

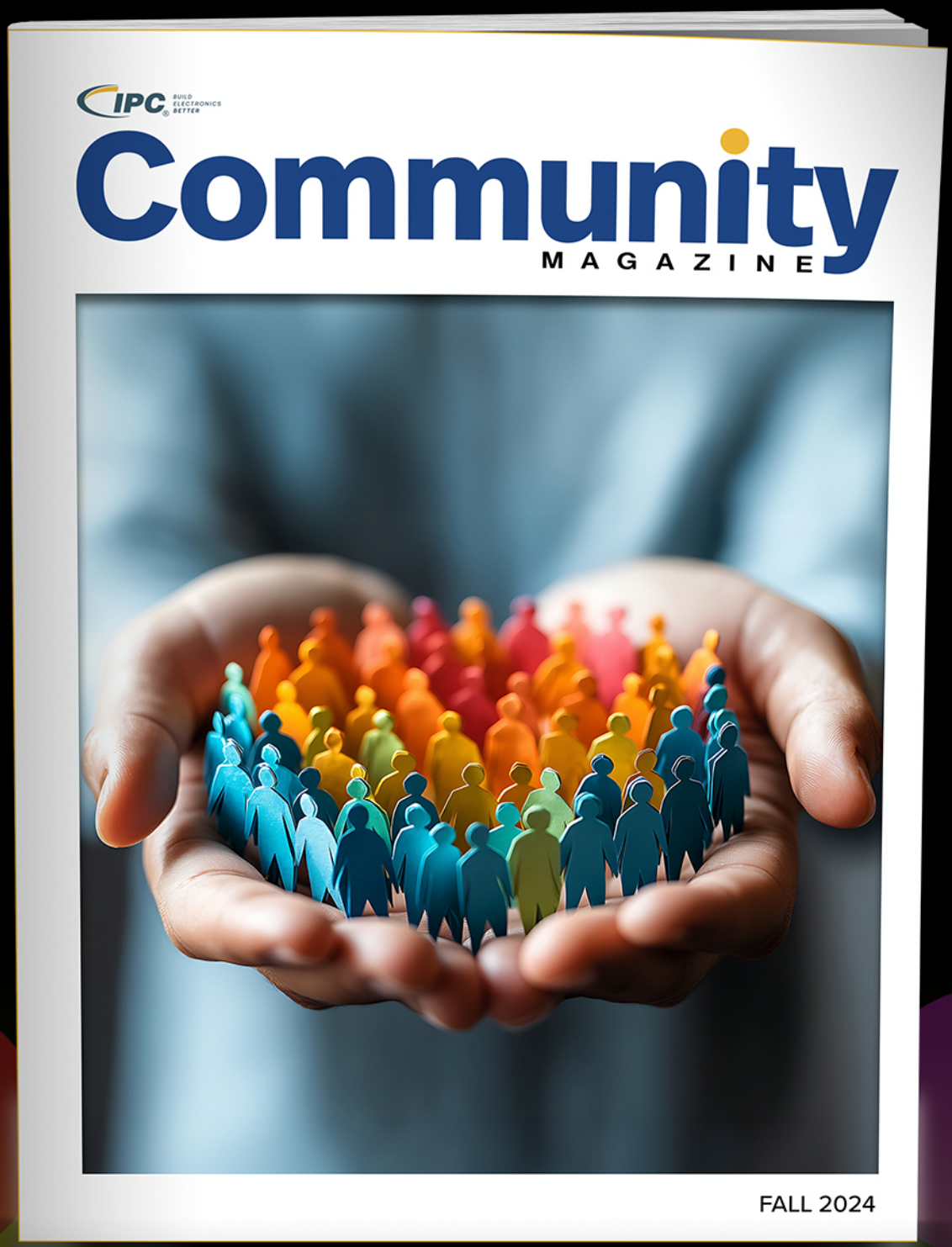
Key Points

- The inverse stackup optimization framework solves the PCB stackup optimization by incorporating a discrete domain hyperparameter optimization (HPO), which searches for the best set of parameters in an optimization problem.
- Besides parameter tuning, researchers also apply HPO to address the analog device sizing problem.
- HPO can be applied to automate the stackup design to adjust the trace width, clearance, and dielectric properties in inverse optimization.
- The first stage involves sampling parameters globally to explore the search space.
- A machine learning model termed the "learner" then identifies a limited set of candidates within the input design space whose predicted outputs closely align with desired outcomes.
- The second stage selects the final stackup design based on the initial results.
- A separate surrogate model, functioning as an "evaluator," assesses the reduced candidate space generated in the first stage.
- One surrogate acts as a forward problem proxy, identifying promising solutions, while the other plays an advisory role, effectively eliminating inaccurate or uncertain outcomes. **DESIGN007**

Resources

- "Beyond Design: Stackup Planning: Three Decades of Innovation," by Barry Olney
- "Machine Learning-Assisted Inverse Stack-Up Optimization for Advanced Package Design" by Chae Hyunsu, et al.
- "Two-Stage Surrogate Modeling for Data-Driven Design Optimization with Application to Composite Microstructure Generation" by Farhad Pourkamali-Anaraki, et al.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software, incorporating the iCD Stackup, PDN, and CPW Planner. You can download the software at www.icd.com.au. To read past columns, click here.



LOOK INSIDE

IPC BUILD ELECTRONICS BETTER

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IPC, FED Partner for New Design Conference in Vienna

Interview by Andy Shaughnessy

IPC and its German partner FED have teamed up to create a new PCB design conference in Vienna, Austria. The Pan-European Electronics Design Conference (PEDC) is scheduled for Jan. 29-30, 2025 at the NH Danube City hotel in Vienna.

IPC's Peter Tranitz, one of the show organizers, discussed how this new show came about, pointing out that, unlike many of the regional conferences in Europe, PEDC will host curated, peer-reviewed presentations, not promotional content or product pitches. Will PEDC become an annual event?

Andy Shaughnessy: Peter, tell us about the new design conference in Vienna, Austria.

Peter Tranitz: The idea for the Pan-European Electronics Design Conference came out of discussions that IPC and FED (Germany-based electronics design and manufacturing association) had with the PCB and EMS communities around our activities in Brussels. During those discussions, we learned that high-level scientific conferences are missing within the European landscape. In Europe, we have regional language conferences on electronic design organized by national associations. Often, little care is taken to avoid promotional and product pitches.

The PEDC is targeting the pan-European community for electronics design. We are transporting the model of the IPC APEX EXPO conference, which

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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(L-R) Christoph Bornhorn, FED executive director, Hans-Peter Tranitz, IPC, and Dieter Muller, chairman of the FED board.

excludes commercialism and ensures a high level of technical content for the presentations. Our technical program committee is targeting content with a high technical and scientific level. This pure, technically scientific approach is the differentiator from other events happening in Europe. We prefer presentations that haven't been published before, so that attendees see the content for the first time.

Are the presentations in English? What does the program consist of?

Yes, it's all English. We are open to engineers of all levels to academia and students, and we embrace diversity. We are seeking European participants as well as interested people from around the globe. Our Day 1 program consists of two keynotes. One is focused on electronic design and AI utilization, and the other keynote is around silicon-to-systems development. We have two panels: One tackles AI in electronics, and the other focuses on regulations and sustainability. These are big topics, especially in Europe.

On Day 2, we have two tracks with 12 presentations, each in parallel. One track focuses on silicon-to-systems and design techniques, and the other is around design for excellence, software, and tools. We've managed to engage professors from academia, top experts from research institutes, and companies that do a lot of research and development to help us set up a very attractive program. It is also worth mentioning that we have received far more presentation abstracts than we can cover at the conference.

We needed to make some tough decisions. With the good abstracts submitted that we could not cover at the Vienna conference, we tried to find other homes for them, such as IPC or FED conferences.

As a former conference chair, I know that having too many abstracts is a good problem to have. It sounds like you struck a chord with the industry.

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

Every day we get questions like those. And we love it. We have more than 600 PCB experts on 3 continents speaking 19 languages at your service. **Regardless where you are or whenever you have a question**, contact us!

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Yes, I think so. Registration is open. Anyone who intends to participate should register now because space is limited.

Tell us about the expo portion of the show.

We have about 20 tabletops available. As of late October, some of them had already been reserved, but we plan to sell those 20. Two sponsorship programs are available: one for the tabletop exhibits and one for additional sponsorships, as described on our website, pedc.eu.

I noticed a lot of AI content at the conference. Is that the theme for the show?

I would say that AI is the trend. The EDA industry is massively going in that direction. I think we'll have a broad look into different AI applications. From design software through manufacturing applications, AI is being used to improve results.

Do you see this show becoming an annual event?

Let's see how the first show goes. Of course, we would like to repeat this show.

There are certainly worse places to hold a conference than Vienna. It's a great location.

Vienna is a beautiful place. That's one reason why we have located the show there. Another reason is that it's located between Western Europe and Eastern Europe, and we want to grow as one Europe.

It sounds like there was a real need for this show. Good luck with the conference, Peter.

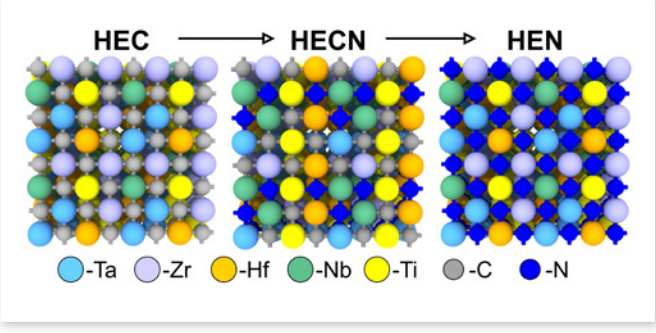
Thank you, Andy. **DESIGN007**

Register now for the Pan-European Electronics Design Conference, Jan. 29-30, 2025, in Vienna, Austria. For more information, click here.

New Research Used Plasma Dynamic Synthesis to Produce Carbide and Carbonitride

A group of researchers from Skoltech, Tomsk Polytechnic University, and other academic organizations in Russia and China used the method of plasma dynamic synthesis to obtain a high-entropy carbide in the form of nanopowders. The new technology provides a simple and universal way to produce high-entropy materials that are used in protective coatings, nuclear power, lithium-ion batteries, catalysts, and microelectronics. The results are published in the *Journal of Alloys and Compounds*.

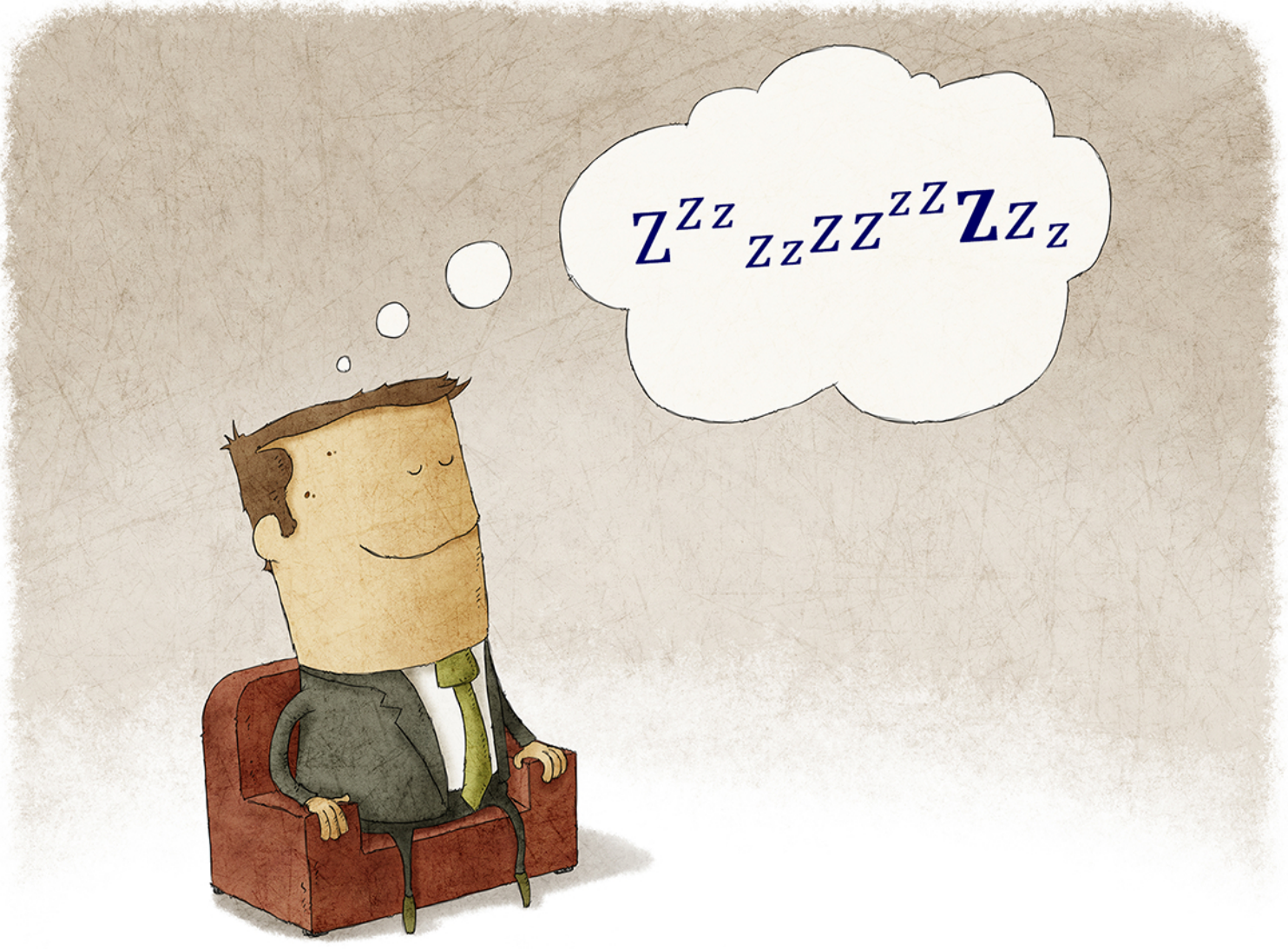
The composition of high-entropy compounds includes four or more different elements—in this case, metals and carbon. In the paper, scientists used a new technology and synthesized carbide from titanium, zirconium, niobium, hafnium, and tantalum (TiZrNbHfTaC5), as well as carbonitride from these components. The authors point out that the substance is one of the most suitable materials for manufacturing ultra-high-temperature ceramic elements due to its high mechanical properties and temperature stability. However, the synthesis of carbide is difficult: It requires careful preparation of the feedstock, and it is carried out at ultrahigh temperatures—about 2200-2300°C—for a long time.



"Multicomponent and high-entropy materials have been studied since recent times. We modeled various structures of carbonitrides with different concentrations of nitrogen and carbon and studied thermodynamic stability at different temperatures. We found out that a large amount of nitrogen can lead to strong mechanical stresses of the lattice, which will negatively affect the stability of the material," said the study supervisor, Professor Alexander Kvashnin from the Skoltech Energy Transition Center.

(Source: Skoltech)

We DREAM Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."
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Advanced Packaging Technologies: Look Before You Leap

Target Condition

Feature Column by Kelly Dack, CIT, CID+

Every so often, I'm disappointed by a high expectation that didn't work out. Some of these disappointments in the PCB design and manufacturing industry have been related to "new and advanced" PCB design products or services which proved to be impracticable for too many PCB designers (including me).

Often, my unmet expectations have involved automated or next-generation PCB layout software products that show well within the confines of a canned trade show presentation but fail miserably when applied in a real-life design. Over the years, I've been awed by "disruptive" technologies, products, or services only to realize I'd been reeled in by a slick, hyped-up sales and marketing presentation. I would find that the advanced technology was still in a development phase or so specialized that it was hardly executable within the scale of my workflow, and the sales team dropped me like a hot potato once they realized my production budget didn't exist above the stratosphere.

Understanding Marketing Hype

However, just because a technology is advanced doesn't mean it is right for your project. How many electronics engineers found this out after the 01005 chips came out? "Wow, smaller must be better," they said. Yet some eagerly placed them in strategic areas of their layouts only to find very few suppliers with assembly equipment capable of placing or inspecting them.

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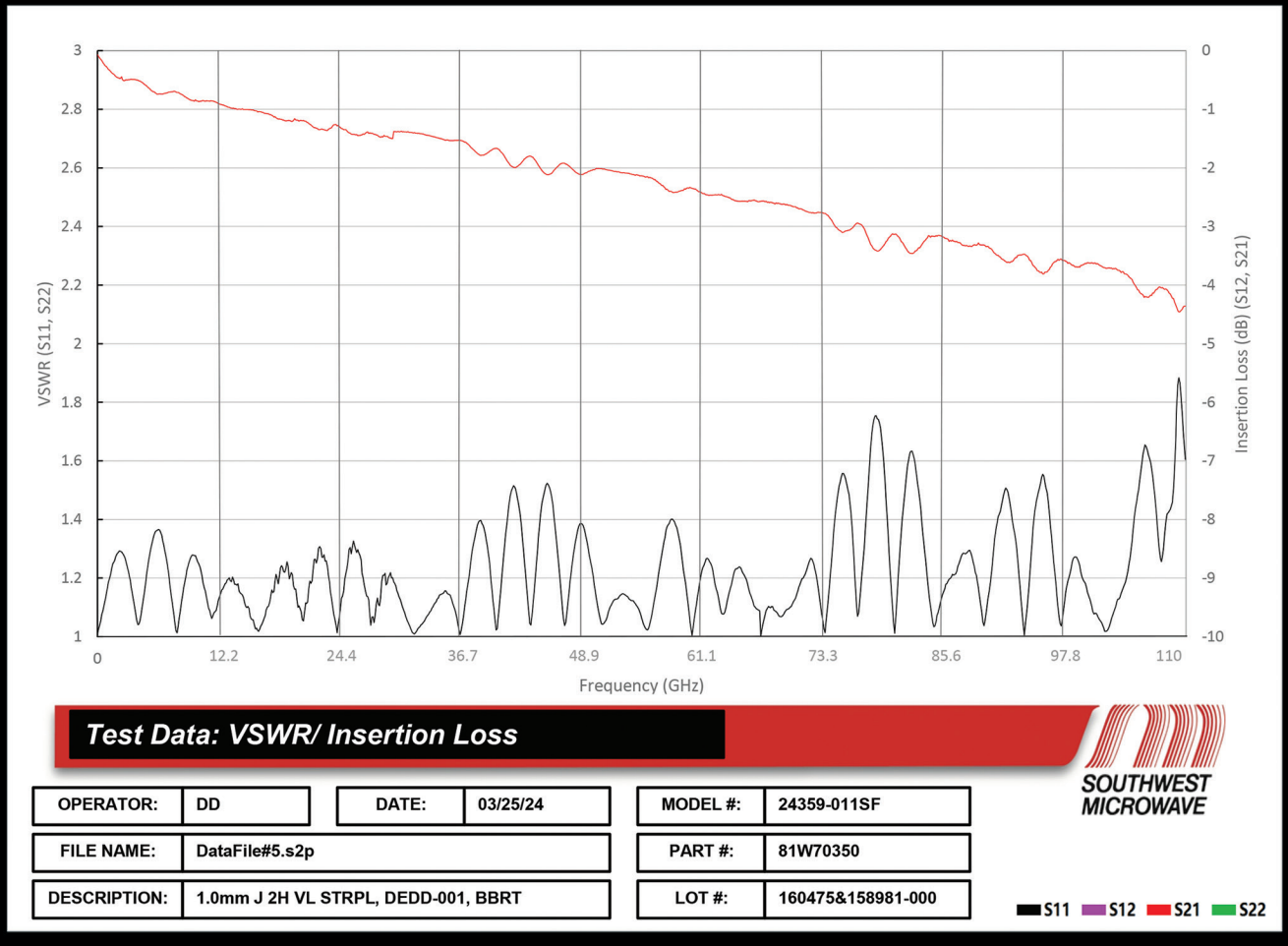

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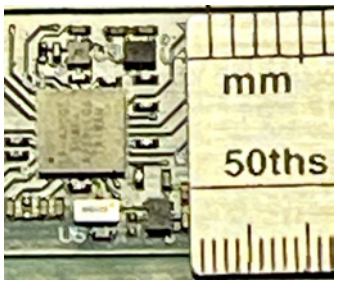


Advanced scale chips.

Even the "larger" 0201-sized chips are still considered advanced packaging by some EMS suppliers. They continue to cause headaches and lower profit margins due to processing issues relating to their scale.

On another front, how are those advanced, automated PCB DFM-checking tools working for us when we don't even know the capabilities of the suppliers who will build the boards? Why is it so easy for an experienced manufacturing engineer to catch glaring DFM issues on a design after the CAM data has been run through an automated audit? As an EMS stakeholder who liaises between PCB design and global manufacturing suppliers, I can tell you that there is still much room for improvement. Supplier requests for DFM changes for outside designs continue nonstop.

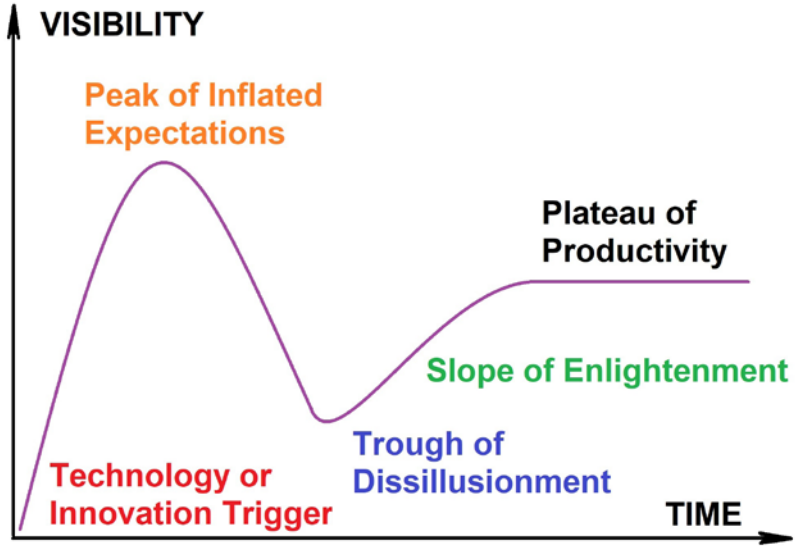
Regarding using AI to design and lay out a circuit board, it's not that it can't happen. But I've learned that I need to be in touch with the context of feasibility when considering the implementation of something so advanced. Before redirecting any of my time or resources away from a workflow paradigm for which the wheels are already well-greased, I must be certain of the advantages. In sales and marketing, adding "advanced" to your products or capabilities can get them more attention. Potential customers will presume they must be "better" while still offering availability and manufacturability, though maybe with a higher price tag.

As cliché as it sounds, "cutting edge" has traditionally indicated a condition better than advanced; the product or service slices through all the peripheral BS. It implies direct contact and exposure to a problem at hand so a definitive solution can be implemented. As most of us know, when the marketing hype reaches "bleeding edge" status, there is at least an admission from the technology marketers that the product or service may hurt until fully implemented.

Deep-pocketed visionaries who can afford to bleed for a while get in early on, but this class of advancement can be risky. There is no guarantee that competitors won't have caught up, even after the initial wounds heal and the process smooths out.

Understanding the Technology Development Hype Phases

If you are an informed, DFM-savvy PCB designer or engineer considering advanced technology, you must understand what happens throughout the development phases of a product or service. The Gartner hype cycle1 depicts the five phases of maturity for emerging technologies. Gartner Inc. actively tracks technologies to examine and report on their advancements using graphic milestones. This chart concept is an effective tool for the PCB design and manufacturing industries to evaluate which phase of an advanced technology makes the most sense to dive in.



Simplified Gartner hype cycle chart.

Integrated Tools to Process PCB Designs into Physical PCBs

Visualize

Use manufacturing data to generate a 3D facsimile of the finished product.

Verify

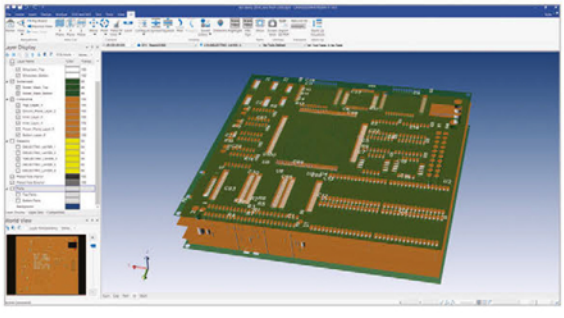
Ensure that manufacturing data is accurate for PCB construciton.

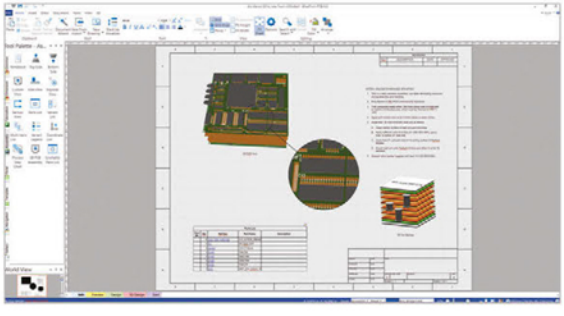
Panelize

Minimize costs in both PCB fabrication and assembly through maxiumum panel usage.

Document

Quickly and easily specify the PCBs form, fit and function.





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The Gartner Hype Cycle: Breaking Down the Phases

Let's examine the chart and see if we can relate to some of the common ups and downs many engineering groups experience when developing their own advanced solutions or trying to implement others from outside.

1. Innovation (Technology) Trigger

"A potential technology breakthrough kicks things off. Early proof-of-concept stories and media interest trigger significant publicity. Often no usable products exist and commercial viability is unproven."[1]

This initial phase could come about as a noble challenge, like the day that JFK announced America would land a man on the moon. Innovation can be triggered by a change in technology, like a new chipset, or more capability packed into a less expensive part. Sometimes, a project launches to solve an immediate need during a world crisis, like when the Open Source Ventilator project was formed to quickly address the need for ventilators during the pandemic.[2]

Building a team to respond to an innovation trigger and then engage in a full-blown project is not for the faint of heart. At this stage, information and decision-making move fast. The concept involves unknown risks and no guarantee of success or reward.

2. Peak of Inflated Expectations

"Early publicity produces a number of success stories—often accompanied by scores of failures. Some companies take action; most do not."[1]

Once news breaks of a new advanced product or service, a sales and marketing team will most certainly become involved. Often before the idea is developed and proven, publicity has been generated and investors are being solicited. This is the high point in a project in which hyped expectations have not been vetted against solid application, and a PCB designer obtains that new limited capability demo software to try out. It's also when product or service development begins shaking hands with real users.

3. Trough of Disillusionment

"Interest wanes as experiments and implementations fail to deliver. Producers of the technology shake out or fail. Investment continues only if the surviving providers improve their products to the satisfaction of early adopters."[1]

Both innovators and customers find themselves crashing and burning into the trough of disillusionment from time to time. At the bottom of the trough there is a bright adage attributed to author John C. Maxwell: "Fail early, fail often, but always fail forward." This quote appears to have been adopted by some Silicon Valley startups, morphing into the more familiar "fail fast, fail often" meme most PCB industry development folks are familiar with. Continuing from here will require more investment and more time. Will it be worth it?

4. Slope of Enlightenment

"More instances of the technology's benefits start to crystallize and become more widely understood. Second- and third-generation products appear from technology providers. More enterprises fund pilots; conservative companies remain cautious."[1]

If it is determined that the rewards can still exceed the risks, much can be gained from leveraging experience and feedback data collected from all the failures experienced during previous phases. Think of how many rockets exploded or crashed before SpaceX was successful in landing a reusable booster stage. New technology and ideas—successes and failures—make valuable reference points to gauge applicability over time. It may be during this advanced phase of a product or service timeline that an engineer with only a substratosphere limited budget begins adopting a technology, as it appears to be the best place to jump in before the competition does.

5. Plateau of Productivity

"Mainstream adoption starts to take off. Criteria for assessing provider viability are more clearly defined. The technology's broad mar-

ket applicability and relevance are clearly paying off. If the technology has more than a niche market, then it will continue to grow."[1]

We are all familiar with and use products and services that have long resided on the plateau of productivity. They have been there so long that we no longer refer to them as advanced—though once they were. We take for granted the ease at which we can order or design around this basic, proven technology.

For instance, glass-epoxy materials have been around for more than a half-century. It is still the go-to laminate for more than 80% of the PCB designs in the world. Will it ever be widely displaced? Perhaps, but only after new materials or processing makes its way through the slope of enlightenment phase and levels out on the plateau of productivity. There are many on the way, and many with a long way to go.

Beyond the Fifth Phase

Obsolescence is not a phase that is made clear in the Gartner hype cycle chart for an obvious reason. There is not much to hype about a product so old it's being discontinued or replaced by new technology.

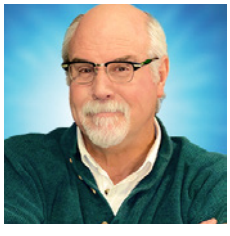
Since I started doing PCB design layout in the 1980s, many advanced technologies have long since slid off the plateau of productivity and are mulching in a landfill somewhere. Some of our old designs are even preserved and featured in PCB design history museums every so often.

We must always be on the watch for better solutions for the products we design. We must balance all the forces of reason in selecting technology in order to design for excellence.

If you are an informed, DFM-savvy PCB designer or engineer thinking about implementing some advanced technology, consider that our industry "right-sizes" headcount, machinery, production volumes, and even software capability all the time. Rather than quickly reaching for that sparkling, glittery piece of advanced technology to incorporate into your design, it makes sense to consider a "right-tech" approach to product design. **DESIGN007**

References

1. Gartner hype cycle, Wikipedia.com.
2. Engineering Together to Save Lives—The Open Source Ventilator Project, Altium, youtube.com.



Kelly Dack, CIT, CID+, provides DFX-centered PCB design and manufacturing liaison expertise for a dynamic EMS provider in the Pacific Northwest while also serving as an IPC design certification instructor (CID) for EPTAC.

To read past columns, click here.

MilAero007 Highlights

U.S. Navy, Lockheed Martin Skunk Works Demonstrate First Live Control of an Uncrewed Air Vehicle by UMCS and MDCX ▶

Powered by the Skunk Works® MDCX™ autonomy platform, the UMCS controlled a GA MQ-20 Avenger uncrewed air system (UAS) as it completed a live fly mission. This demonstration is a pathfinder that helps to advance the complex technology necessary to enable crewed and uncrewed teaming as envisioned for programs such as CCA and others.

Lockheed Martin and Anduril to Successfully Detect and Track Drone Threats in Middle East ▶

Lockheed Martin has successfully integrated the Q-53 multi-mission radar (MMR) with Anduril's Lattice Command and Control (C2) environment during the U.S. Central Command Desert Guardian exercise held at Fort Drum earlier this month.

Teledyne FLIR Defense Wins $91 Million Contract from U.S. Army for Black Hornet 4 Nano-Drones ▶

Teledyne FLIR has received $25 million in initial orders that will cover delivery of the first tranche of Black Hornet 4 drones, as well as controllers, spare parts, and training.

Attention Students: NASA Launches Power Systems Student Essay Contest ▶

NASA's fourth annual Power to Explore Student Challenge kicked off on Nov. 7, 2024. The science, engineering, technology, and mathematics (STEM) writing challenge invites kindergarten through 12th-grade students in the United States to write an essay about a new nuclear-powered mission to any moon in the solar system they choose. Submissions are due Jan. 31, 2025.

Sikorsky, Rain Successfully Demonstrate Autonomous Flight ▶

Sikorsky, a Lockheed Martin company and Rain, a leader in autonomous aerial wildfire containment technology, successfully demonstrated how an autonomous Black Hawk® helicopter can be commanded to take off, identify the location and size of a small fire, and then accurately drop water to suppress the flames.

An Update on USPAE's Strategic Initiatives ▶

James Will, executive director of the U.S. Partnership for Assured Electronics (USPAE), provides this update on the group's strategic initiatives. The organization, which is affiliated with IPC, recently transitioned to being a 501(c)(3). It is navigating through a dynamic landscape, working to enhance our microelectronics manufacturing capabilities including PCBs, and adapt to emerging technology trends and market challenges.

DARPA Taps RTX to Strengthen Cyber Resiliency ▶

RTX's BBN Technologies was awarded a contract to support DARPA's Compartmentalization and Privilege Management, or CPM, program. The CPM program aims to enhance cyber resilience by automatically subdividing software systems into smaller, secure compartments, preventing initial breaches from escalating into successful cyberattacks while maintaining system efficiency.

DESIGN TIPS #124:

ETCH COMPENSATION

What is minimum space and trace? The answer depends on the starting copper weight.

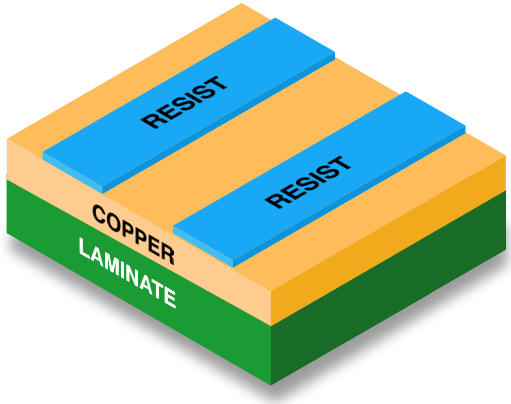
This is because we must do an etch comp on the traces in CAM to compensate for known etch loss. The space between traces after compensation will play a role in whether a board can be manufactured.

The lower the spacing width, the higher the cost. Designers don't always account for the proper starting copper weight after edge compensation.

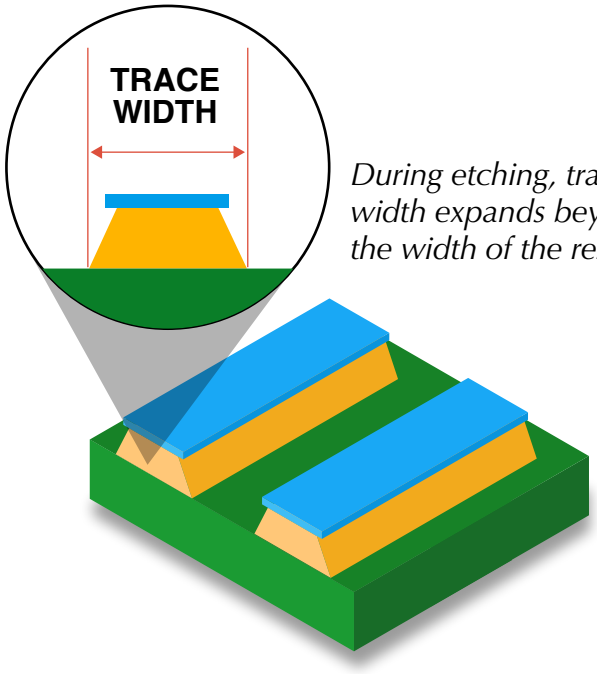
Design tips:

- For accurate starting copper weight, **add a half mil (.0005″) to all copper features**.
- **Start with 3/8 or 1/4 oz. foil**, reducing etch comp and less likely to cause a spacing issue.
- **Boards that call for full body electrolytic gold are not comped** to avoid gold slivers occurring during the etching process.

Before etching



After etching



During etching, trace width expands beyond the width of the resist.

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Impact of Advanced Semiconductor Packaging on PCB Stackup

Designers Notebook

Feature Column by Vern Solberg

To accommodate new generations of high I/O semiconductor packaging, printed circuit board fabrication technology has had to undergo significant changes in both the process methods and the criteria for base material selection and construction sequence (stackup). Many of the new high-function multi-core semiconductor package families require more terminals than their predecessors, requiring a significantly narrower terminal pitch. Interconnecting these very fine-pitch, high I/O semiconductors to the PCB is made possible by an intermediate element referred to as an interposer. The interposer enables the interconnect of the semiconductor package with an ultra-high-density socket (Figure 1), for example, that is configured to interface with a conventional FR-4 laminate-based, multiple layer printed circuit board.

When defining the complexity level for the circuit board, the designer will first establish a criterion for fabricating the circuit board. This will include the board outline and thickness limitation. In regard to controlling the specified circuit board thickness limit, a clear objective must be established to identify the number of circuit layers that are to be dedicated to signal routing and the number of layers reserved for power and ground distribution. Estimating the required number of signal layers will be determined by the component density and interconnect complexity. The number of power and ground layers will be determined by the number of ground terminals on the components and any requirements for multiple operating voltages.

Before beginning the circuit board design process, experienced professionals advise the designer to perform an interconnect capacity analysis. This analysis is based on the board's usable area and terminal number for all components defined in the parts list, but it excludes the circuit conductors. To determine the basic component area, the designer must first gather mechanical outline specifications and electrical data for all active and passive component parts.

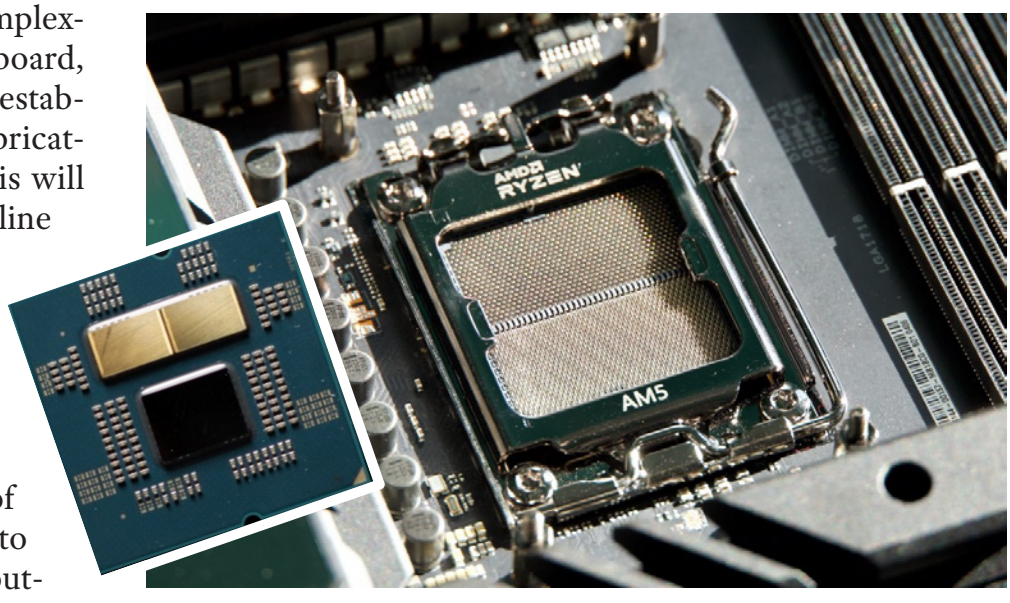

Figure 1: AMD's universal 1,718 I/O land grid array socket developed for the Ryzen 7000 series of high-function multicore CPU products.

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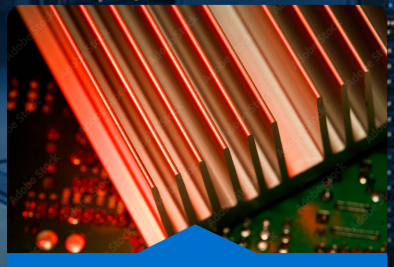

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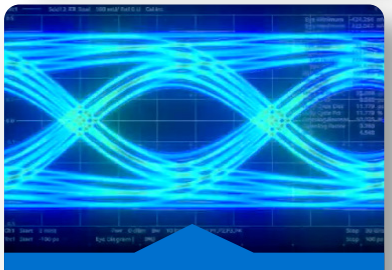

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From this data, the designer can assign the associated land pattern geometries and pad stack from the pre-established CAD library. To calculate the basic area required for component placement and conductor layers needed for circuit interconnect, designers must contemplate the land pattern features for mounting the components, define "keep out zones," establish clearances reserved for assembly process evaluation, and, when necessary, post assembly rework and repair. The final analysis will provide the designer with an estimated maximum surface area needed to complete all circuit interconnects.

Establishing Circuit Routing Criteria

Although printed circuit board fabrication process capabilities have continued to expand on a global scale, fabrication process capability from one supplier to another, however, is not likely to be equal. This is because of the continuous advancement in related chemistries, processing systems, materials, and overall process control evolution. Ensuring the success of the end-product's functionality requires an understanding of the designated fabricator's primary capability attributes and how design complexity will affect the printed circuit board's producibility and cost.

Following component placement, the CAD system's auto-router will assist the designer in determining the expected interconnect completion rate. The auto-router function can also be used to aid the designer in identifying circuit routing bottlenecks or other critical interconnect issues not identified during the initial component placement process. If the interconnect result is less than 85%, then it is a likely indication that the designer will need to make some adjustments to component placement. In regard to auto-routing for frequency management applications, CAD routing tools are very good, but conductor routing on circuit boards requiring controlled impedance or selective conductor shielding will likely require a degree of interactive manipulation by the design engineer.

When component density and interconnect complexity exceed the area defined by the PCB outline, a higher level of fabrication technology will be justified, requiring additional circuit layers and/or increased conductor intercon-

Table 1: Inner layer circuit routing from an independent industry capability survey

Copper Foil Thickness	Standard	Min. Lines & Spaces	Emerging
0.24 oz. 8.5 µm	.002"/.002" 5.0 µm/5.0 µm	.002"/.002" 5.0 µm/5.0 µm	<.002"/.002" <5.0 µm/5.0 µm
0.37 oz. 13 µm	.003"/.003" 7.5 µm/7.55 µm	.025"/.003" 6.5 µm/7.5 µm	<.0025"/.002" 6.5 µm/5.0 µm
0.50 oz. 17 µm	.004"/.004" 10.0 µm/10.0 µm	.003"/.003" 7.5 µm/7.5 µm	<.003"/.003" 7.5 µm/7.5 µm
1.0 oz. 34 µm	.005"/.005" 13.0 µm/13.0 µm	004"/.004" 10.0 µm/10.0 µm	. 0035"/.004" 7.5 µm/10.0 µm
2.0 oz. 68 µm	.008"/.008" 20.0 µm/20.0 µm	.006"/.008" 15.0 µm/20.0 µm	.006"/.006" 15.0 µm/15.0 µm
3.0 oz. 102 µm	.010"/.010" 25.5 µm/25.5 µm	.008"/.010" 20.0 µm/25.5 µm	.008"/.008" 20.0 µm/20.0 µm

nect density. Electrical interconnect on internal layers for the board enables significantly greater circuit routing density. The circuit path between key components can be more direct as well, providing greater circuit speed and lower resistance. To ensure the greatest interconnect efficiency, the designer should alternate the overall direction of the circuit path from one layer to another, using plated via-holes to accommodate direction change as needed. With the circuit width and space requirement already established in the CAD system, the auto-router function can quickly complete the initial interconnect process.

Three technical levels of capabilities for circuit conductor routing on the inner layers of the circuit board are presented in Table 1: standard, advanced, and capability classified as emerging technology.

The capability shown in the emerging technology column may be a standard capability for some fabricators but, for others, the process will require improvement in process control and chemistry refinement. The individual circuit board supplier's standard level of complexity will generally represent what is recommended to achieve their highest yield and most favorable unit quality. The circuit routing complexity and copper foil thicknesses on the external surfaces of the multilayer printed circuit board fabrication may differ from those routed on the inner layers of the stackup.

The final process stage for the multiple layer circuit board is lamination of all the circuit layers, including the two external layers. Following lamination, via holes will be drilled or formed, followed by a number of plating steps to fill holes, and in some cases, build up the conductor pattern thickness. A series of imaging, plating, and chemical etching processes takes place for the two external layers. Depending on the board fabricator's capability, conductor routing on the external surfaces of the circuit board may require a slightly different requirement for conductor routing. The data furnished in Table 2 may be required by the supplier, and although it will have an impact on circuit routing density, fabrication yield may be a factor.

Stackup Planning for High Density Multilayer Circuit Boards

A PCB stackup plan must be developed to define the order, thickness, and materials used for each layer of the circuit board. The circuit layers are either dedicated to routing signal

Table 2: External layer circuit routing from an independent industry capability survey

Copper Foil Thickness	Standard	Min. Lines & Spaces	Emerging
0.24 oz. 8.5 µm	.003"/.003" 7.5 µm/7.5 µm	.0025"/.0025" 6.5 µm/6.5 µm	.002"/.002" 5.0 µm/5.0 µm
0.37 oz. 13 µm	.004"/.004" 10.0 µm/10.0 µm	.003"/.003" 7.5 µm/7.5 µm	.0025"/.003" 6.5 µm/5.0 µm
0.50 oz. 17 µm	.005"/.005" 13.0 µm/13.0 µm	.004"/.004" 10.0 µm/10.0 µm	.0035"/.004" 7.5 µm/10.0 µm
1.0 oz. 34 µm	.006"/.006" 15.0 µm/15.0 µm	.005"/.005" 13.0 µm/13.0 µm	.004"/.005" 10.0 µm/13.0 µm
2.0 oz. 68 µm	.012"/.012" 30.5 µm/30.5 µm	.010"/.010" 25.5 µm/25.5 µm	.008"/.008" 20.0 µm/10.0 µm

traces or to provide for power and ground distribution. The fabricators emphasize the importance of the layer stackup order and how it affects both end-product performance and functionality. Key concerns include maximizing signal integrity, impedance control, power and ground distribution, and avoiding excessive thermal concentration (hot spots).

The primary materials used for the multiple layer circuit board are the copper foil to form the interconnect, the glass-reinforced epoxy-based laminate material for the core structure, and prepreg material for bonding the layers together.

- There is a wide range of copper foil thicknesses available, but the most common PCB copper specified for multilayer PCB applications is 17.5-micron. However, when very higher circuit density is warranted, the circuit board fabricator may implement a semi-additive copper forming process that uses a much thinner (5-miron, 9-micron, or 12-micron) copper foil.
- A glass-reinforced epoxy material developed expressly for printed circuit core has been (and will continue to be) the workhorse of interconnection technology. The materials are widely available, very versatile, and can be tailored to accommodate different product functions or applications. Although all epoxy/glass laminates have similar physical attributes, the products that adapt these materials often have very different manufacturing focus and performance requirements.
- The prepreg materials are a dielectric engineered to bond the copper foils to each other and to the copper-clad core structure of the multilayer circuit board. The thickness of the prepreg material selected for the multilayer board will vary, depending on the number of circuit layers and the maximum finished board thickness specified.

In the past, the circuit board designer did not get an opportunity to be involved with the planning of the layer stackup sequence strategy used to build the circuit board. The design tools simply didn't have the sophistication for board layer stackup and configuration capabilities that they do today. That responsibility for stackup planning was transferred to the experts, the actual fabricator of the circuit board. Once established, the designer would then document the circuit board's formation with the specific material set and construction.

The fabrication process for the multiple core stack examples illustrated in Figure 2a begins with hole forming and plating, imaging, and chemically etching the circuit pattern on both sides of each core section with the exception of the two outer layers of the stack. Although the holes will be formed and plated, only the inside-facing circuit pattern will be processed. Next, the core layers are assembled using the prepreg material between the opposing copper surfaces for lamination. Holes that are furnished to inter-

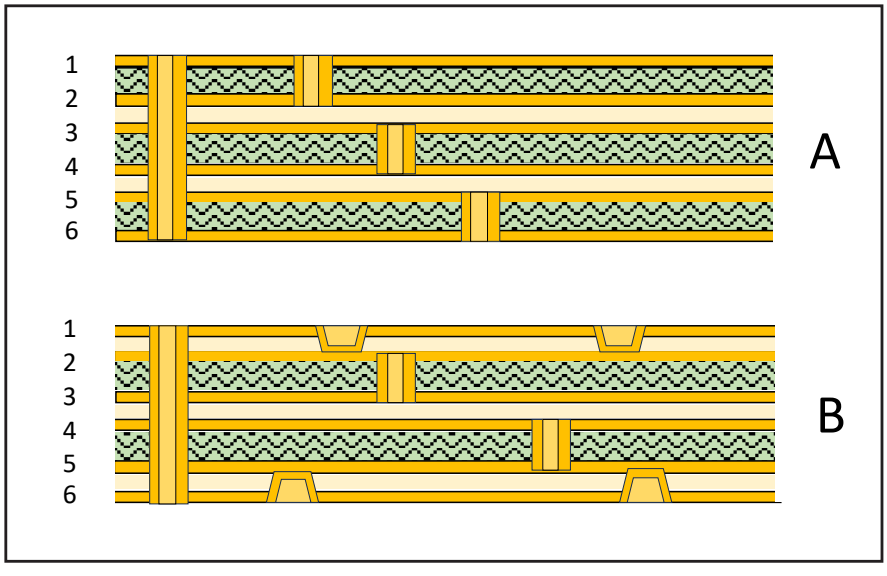

Figure 2: Comparing two 6-Cu layer circuit board stackup construction variations, one having three cores to one with cap layers requiring only two cores.


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face with the conductor pattern within the now laminated structure are formed, the circuit pattern imaged, followed by copper plating to build up the surface of the conductor pattern and plate the holes. After chemical etching to define the circuit pattern on the two outer layers, the boards are made ready for solder mask application and final electrical test. The process sequence for Figure 2b will be the same for the two inner core sections, but the outer circuit pattern is referred to as a cap layer that will interface with the conductor patterns on the core sections with laser-ablated and copper-plated microvias.

Today, the printed circuit board layout process is very different, as most major CAD software developers are furnishing design tools equipped with advanced PCB layer configuration features. Although these tools establish the general order of the conductive layers, the actual construction can have significant variations. The 12-layer stackup shown in Figure 3 incorporates all of the process steps noted above but it includes a center-located core section that is referred to as a floating core.

Assembly sequence:

1. The two double core sections (circuit layers 2, 3, 4, and 5 and circuit layers 8, 9, 10, and 11) are first assembled and processed separately, typical of the example shown in Figure 2b, but without the copper foil cap layers 1 and 12 on both.
2. The two multi-core sections are then assembled with the addition of single copper-clad (floating) core for layers 6 and 7 (reserved for power and ground distribution) between the two multiple layer sections.
3. The two sections and floating core are then topped off with the two copper foil cap layers (1 and 12) and made ready for lamination.
4. Following lamination, through-holes for inner layer interconnect are drilled and cap layer microvia holes for joining layers 1 and 2 and layers 11 and 12 are formed.
5. The final stages provide copper hole plating operation, final imaging on both outer surfaces, chemical etching, and solder mask application previously described.

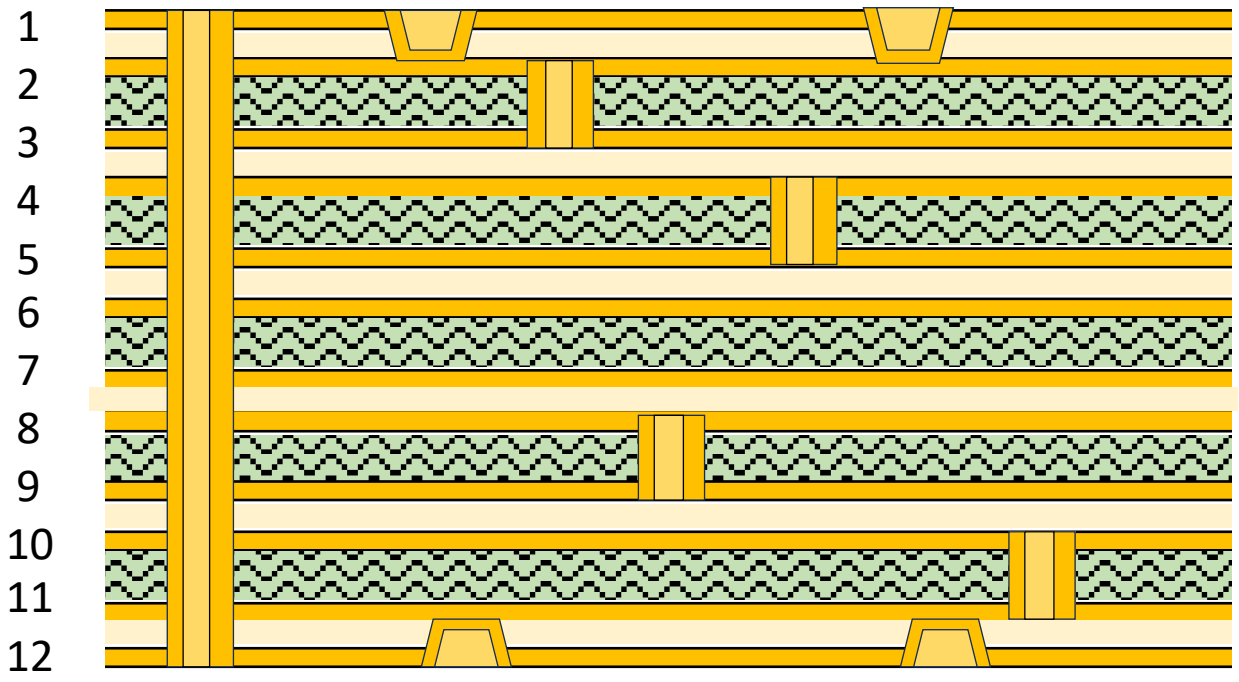


Figure 3: Twelve-Cu layer circuit board includes four core layers plus one floating core and two cap layers.

When designing a PCB stackup, several important considerations must be made to ensure proper functionality, signal integrity, and manufacturability[1].

1. Consider factors such as signal density, power distribution, and noise isolation.
2. Allocate power and ground planes to provide a stable, low-impedance power distribution network.
3. Maximize ground plane size to reduce noise, improve signal quality, and facilitate thermal dissipation.
4. Place decoupling capacitors near power and ground plane pairs to suppress high-frequency noise and provide clean power to components.
5. Plan the arrangement of signal layers to minimize signal degradation and maintain good signal integrity.
6. Proper layer ordering, impedance control, and controlled dielectric constants are crucial for managing signal integrity issues such as crosstalk, signal reflections, and impedance mismatches.
7. Minimize EMI through careful placement of signal and power planes, using shielding layers if necessary, and use proper grounding techniques.
8. Determine the order of signal layers to minimize crosstalk and ensure efficient routing.
9. Grouping high-speed signal layers and separating them from low-speed layers can help manage signal integrity.
10. Design the stackup with controlled impedance for critical high-speed signals.
11. This involves calculating and controlling the trace widths, dielectric thickness, and layer separation to achieve the desired impedance values.
12. Use thermal vias and distribute thermal planes to manage heat dissipation.
13. Place components with high heat production away from more sensitive components.
14. Note the capabilities and limitations of your PCB manufacturer (minimum track width and spacing, minimum drill size, and material availability).
15. Select laminate materials based on electrical performance, thermal properties, and cost.

Different materials have different dielectric constants, loss tangent values, and thermal conductivities that can affect the overall performance of the PCB.

Note: PCB stackup methods and design guidelines will vary somewhat from one supplier to another, depending on the project's specific requirements, such as the frequency of operation. The board fabricator selected or qualified by your company may recommend a stackup sequence different from those shown here, one that the matches their unique process procedures, environmental conditions, and industry standards.

Before investing a lot of time in the design phase of the product, make an effort to consult with the potential circuit board fabricator to review the construction options most suitable for the application. For example, when the external surfaces of the board require a greater level of conductor routing density for the high I/O very fine-pitch semiconductor interconnect, the supplier may recommend implementing the sequential build-up (SBU) process. This process enables up to three additional conductor layers to be incorporated on the external surfaces of the board but the sequential build-up process will have its own unique set of design rules. **DESIGN007**

References

1. PCB Stackup Design Guidelines,
2. Cadence Design Systems.

Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns, click here.

Designing for Reality: Solder Mask and Legend

Connect the Dots

by Matt Stevenson, ASC SUNSTONE CIRCUITS

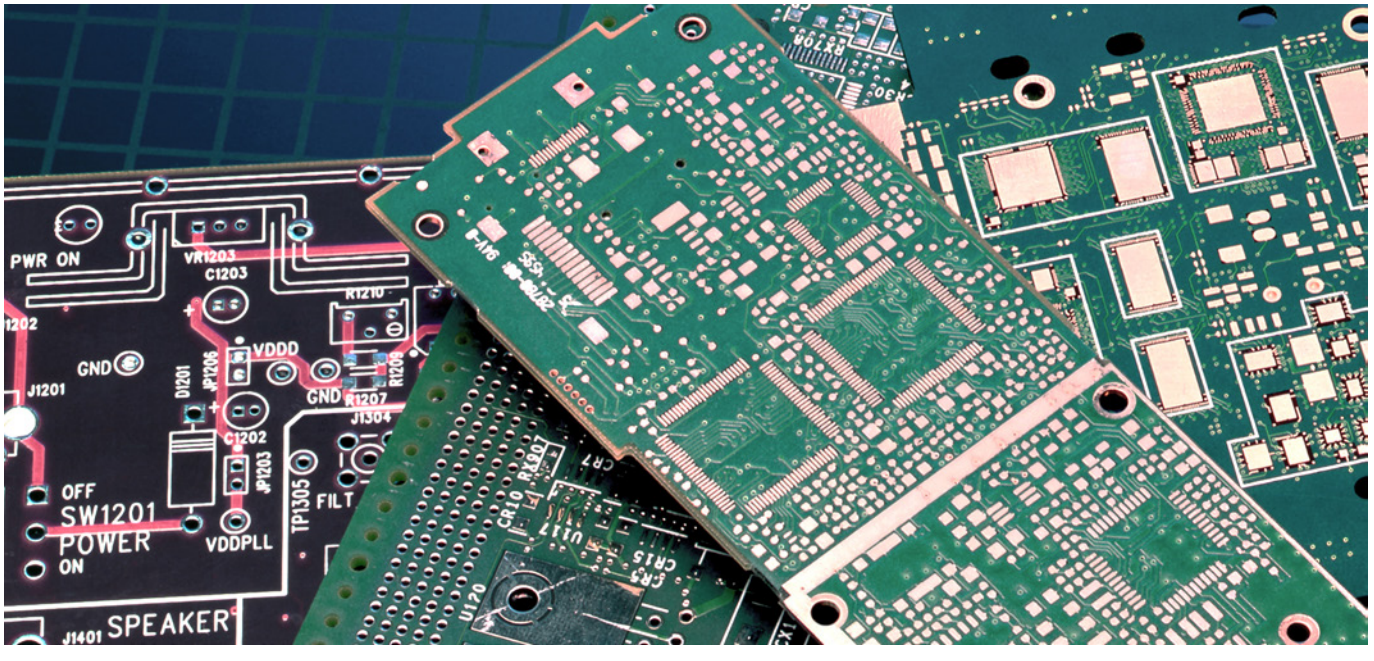
In the previous episode of I-Connect007's *On the Line with...* podcast, we discussed the strip, etch, and strip process. At this point, we have a functioning board, but we still need to protect the PCB from environmental effects and document the circuit components. This brings us to the solder mask and legend phase of production.

Before the process begins, we must inspect the boards to ensure that the plating and etching process is effective and the PCB meets customer functionality requirements. We have two inspection methods: visual and automated optical inspection (AOI).

A visual inspection under magnification by an inspector is adequate for simpler designs. Inspectors examine the board components for various issues, such as ragged traces or copper where it does not belong, and reject those that do not pass the test. For more complex boards or where a customer requests higher than Class 2 IPC-A-600 inspection, we use an AOI process that performs a near pixel-to-pixel comparison between the physical board and the original design data.

Pro Tips for a More Effective Board Inspection

Designers can help the inspection process run more smoothly and effectively by providing their manufacturers with clean data files. The size of the files and the memory required can affect the speed and accuracy of the AOI process, so it is important not to overload the design file with unnecessary data.



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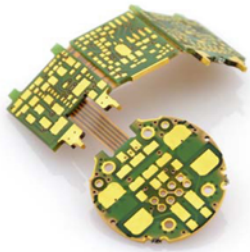

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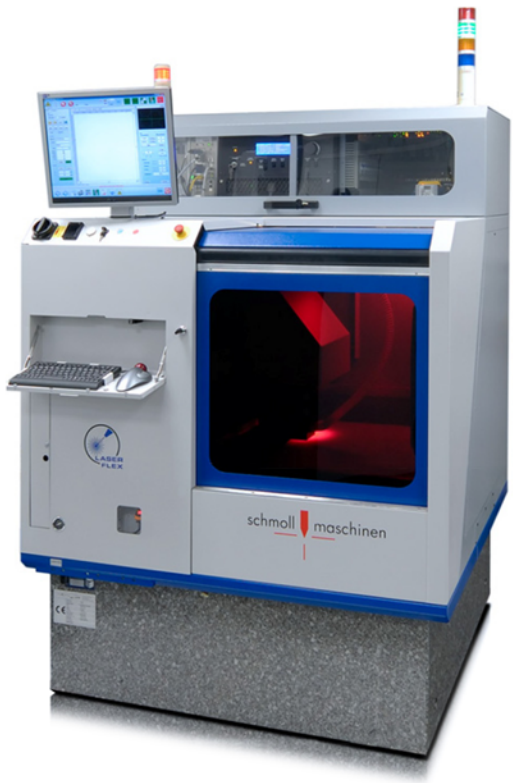

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Roughening the Copper Once the board has passed inspection, we begin the solder mask process by slightly roughing up the board's copper. This is to promote adhesion and create a good bond between the copper on the surface and the solder mask.

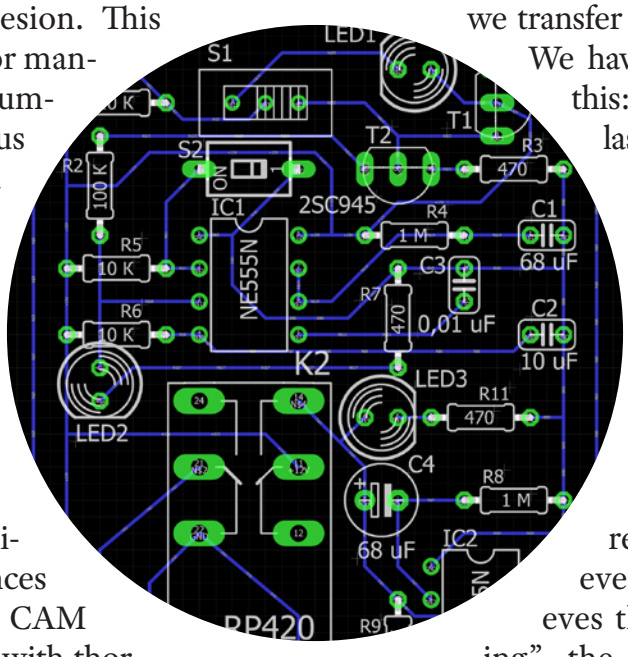
We use three different methods to rough up the copper, each with distinct advantages and disadvantages. Designers should consider which is best for their designs.

A mechanical scrub, depending on how aggressively it is performed, can create gouges, troughs, and rivers that impact performance for boards requiring high-speed signals. For most boards, a mechanical scrub will not create issues and is a common, cost-effective method for roughening copper.

The second method involves running the panels through a slurry of a soft pumice material that can also create pits and gouges. This process does not have as much impact on the trace performance as a mechanical scrub, and it creates great adhesion. This method has a downside for manufacturers because the pumice becomes a hazardous waste that requires extra care upon disposal.

The last method is an adhesion promoter that chemically roughens the surface. This is the least likely to create performance-impacting abnormalities on the PCBs.

Designers can communicate their method preferences by consulting with their CAM engineer and calling it out with thorough design notes in the design specifications.



Solder Mask Application

There are two common methods for applying solder mask. Most of us think of the classic flood-coating the board with liquid solder mask and removing it in the areas we want to remain solderable. However, additive printing works like an inkjet printer. It is cool, but for this discussion, we will focus on the tried-and-true methodology.

There are a couple of different ways to apply solder mask to panels. Screening of the solder mask involves placing the boards in a tight mesh screen contraption—a rectangle with a wood or metal frame with the mesh stretched across it. We use a squeegee to apply the solder mask by pushing it through the mesh onto the board's surface with a uniform thickness.

With this process, we coat every square inch of the panel that can contain a circuit board, effectively flood-coating the entire side. To ensure we leave holes where the solder goes, we use a liquid photo-imageable solder mask (LPI) that allows us to transfer the solder mask file onto the board and make the solderable areas visible.

After thermally drying (a fancy way of saying baking) the panel to remove some solvents used, we transfer the image onto the board. We have two methods for doing this: photolithography and laser direct imaging (LDI).

The first method involves creating a film with all the board components such as solderable surfaces, through-holes, pads, and traces blacked out. We then run the boards through a developing process that removes the solder mask everywhere else. LDI achieves the same result by "marking" the LPI that needs to be removed during exposure to the laser and protecting the solderable areas from it.

After running through the chemical development process, we have a board that is the familiar green (or other color of choice) with the pads exposed. At this point, we have applied the solder mask and exposed it, but before we

final-cure the panel, we will put the silkscreen (legend) layer on top of it so there is a good bonding adhesion in place. Then, we bake the panel again to remove the remaining solvents. Once it comes out of the oven and cools, the solder mask becomes hard and durable, exposing all the solderable pads.

> "As with any phase of production, designers should be aware of what can go wrong during solder mask and how to prevent issues before they occur."

Solder mask has always been a relatively straightforward element of the manufacturing process, but as designs become tighter, high-speed requirements more frequent, and copper on the layers thicker, solder mask becomes a more critical part of the manufacturing process. In tight pitch areas of the board, designers need to be sure they have enough solder mask web or dam between fine pitch pads.

Most manufacturers can resolve and maintain a 2 to 3-mil wide web between pads. Keeping as much of the spacing between pads to accommodate a smaller dam or web between features is important. If pad spacing leaves something like a 1-mil web, most manufacturers will struggle to produce boards that meet design requirements. Narrow pad spacing can create solder bridging during assembly and shorting defects.

Why Are PCBs Green?

PCB boards can come in more than one color, but these days, they are often green. Green became the standard mostly because of the contrast of color it provides with other components of the board, such as copper traces. It offers the most visibly inspectable color to contrast the PCB's features.

Over time, manufacturing best practices increasingly aligned with using green solder mask during production, and now it is the predominant color for PCBs. Other colors were and are used for several reasons. Some manufacturers use different-colored boards to differentiate prototypes from production-ready boards, and many designers choose different colors for aesthetic reasons. For high performance, green is the best choice because it is the most well-understood across the industry.

Solder Mask Design Considerations

As with any phase of production, designers should be aware of what can go wrong during solder mask and how to prevent issues before they occur. Thickness can impact the manufacturing process, and so can the type of solder mask. When we get down to an impedance tolerance of plus or minus 5%, every little thing can have an impact, including the thickness and pigmentation of the solder mask. Solder pad shapes, sizes, and locations should allow sufficient room for solder mask webs and dams—considering the swell of the solder mask. Knowing your tolerances and making sure you have design consistency is key to a smooth solder mask process.

We are nearing the end of the manufacturing process and are ready for the surface finish. Keep an eye out for my next article on that subject. If you can't wait, listen to the Designing for Reality: Surface Finish episode of On the Line with... and to hear our in-depth conversation about solder mask and legend, please listen to episode 10. DESIGN007

Matt Stevenson is vice president and general manager of ASC Sunstone Circuits. To read past columns, click here. Download *The Printed Circuit Designer's Guide to... Designing for Reality* by Matt Stevenson and listen to the podcast here.

UHDI FUNDAMENTALS:

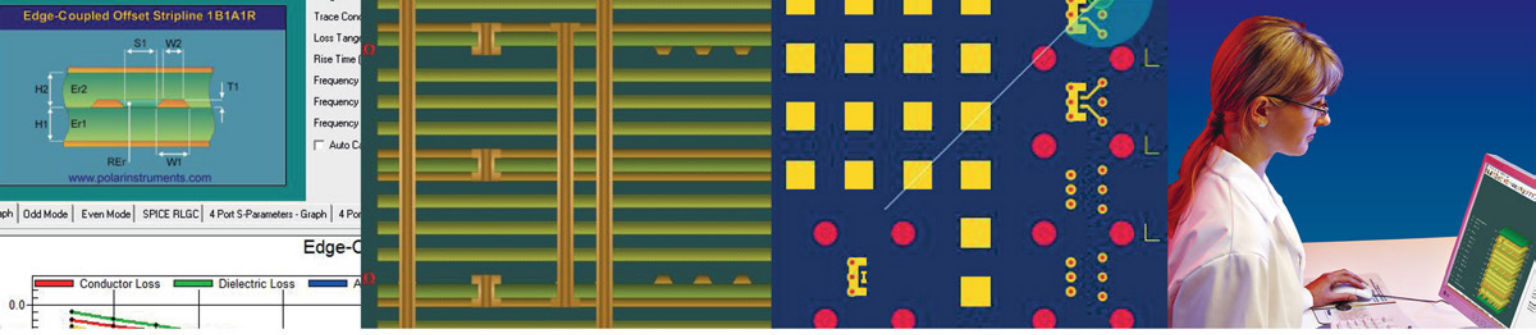
UHDI Bleeding-edge Manufacturing Applications, Part 2

Article by Anaya Vardya
AMERICAN STANDARD CIRCUITS

Ultra high density interconnect (UHDI) technology is transforming manufacturing by enabling compact, high-performance, and energy-efficient electronics in cutting-edge industrial systems. Its precision and scalability meet the demands of advanced manufacturing technologies. Here's another overview of bleeding-edge UHDI applications in manufacturing:

Smart Manufacturing and IoT-driven Automation

UHDI enables the miniaturization and performance enhancement of IoT sensors, which are the backbone of Smart manufacturing. With this level of automation, UHDI aids in integrating advanced security measures within IoT devices to prevent data breaches.



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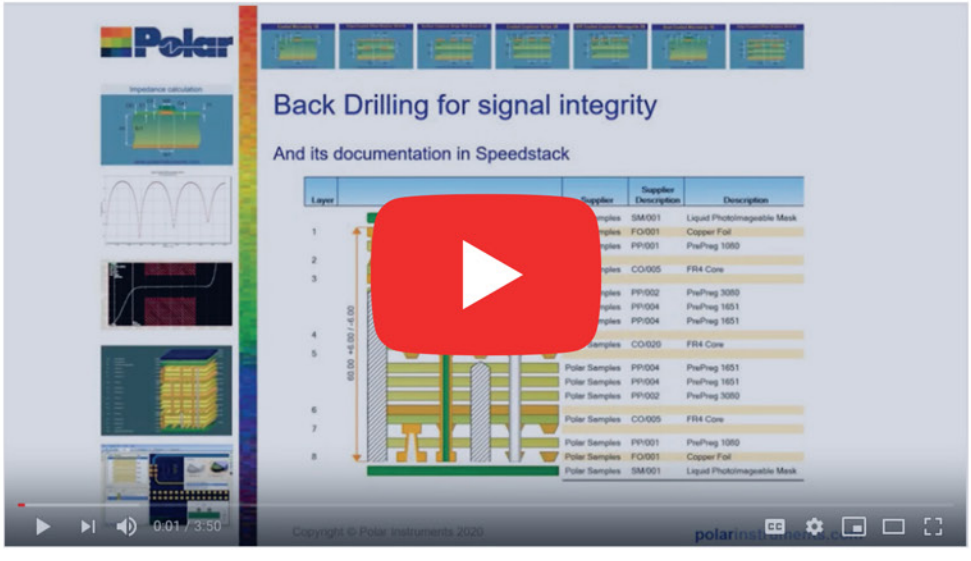

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- **High-density connectivity:** For edge computing devices that process data locally in smart systems
- **Energy-efficient controllers:** For powering distributed sensor networks
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- **Real-time data processing:** Dense circuitry ensures high-speed data acquisition and transmission
- **Durability:** Reliable connections for sensors operating in harsh factory environments
- **Hardware-based encryption modules:** Ensuring secure data transmission
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Smart manufacturing systems depend on seamless connectivity through high-speed communication:

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- **Low-power wireless chips:** Energy-efficient designs for battery-operated IoT devices
- **Compact antenna systems:** Enabling robust communication in limited spaces

Autonomous and Additive Manufacturing

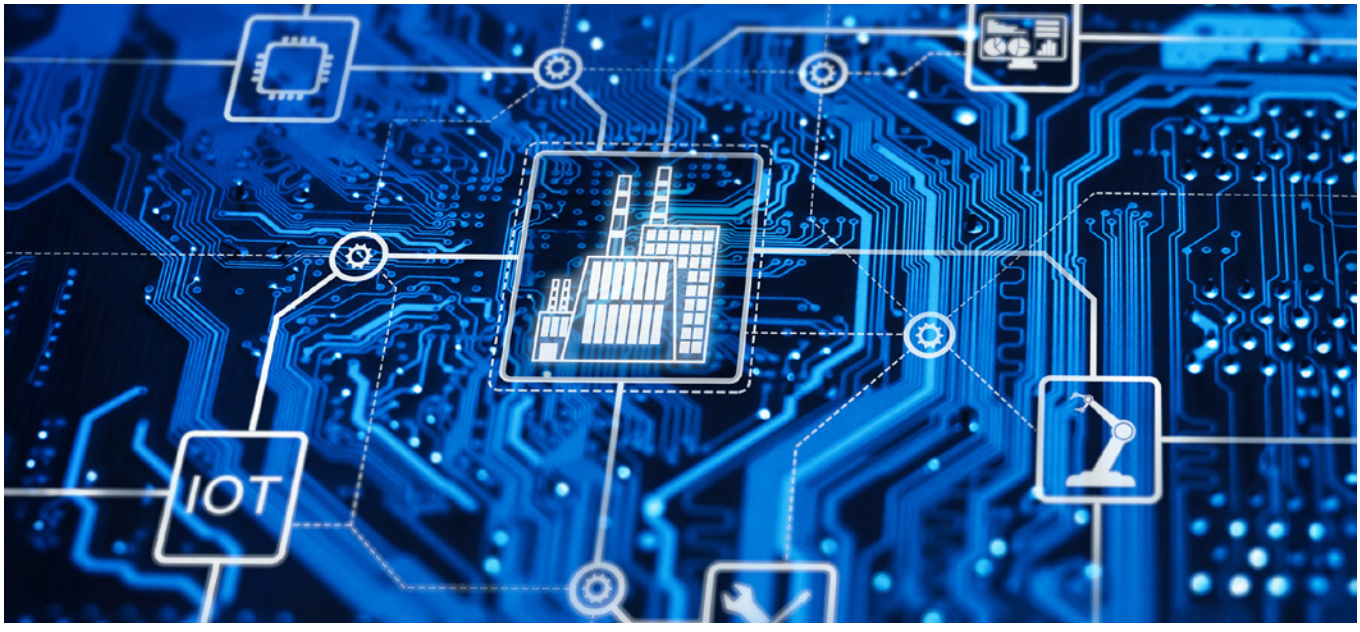
Smart factories require modularity for flexibility, and UDHI enables autonomous systems that adapt based on real-time data. Tools like UHDI-powered 3D printing systems enable compact, high-speed electronic controls:

Autonomous and Additive Manufacturing

- **Miniaturized control units:** Compact designs for precise motion control and decision-making
- **Sensor fusion:** Integration of data from multiple sources (e.g., cameras, LIDAR, and proximity sensors)
- **Dynamic optimization:** Real-time adjustments to production parameters

3D Printing Systems

- **Miniaturized driver boards** for precise control of print heads and stepper motors
- **High-resolution control units** for monitoring layer-by-layer material deposition
- **Real-time data processing modules** for adaptive manufacturing workflows
- **Compact modular systems:** Easily upgradable electronics for adaptive manufacturing setups



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AMBER

- Excellent bendability
- High Resolution by photolithography
- High Reliability
- Simplified process
- UL94 VTM-0 certified
- Low spring back force
- Resolution Line/Space=50/50μm
- Solder mask defined opening (30μm diameter)

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- **Plug-and-play devices:** Miniaturized, high-density circuits that integrate effortlessly into larger systems

Advanced CNC Machines

CNC (computer numerical control) machines require UHDI for high-performance control systems:

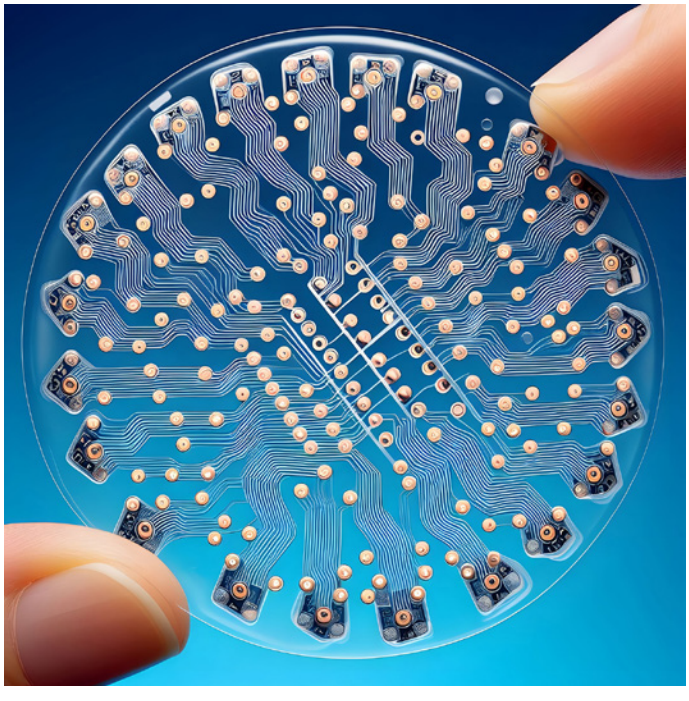
- **Dense interconnects:** For high-speed data processing and multi-axis coordination
- **Compact controllers:** With integrated motion planning algorithms
- **High-frequency circuits:** For real-time feedback and tool path adjustments

Flexible Electronics Manufacturing

UHDI is key in manufacturing flexible electronics like wearable sensors or foldable devices:

- **Thin, bendable PCBs:** They integrate UHDI for high-density connections
- **Precision assembly systems:** Handles delicate, flexible components
- **Energy-efficient drivers:** For low-power applications

Modern assembly lines demand high-speed and precise control, enabled by UHDI:



- **Miniaturized controllers:** For managing servo motors and actuators in compact spaces
- **Real-time monitoring circuits:** For error detection and quality assurance
- **Advanced motion control systems:** For synchronizing multiple components

Automation in logistics and manufacturing leverages UHDI in drones and AGVs:

- **High-performance navigation systems:** With integrated UHDI-based circuits for real-time obstacle detection
- **Compact battery management systems (BMS):** For extended operational hours
- **Wireless communication modules:** For seamless interaction with factory systems

Semiconductor and Chip Manufacturing

UHDI itself is instrumental in chip production, where extreme precision and density are required:

- **Compact lithography control units:** For precise etching
- **Integrated testing circuits:** For quality control in chip production
- **Robotic wafer handling:** Compact control systems for precise movement of wafers
- **Real-time monitoring:** UHDI circuits in equipment ensure process consistency
- **Data analytics modules:** Integrated UHDI components support AI-driven optimization of manufacturing processes
- **Automation systems:** Manage the wafer fabrication process
- **System-in-package (SiP):** UHDI enables dense interconnections between components like processors, memory, and power management chips
- **Chiplets integration:** Facilitates high-speed, high-density communication between chiplets in modular designs
- **3D packaging:** Supports vertical stacking of chips, providing interconnects for improved performance and reduced form factor

Environmental Monitoring in Factories

Factories require compact, durable monitoring systems and efficient energy management:

- **Multi-parameter sensors:** For air quality, temperature, and humidity
- **Low-power connectivity modules:** For remote data collection and reporting
- **Integrated AI systems:** For environmental optimization
- **Compact power management units:** Circuits for monitoring and optimizing power usage
- **Integrated battery systems:** Efficient designs for backup power in IoT devices
- **Renewable energy systems:** UHDI supports energy harvesting devices for self-powered sensors

Bleeding-edge UHDI applications in manufacturing enable transformative advances in precision, efficiency, and automation. From IoT-driven factory automation to factory environmental monitoring, UHDI is becoming a cornerstone of the smart factory revolution. The ability to transmit ultra-high-definition data in real-time allows manufacturers to enhance productivity, reduce errors, and implement advanced technologies, and as UHDI technology continues to mature, it will play an increasingly critical role in the future of manufacturing and Industry x.0. **DESIGN007**

Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals*. He is the author of *Thermal Management: A Fabricator's Perspective* and *DFM Essentials*. Visit *I-007eBooks.com* to download these and other free, educational titles.

Robots Could Help Close Surgeons' Skill Gaps and Improve Patient Outcomes


Ken Goldberg

Robots could soon play a larger role in surgery thanks to recent AI developments, experts said in a new Science Robotics paper published today.

Advances in generative AI and other areas could enable robots to assist human surgeons during certain tasks that require significant dexterity like suturing. Under an "Augmented Dexterity" approach, a human surgeon would closely oversee the robot's work and take over if needed.

"A surgeon's dexterity often separates the good surgeons from the great ones," wrote Ken Goldberg, UC Berkeley's William S. Floyd Jr. Distinguished Chair in Engineering, and Gary Guthart, Intuitive Surgical's chief executive officer. "Augmented Dexterity has potential to elevate good surgeons to the level of the best surgeons, which could support faster, and more reliable surgery."

This paper, "Augmented Dexterity: How robots can enhance human surgical skills," suggests one way the latest developments in artificial intelligence could be used to advance medicine and improve the health and wellness of society.

Surgeons already routinely use robots to conduct certain minimally invasive procedures. But the human determines almost every move the machine makes.

With Augmented Dexterity, robots would develop and place digital images of planned maneuvers on top of live images of the surgical field. A human surgeon would review, edit and approve the plan, then supervise as the robot executes it. This could be applied to tasks like suturing and debridement, areas where surgeons' skills vary and where small errors could harm patients.

EECS is shared by the Berkeley College of Computing, Data Science, and Society and the Berkeley College of Engineering.

(Source: University of California, Berkeley)

Another PCB Design Paradigm Shift in the Works

Flexbile Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Spend a half-century engaged in any kind of manufacturing technology, and you will see a boatload of change, especially in the realm of printed circuits. I can attest to this from personal experience.

While the precise date is contested, Paul Eisler is often credited with the invention of circuit boards in the 1930s, but the patent was suppressed for strategic reasons in the run-up to World War II. It was a military application (proximity fuses for mortar shells) that ushered in the mass production of printed circuits. Since then, the rapid advancement of technology (often still in service of the military's needs) has altered the landscape of PCB design over the years. We have shared and codified what we have learned into industry standards. The once tried, tested, and relied-upon "rules" are now being challenged by the ever-increasing complexity of electronic systems, driven by the pursuit of higher performance, smaller form factors, and lower power consumption—all at lower costs.

We all read from the same technology scriptures and sing from the same design hymnals that serve the global congregation of printed circuit manufacturers and users, though there are still a few iconoclasts and heretics to challenge them in the service of largely positive change. Even subtle changes are hard to effect. People, especially those in manufacturing, do not like change because it disrupts the manufacturing floor routine. However, change, as even the ancient philosophers knew, is constant and required for continued growth and evolution.

Here are some factors that have influenced and driven design rule changes:

Miniaturization: Small has long been a hallmark of electronics because it is the watershed from which flows almost every other benefit that we desire in our electronic products. Smaller is convenient, lighter, requires less energy, is higher performing because of proximity, and is more environmentally friendly.

Power/thermal management: Miniaturization is desirable but comes at a cost. Packing more electronics in closer proximity may improve size and performance and even battery life in portable products, but it also increases energy density and, therefore, heat generation, which needs to be managed. Heat is the product of

electron movement and the enemy of product reliability. This requires attention early on, not as an afterthought.

I have been developing ways to integrate thermal management into electronic assemblies and solve the thermal problem up front. This espouses ways to minimize heat damage to electronics by reversing the manufacturing process. Rather than building a printed circuit and assembling components on them, build heat-spreading component boards and then build circuits on them. This is one of the iconoclastic/heretical ideas alluded to earlier. It could be simpler and cheaper, however, it will also require more care up front and in the manufacturing process because rework and repair will be more challenging, if not impossible. Just as the nascent aerospace industry was often dangerous and even fatal, I believe we will adjust to deliver the promise through learned and shared experience. Change your thinking, change your outlook.

For the foreseeable future, signal integrity and timing constraint management will also require attention. With signals now nearing their practical limits based on physics, factors such as crosstalk, impedance mismatch, and delay variations are critical, and strict management of timing needs requires the designer to carefully consider things that were once of little concern. Matching trace lengths, via design, placement, construction, and even power plane design, is consequential. There are also concerns related to layer count. The number of layers in a PCB stackup and material selection can directly impact signal and power integrity, and thermal performance. Moreover, layer sequencing—the arrangement of signal, power, and ground layers—done incorrectly can create many signaling problems. Done correctly, it can minimize crosstalk, reduce impedance variations, and help control unwanted noise. On the bright side, electronic design automation and validation tools are rapidly evolving, and with increased availability and adaptation of AI to the design process, improvements will continue to accelerate.

Changes are coming at an accelerated pace. We must try to stay ahead of them or get run over. We must be the masters of our future rather than its victims.

The long-standing rules of PCB design are insufficient to address the challenges posed by current trends and new developments. As a result, new design methodologies, simulation tools, and manufacturing techniques are emerging to meet these requirements. To make it all work, we will need to engage in improved practices, including:

Creating a closer collaboration between PCB and system designers, packaging engineers, and manufacturing experts to ensure early design optimization. Several years ago, I wrote that it will be essential to optimize the design from the outset. To achieve this, we should design with manufacturing, rather than for manufacturing—DWM instead of DFM.

Using advanced simulation tools to analyze signal and power integrity, and thermal performance will help identify and mitigate potential issues early in the design process.

Everyone in the electronics industry will need to adapt to the rapid changes. Given the industry's breakneck speed of development, staying up to date with the latest technologies and design techniques will be essential to remaining competitive. By embracing these evolving principles and leveraging advanced technologies, PCB designers can push the boundaries of performance and innovation and have a great time while doing so. **DESIGN007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition*, and watch his in-depth workshop series "Flexible Circuit Technology."

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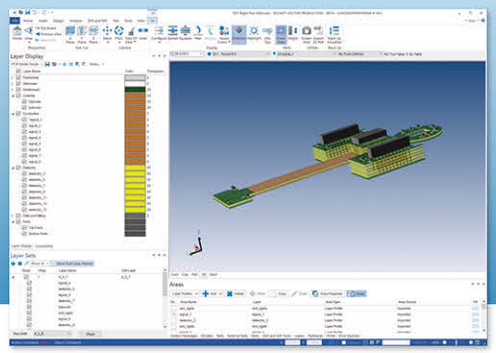

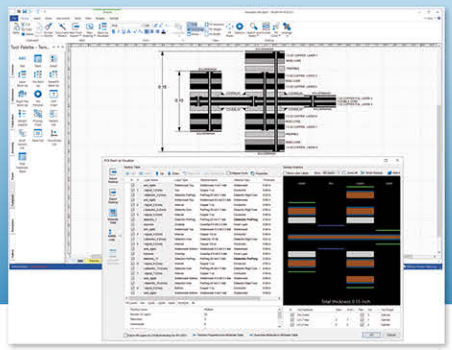

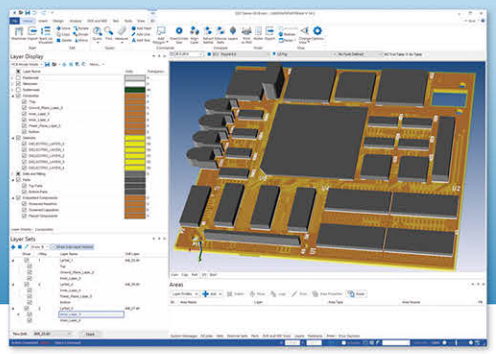

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TOP TEN

EDITOR'S PICKS

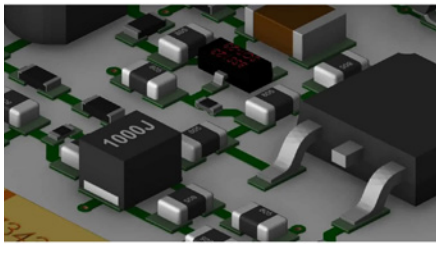
PCB Design Software Market Expected to Hit $9.2B by 2031

The printed circuit board (PCB) design software market is evolving rapidly as the global demand for semiconductors and electronic devices continues to surge. PCB design software is critical in the electronics industry, allowing engineers to design, simulate, and optimize PCBs used in a variety of devices, including consumer electronics, automotive systems, medical devices, and communication equipment.

Understanding Depreciation for Electronic Manufacturers

As a PCB design engineer, your focus is on creating innovative, cost-effective designs. However, the financial aspects behind your designs—such as depreciation—play a significant role in the overall business. Most people don't fully understand the meaning of depreciation, especially young engineers and designers entering the field, yet when it comes to calculating the total cost to manufacture or the total cost to operate, it is an important financial piece of the total manufacturing cost algorithm. Here's a breakdown of depreciation from a financial controller's perspective, aimed at those less familiar with accounting.

PCB Layout Rules of Thumb for Consideration



Just because a "rule of thumb" is usually based on experience instead of precise facts doesn't negate its value. For instance, when I told my kids that a good rule of thumb was not to back-talk to their mother, they discovered very quickly how accurate my advice was once they crossed that line.

Elementary, Mr. Watson: Rules of Thumb—Guidelines vs. Principles for PCB Design

The infamous "rules of thumb" are simple guidelines that help you make decisions based on experience, not exact facts. They're like shortcuts we use because they work most of the time. For example, if you want to know if spaghetti is done cooking, a common rule of thumb is to grab a spaghetti strand and throw it against the wall to see if it sticks.

Meet Polar's New Product Specialist Jess Hollenbaugh

At PCB West, Andy Shaughnessy spoke with Jess Hollenbaugh, a recent college graduate who has now joined Polar Instruments. In this interview, she shares her journey from a physics student focused on high-energy astrophysics to her new role at Polar.

Rules of Thumb for PCB Layout

The dictionary defines a "rule of thumb" as "a broadly accurate guide or principle, based on experience or practice rather than theory." Rules of thumb are often the foundation of a PCB designer's thought process when tackling a layout.

Beyond Design: High-speed Rules of Thumb

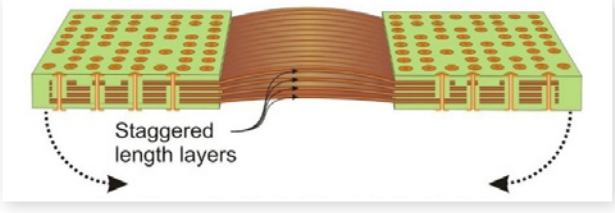
The most popular rule of thumb is probably, "Rules are meant to be broken." This implies that there are times when we should think for ourselves and not obey every rule presented to us blindly. I find that with every PCB design I complete, there is at least one rule that needs to be broken to accommodate a certain situation. All board designs are different.

Global PCB Connections: A Technical Overview of Long-flex Printed Circuit Boards

Flex printed circuit boards are an essential advancement in the electronics industry, enabling the development of flexible, lightweight, and durable electronic designs. As technology has evolved, long-flex PCBs have emerged as a key component in applications requiring extended or intricate routing paths.

Flexible Thinking: Rules of Thumb—A Word to the Wise

In the early days of electronics manufacturing—especially with PCBs—there were no rules. Engineers, scientists, and technicians largely felt their way around in the dark, making things up as they went along. There was a great deal of innovation, guessing, and testing to make sure that early guidelines and estimates were correct by testing them. Still, they frequently made mistakes.



Standard of Excellence: Hiring for Quality Positions in Manufacturing, Engineering, and Management

In continuing my series on finding, signing, and keeping good people for your company, this month we discuss hiring good people for your quality department. Even when hiring was easier, hiring for the quality department has always been especially challenging.

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For just $975, your 200-word, full-column ad will appear in the Career Opportunities section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, suppliers and the academic community.

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Career Opportunities

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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ACE
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PCB Manufacturing Technician

Join the Team at Accurate Circuit Engineering!

Located in Santa Ana, California, Accurate Circuit Engineering (ACE) delivers high-quality PCB solutions with a focus on innovation and precision.

Role: Accurate Circuit Engineering is looking for detail-oriented PCB Manufacturing Technicians for all areas in PCB manufacturing. Responsibilities include operating manufacturing equipment, performing quality checks, and documenting production data.

Qualifications:

- High school diploma or equivalent; technical training preferred
- Experience in PCB manufacturing or electronics assembly a plus
- Strong attention to detail and ability to follow instructions
- Familiarity with PCB manufacturing and testing tools is advantageous

What ACE Offers:

- Competitive wages and benefits
- Career growth opportunities
- Supportive work environment with comprehensive training

To apply, send your resume and cover letter to sales@ace-pcb.com with the subject "PCB Manufacturing Technician Application."

Accurate Circuit Engineering is an equal-opportunity employer and values diversity in the workplace.

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Career Opportunities

Europe Technical Sales Engineer

Taiyo is the world leader in solder mask products and inkjet technology, offering specialty dielectric inks and via filling inks for use with microvia and build-up technologies, as well as thermal-cure and UV-cure solder masks and inkjet and packaging inks.

PRIMARY FUNCTION:

1. To promote, demonstrate, sell, and service Taiyo's products
2. Assist colleagues with quotes for new customers from a technical perspective
3. Serve as primary technical point of contact to customers providing both pre- and post-sales advice
4. Interact regularly with other Taiyo team members, such as: Product design, development, production, purchasing, quality, and senior company managers from Taiyo group of companies

ESSENTIAL DUTIES:

1. Maintain existing business and pursue new business to meet the sales goals
2. Build strong relationships with existing and new customers
3. Troubleshoot customer problems
4. Provide consultative sales solutions to customer's technical issues
5. Write monthly reports
6. Conduct technical audits
7. Conduct product evaluations

QUALIFICATIONS / SKILLS:

1. College degree preferred, with solid knowledge of chemistry
2. Five years' technical sales experience, preferably in the PCB industry
3. Computer knowledge
4. Sales skills
5. Good interpersonal relationship skills
6. Bilingual (German/English) preferred

To apply, email: BobW@Taiyo-america.com with a subject line of "Application for Technical Sales Engineer".

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Service Engineer: Chicago

Join the Schmoll America Team as a Service Engineer—Where Innovation Meets Customer Excellence! Are you a technical mastermind with a passion for solving complex problems and delivering exceptional customer experiences? Look no further than Schmoll America!

We're looking for engineers to work in the Chicagoland area.

As a Service Engineer, you'll be the driving force behind our customers' success, providing top-notch technical support and maintenance services for our PCB industry-leading equipment.

What you'll do:

- Install, commission, and maintain Schmoll equipment at customer sites
- Troubleshoot and repair equipment with ease and precision
- Provide technical training and tailored applications solutions to customers

What we offer:

- A dynamic and supportive work environment where your voice matters
- Opportunities for professional growth and development in a cutting-edge industry
- A competitive salary and benefits package
- The satisfaction of knowing you're making a real difference in our customers' lives

What we're looking for:

- Engineering degree preferred
- 3+ years of experience in an engineering role
- Strong technical knowledge of electrical and mechanical systems
- Excellent problem-solving and analytical skills
- Willingness to travel (up to 75%) to customer sites and HQ in Germany

If you're a motivated professional looking for a challenging and rewarding role, we want to hear from you! Please submit your resume and cover letter to HR@SchmollAmerica.com.

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Career Opportunities

The Test Connection, Inc.

Sr. Test Engineer (STE-MD)

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

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The Test Connection, Inc.

Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/ Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

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Career Opportunities

BLACKFOX
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IPC Instructor
Longmont, CO

This position is responsible for delivering effective electronics manufacturing training, including IPC certification, to adult students from the electronics manufacturing industry. IPC Instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC certification programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will primarily conduct training at our public training center in Longmont, Colo., or will travel directly to the customer's facility. It is highly preferred that the candidate be willing to travel 25–50% of the time. Several IPC certification courses can be taught remotely and require no travel or in-person training.

Required: A minimum of 5 years' experience in electronics manufacturing and familiarity with IPC standards. Candidate with current IPC CIS or CIT Trainer Specialist certifications are highly preferred.

Salary: Starting at $30 per hour depending on experience

Benefits:
- 401k and 401k matching
- Dental and Vision Insurance
- Employee Assistance Program
- Flexible Spending Account
- Health Insurance
- Health Savings Account
- Life Insurance
- Paid Time Off

Schedule: Monday thru Friday, 8–5

Experience: Electronics Manufacturing: 5+ years (Required)

License/Certification: IPC Certification–Preferred, Not Required

Willingness to travel: 25% (Required)

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Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB manufacturer located in Tucson, AZ, is looking for sales representatives for the Utah/Colorado, and Northern California territories. With 35+ years of experience, our PCB manufacturing capabilities reach far beyond that of your typical fabricator.

Reasons you should work with Prototron:
- Solid reputation for on-time delivery (98+% on-time)
- Capacity for growth
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- 5-day standard lead time
- RF/microwave and special materials
- AS9100D
- MIL-PRF- 31032
- ITAR
- Global sourcing option (Taiwan)
- Engineering consultation, impedance modeling
- Completely customer focused team

Interested? Please contact Russ Adams at (206) 351-0281 or russa@prototron.com.

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Career Opportunities

ARLON ELECTRONIC MATERIALS

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- **Engineering**
- **Quality**
- **Various Manufacturing**

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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INSULECTRO

Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers to build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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Career Opportunities

MivaTek Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
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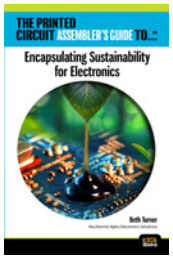

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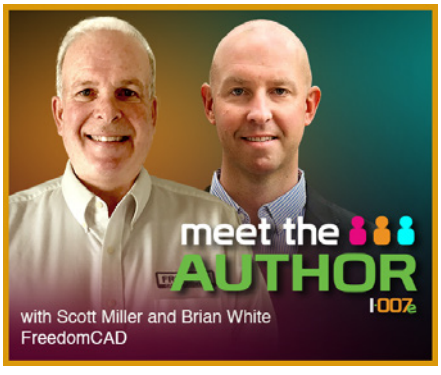

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COVER IMAGE: **ADOBE STOCK © VIKTOR**

DESIGN007 MAGAZINE

DESIGN007 MAGAZINE®
is published by IPC Publishing Group, Inc.
3000 Lakeside Dr., Suite 105N, Bannockburn, IL 60015

December 2024, Volume 13, Number 12
DESIGN007 MAGAZINE is published monthly
by IPC Publishing Group, Inc., dba I-Connect007

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