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I-Connect007

DESIGN007 MAGAZINE

Embedded Design Techniques

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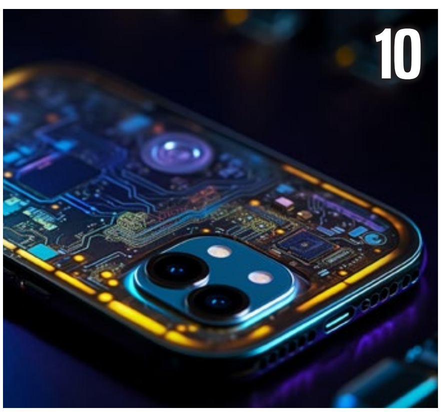
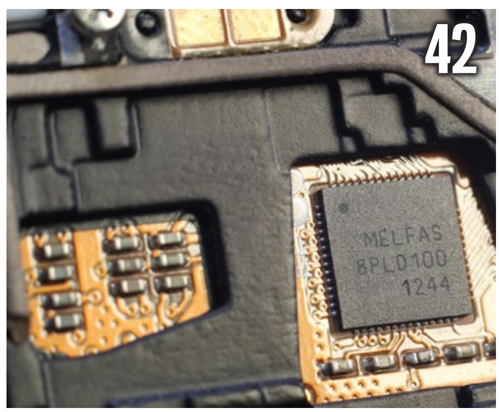
In this issue, our expert contributors lay down the foundation of knowledge that designers need to be aware of to make intelligent, educated decisions about embedded design. They discuss the many design and manufacturing hurdles that can trip up designers who are new to this technology and provide an array of solutions.





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In Bed With Embedded

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

We're always hearing about PCB technology running into a wall. On the design side, Moore's Law hit one such wall. On the fab side, features are now so tiny that the traditional subtractive methods have hit another type of wall. And we see OEMs who never planned to use flexible circuits wind up embracing them, because rigid boards just won't fit into a new product's form factor.

Similarly, the popularity of embedded components results from technology hitting a wall, or a series of walls. If your board's skyline faces height limitations, and/or reliability is paramount, embedding components into the layers of the PCB is a great way to go.

Now, embedded components are found in everything from smartphones to health monitor bracelets. But there are several design

and manufacturing hurdles that can trip up designers who are new to this technology.

In this issue, our expert contributors lay down the foundation of knowledge that designers need to be aware of to make intelligent, educated decisions about embedded design.

We start with a conversation with IPC's Kris Moyer, who teaches embedded design techniques. He provides an overview of the design and manufacturing steps related to embedding components. John Andresakis discusses embedded resistor copper foils, their design challenges and benefits, and some resources available to designers working with embedded components. Next, columnist Vern Solberg offers some handy tips, tricks, and techniques for designing with embedded components. Stephen Chavez explains how designers can "unleash the power" of embedded components and make their boards more reliable and often less costly—with the right pre-planning.

Cody Stetzel has a feature that outlines all the different types of embedded capacitors on the market today. Columnist Barry Olney takes a signal integrity engineer's view of embedded capacitance materials and breaks down their challenges and benefits. Our own PCB historian, Joe Fjelstad, traces the development of embedded component technology from its postwar roots through today.

We'll bring you coverage of DesignCon and IPC APEX EXPO in the next few months, so stay tuned. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 23 years. To read past columns, click here.

Cadence Advances ECAD/MCAD Convergence with Celsius Studio AI Thermal Platform

Cadence Design Systems has announced Cadence Celsius Studio, the industry's first complete AI thermal design and analysis solution for electronic systems. Celsius Studio addresses thermal analysis and thermal stress for 2.5D and 3D-ICs and IC packaging, in addition to electronics cooling for PCBs and complete electronic assemblies. While current product offerings consist mostly of disparate point tools, Celsius Studio introduces an entirely new approach with a unified platform that lets electrical and mechanical/thermal engineers concurrently design, analyze and optimize product performance without the need for geometry simplification, manipulation and/or translation.

The industry's first complete AI thermal design and analysis solution for electronic systems, Cadence Celsius Studio addresses thermal analysis and thermal stress for 2.5D and 3D-ICs and IC packaging, in addition to electronics cooling for PCBs and complete electronic assemblies.

The industry's first complete AI thermal design and analysis solution for electronic systems, Cadence Celsius Studio addresses thermal analysis and thermal stress for 2.5D and 3D-ICs and IC packaging, in addition to electronics cooling for PCBs and complete electronic assemblies.

Celsius Studio brings a new system-level thermal integrity solution into the marketplace, converging electro-thermal co-simulation, electronics cooling and thermal stress into one cohesive offering.

(Source: Cadence Design Systems)

Every Designer Needs to Understand Embedded

Feature Interview by the I-Connect007 Editorial Team

As the size of electronic devices continues shrinking, more PCB designers consider embedding components in the PCB itself. This not only reduces the skyline of the board, but has the added effect of increasing the board's overall reliability.

IPC's Kris Moyer teaches design techniques for embedding components, and he's noticed an upswing in his students' interest in embedded component design. We recently spoke with him about embedding component design: best practices, pros and cons, and when it makes sense for designers to start embedding.

Andy Shaughnessy: I understand you've had a lot of interest in embedded components in your design classes. What are students curious about?

Kris Moyer: Some interesting student questions have all been related to embedded components, especially about the viability of the embedded for high reliability. They ask, "How viable and reliable are the embedded resistors, cavities, and so on for military applications or stuff that has to go into space?"

When they ask, "Is this an additive process?" I respond that it's a subtractive process for

embedded resistors. There are a lot of processing, reliability, and design questions. There's the trade-off question, too: At what point does it make more sense to embed resistors vs. just shrinking down to, say, an 0105? Is it better to take the cost into the embedded process?

Shaughnessy: I think some people are wary of the cost of getting involved with embedded components, even though it can save money in the long run.

That's one of the trade-offs. There's an initial design and manufacturing cost to get into the embedded design techniques. But once you're in, you will see improvements in the long run. You won't have as many failed boards; you can reduce size and item count. On the other hand, without embedded resistors, if I have to make enough room on my board, even using double-sided placement, to have 1,000 physical resistors on there, how much bigger does my board need to be? How much more does my product need to cost, and what about the weight? If I can take off 1,000 resistors, even at a penny each, that's still $10 per board.

Nolan Johnson: When does it make sense to go with embedded?

One of the biggest trade-offs when you're considering embedded is actually the silicon geometry. The problem is that as the silicon has decreased, the rise times are faster. While you're transitioning from zero to one or one to zero, and you're either rising or falling, you're actively driving the transmission line. Therefore, you don't necessarily need to worry about reflections or crosstalk. When you exceed that distance, now you have to worry about it. As the rise times have gotten faster, the distance the signal travels is now smaller, to the point that for some leading-edge boards, rise times were nearly 100 picoseconds.

But with a BGA, you typically can't get a physical resistor close enough, because if the pin is coming out on rows 3, 4, or 5 close to the core of the BGA, the physical resistor has to be outside the body of the BGA. This means the whole distance that the signal has to travel, even on an inner layer, to get to the resistor is farther than that TTL. Now, the only way to get my signal integrity is to do the embedded resistor, so cost has nothing to do with it anymore.

There are some really great materials out there, and I encourage my students to use them because they're worth it.

Shaughnessy: How does the material selection affect all this?

The material has some influence on embedding components. If we go to the higher-end materials where the dielectric constants are in the low 3s and 4s, you get a little more room, but not much. Unless you start going into the RF materials—PTFE and other thermoplastics—you don't get into the low enough dielectrics to really help much. But yes, material selection will matter if you use the classic low-cost board materials that have dielectric constants in the 4.0 to 4.5 range. We're basically past the point of no return. There are some really great materials out there, and I encourage my students to use them because they're worth it. These right times are so ridiculously fast.

There are plenty of good white papers and design guides from the manufacturers of embedded materials. But normally, when picking a resistor or capacitor, the datasheet has a defined spec for the power dissipation and voltage rating for these devices. With the embedded components, you now have to calculate all that, and there are various trade-offs because it's now a material vs. component situation. There's a lot of information that's needed: power dissipation, voltage drop, current rating, current density, etc.

Shaughnessy: How do you test a component embedded in the board? That sounds like it could be problematic.

Normally, when I'm designing for test, I want to have 100% of the nodes available with a test point. But if I start putting formed resistors in line with a trace on an inner layer, I no longer have 100% unique component testability. I only have chain testability.

Let's assume it's a QFP. The QFP comes out, goes through a full through-via, and gets to an inner layer. Then we attach our resistor to the via, and downstream from the resistor we get to another point. Now I have to go from the pin of the device through one embedded resistor, or maybe two embedded resistors before I hit another via that comes back to the surface for testing those two or three resistors. So, there are DFM challenges when you're doing embedded.

Johnson: How do today's CAD tools handle embedding components?

I can speak to Altium, which does not directly support the embedded workaround that I teach my students. Altium supports the cavities—the embedded as physical parts and cavities. When making and defining that footprint, you can say, "Here are my surface mount pads, and my solder mask." Altium allows you to put the footprint on layer three or whatever of the board, and you can define cavity features. What it does not support right now is formed resistors, but you can get around that manually by adding the layer definition. I can define those as my mask layers for the resistor opening in the resistor definition itself and just add those two component layers. So, there are workarounds for that.

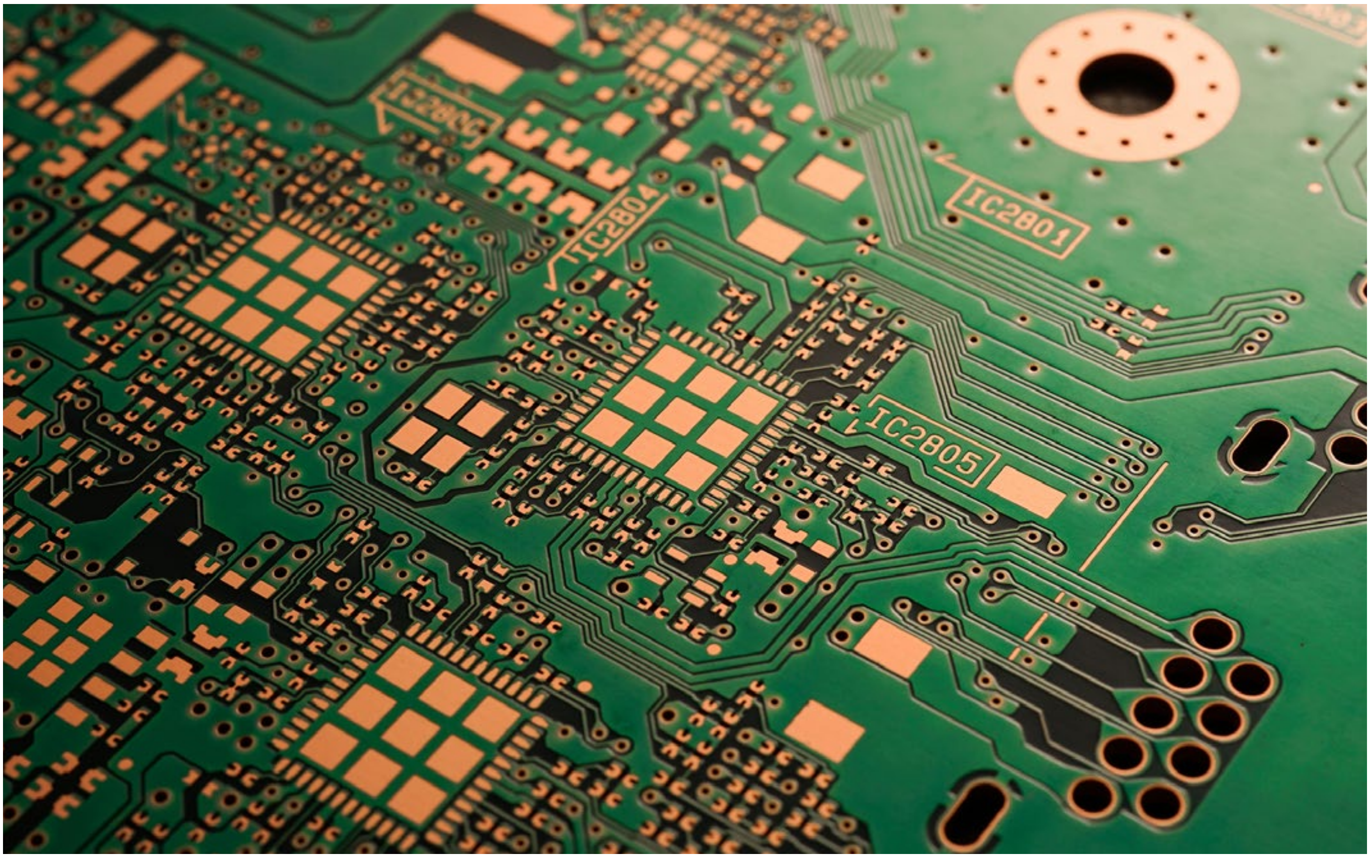
Kris Moyer

Shaughnessy: Is there anything else you'd like to add, Kris?

I'm glad to see my students interested in embedded components. This is something that every designer must be aware of because even in run-of-the-mill commercial digital products, the silicon guys keep making silicon so small. Every PCB designer needs to be able to deal with signal integrity, and the only way we can deal with signal integrity moving forward is with embedded resistors. The traditional techniques we used are becoming not quite obsolete, but certainly ineffectual because of the rise time issue. Embedding components is something that every designer will have to do. It might not be on a daily basis, but they must be at least cognitively aware that they need to consider this process.

Shaughnessy: Thanks for your time, Kris.

Thank you all. I enjoyed it. DESIGN007



Embedded Design: Materials Matter

Feature Article by John Andresakis
QUANTIC OHMEGA-TICER

The rapid advance of mobile technologies has sparked an insatiable demand for radio spectrum bandwidth. The rush to capitalize on wider bandwidths, higher data rates, and lower latency offered by frequency bands like 5G and millimeter wave is evident across industries. Cellular 5G and 6G networks, low-Earth orbit (LEO) and mid-Earth orbit (MEO) satellites, interconnected devices (IoT), autonomous vehicles, and even defense and environmental monitoring systems are driving this paradigm shift. To manage the influx of signals from these diverse applications, antennas, and sensors are undergoing a critical evolution, becoming increasingly sophisticated and miniaturized.

To ensure high data rate connectivity in this complex landscape, broadband high-gain antennas are experiencing a significant transformation. Traditional dish and horn antennas give way to flat-panel active electronically steered arrays (AESA) for beam-forming and massive MIMO designs. These AESA arrays, capable of shaping azimuth, elevation, and antenna patterns on demand, are vital for directing beams toward specific devices and maximizing signal efficiency. To accommodate this shift, the RF industry has rapidly developed new integrated circuits, materials, processes, and equipment to build reliable and accurate devices for these mission-critical sensor applications.

Much of the engineering expertise behind these modern AESA systems draws inspiration

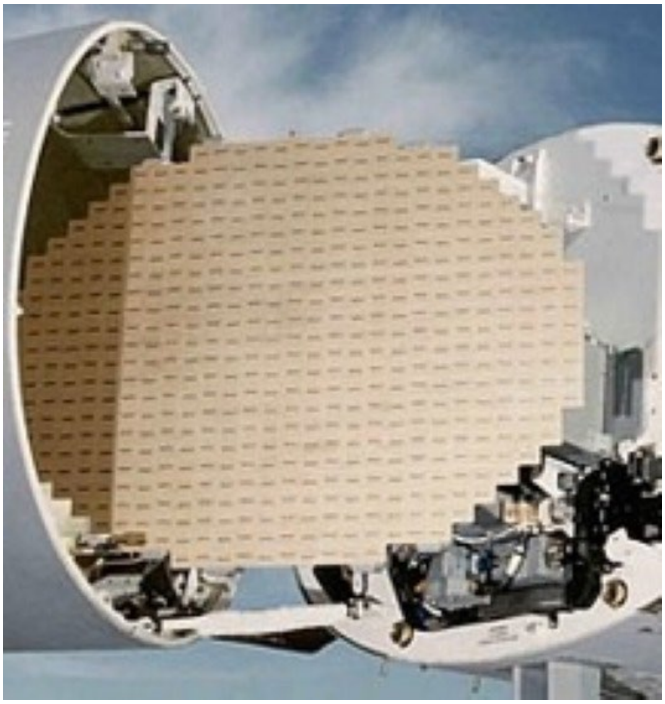


Figure 1: An example of a flat-panel active electronically steered array (AESA) radar system.

from phased array antennas and Ka/Ku-band radar technologies typically used in defense applications. These robust systems have paved the way for AESA products that can dynamically control beam direction and target specific communication devices. However, as these technologies migrate from the defense and space sectors to commercial markets, challenges arise for designers who may not have extensive experience with AESA systems. One particular concern involves managing the limited surface area on PCBs while adhering to tighter routing requirements and accommodating a higher layer count.

Fortunately, a solution exists in the form of embedded resistor copper foils. These innovative materials seamlessly integrate resistors directly into the inner layers of the PCB, freeing up valuable surface space for active components. This frees designers from the constraints of discrete SMT resistors, enabling them to create smaller, lighter, and more efficient PCBs for high-frequency applications.

Beyond the immediate space savings, embedded resistors offer a multitude of advantages:

- **Simplified design and manufacturing.** By eliminating the need for additional components, soldering, and routing vias, embedded resistors streamline the PCB design and manufacturing process. This translates to faster turnaround times, reduced assembly errors, and improved overall manufacturability.
- **Improved electrical performance.** Reduction in parasitic capacitance and inductance is realized compared to surface mount components with reduced metal-to-metal transitions and elimination of vias on critical nets.
- **Enhanced PCB reliability.** The integration of resistors within the PCB layers during lamination strengthens the entire structure. This results in enhanced mechanical and electrical stability, leading to longer component lifespans and increased system reliability.
- **Cost optimization.** Although the copper foil itself incorporates the resistors, their presence doesn't necessitate additional material and only requires a few additional processing steps. This eliminates the need for discrete SMT resistors and their associated procurement, storage, and placement costs, contributing to overall cost savings.
- **Reduced PCB size and weight.** The thin-film nature of embedded resistors allows them to reside within existing PCB layers without increasing overall thickness or requiring internal cavities. This enables the creation of smaller, lighter boards, crucial for applications like handheld devices and satellites where every gram counts.
- **Resistive "blank slate."** Utilizing the printed circuit board imaging process allows the foil to be customized into various structures. This enables it to be used as a radar-absorbing material, in resistive cards (R-cards) as well as high-impedance surfaces (HIS) and frequency-selective surfaces (FSS).

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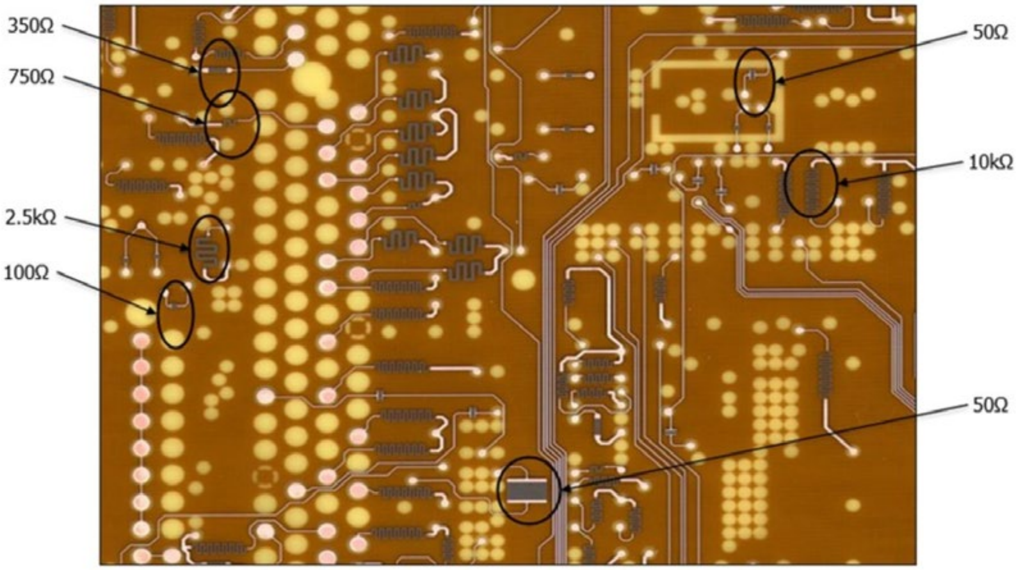

Figure 2: A PCB with varying resistor values of 100 ohms/square.

However, designing with embedded resistors requires careful consideration of several factors:

- **Resistance value and geometry.** The sheet resistance of the resistor material (Rs) and the geometry of the etched resistor path determine the final resistance value. Designers can choose from various patterns and shapes, such as bar, serpentine, circular, or arc, to achieve the desired resistance.
- **Power handling and tolerance.** Embedded resistors have power handling limitations similar to their discrete counterparts. Choosing the appropriate resistor size and material ensures reliable operation without overheating or exceeding tolerance limits.
- **Design tools and resources.** Fortunately, manufacturers of embedded resistor foils provide valuable design tools and resources to guide engineers through the selection and implementation process. These tools aid in determining resistor dimensions, power dissipation, and tolerance based on specific design requirements.

The manufacturing process for embedded resistors involves precise photoresist application, exposure, development, and etching steps. The specific resistor alloy used, such as NiCr, NiP, NCAS, or CrSiO, influences the process parameters and final properties of the resistors. Careful control of the ohms per square (OPS) sheet resistance ensures consistent performance across production batches.

Quantic Ohmega-Ticer offers several copper foil types including those with low-profile roughness for high-frequency circuit boards, minimizing signal loss. Their resistors work across diverse materials and applications. Final resistance tolerance depends on resistor foil tolerance, lamination effects, and PCB etching precision.

There are 70+ fabricators worldwide that offer reliable mass production of high-quality embedded resistors. Various resources, including a resistor calculator, help designers achieve desired tolerances and manage thermal dissipation. Their technology tackles space, packaging, and electrical challenges for millimeter-wave applications in both defense and commercial markets. DESIGN007

John Andresakis is director of business development for Quantic Ohmega-Ticer.


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Tips and Tricks for Embedding Resistor Components

Designers Notebook

Feature Column by Vern Solberg, CONSULTANT

The printed circuit has traditionally served as the platform for mounting and interconnecting active and passive components on the outer surfaces. Companies attempting to improve functionality and minimize printed circuit board size now consider embedding a broad range of components within the circuit structure.

The fact is that more than 70% of the components occupying space on a typical printed circuit board are passive (resistors, capacitors, inductors). Although most discrete passive components on a board's surface will have small outlines, they can occupy up to 50% of its surface area. A key issue is dealing with the shrinking surface area required on the circuit board for passive components and the interconnect complexity of the larger, higher I/O components sharing the same space. The solution for many applications is to distribute most of the passive components directly onto the circuit pattern within the subsurface layers of the multilayer circuit board.

Processes have steadily evolved for embedding and interconnecting a wide range of common passive components: resistor, capacitor, and inductor elements. The materials incorporated into the circuit board during manufacture become an integral part of the PCB's structure. Graphically represented in Figure 1 are examples of the most common formed passive components that may be considered for embedding.

- **Formed resistors:** Several companies have developed material sets and fabrication processes for forming thick- and thin-film resistor elements.
- **Formed capacitors:** The capacitor dielectric separating the copper surfaces of the power and ground plane is an organic polymer thick film or ceramic thin film composite.
- **Formed inductors:** A specific inductance can be formed within the copper circuit pattern, configured in a spiral-like geometry.

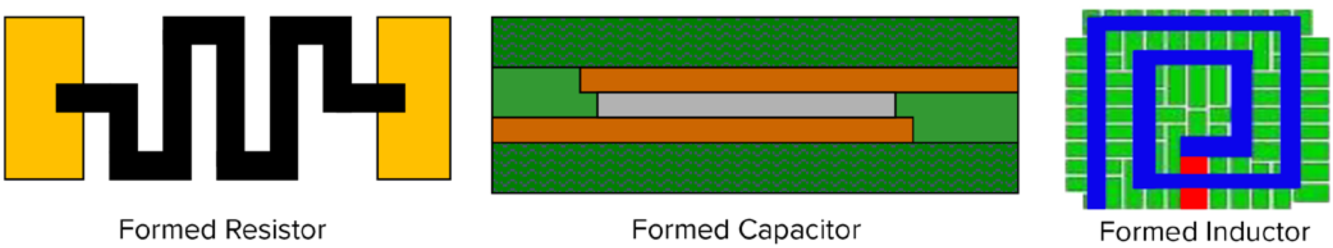


Figure 1: Formed passive component examples.

Resistors, in particular, tend to dominate the surface area of the circuit board, often restricting the circuit paths between active components. So, transferring most of the resistor elements onto subsurface layers of the circuit board allows the designer to optimize semiconductor placement, provide more area for circuit interconnect, and ultimately achieve the most efficient interconnect between principal functions.

Planning for Embedded Resistors

The first step during the planning phase of the circuit board is to select and identify on the schematic the most logical components for embedding. These will include components closely coupled to related active device(s) on the circuit board's outer surface(s). Next, consider the value range and tolerance limits specified for passive functions. Formed passive resistors, for example, will have a limited tolerance range, while the discrete passive components designed for placement and solder attachment onto the outer surfaces of the circuit board can furnish significantly more value choices and greater tolerance parameters.

Embedding Formed Resistor Elements

Formed resistor elements may be furnished either as a printed or deposited thick-film composition or an imaged and chemically etched thin-film process.

- Thick-film resistor materials are formulated to furnish a wide range of primary values and are successfully used for a broad number of commercial applications. The resistor formulations are based on carbon-filled polymer chemistry that enables screen printing or pattern deposition to form the elements directly onto termination lands furnished on a designated circuit board layer.
- Thin-film resistor elements are formed using thin copper foil sheets pre-coated with a resistive material. The resistor layer is pre-deposited onto the copper sheet material using vapor disposition or electroplating. Both processes ensure uniformity of the resistor base value across the entire sheet.

Initial planning for embedding formed resistors:

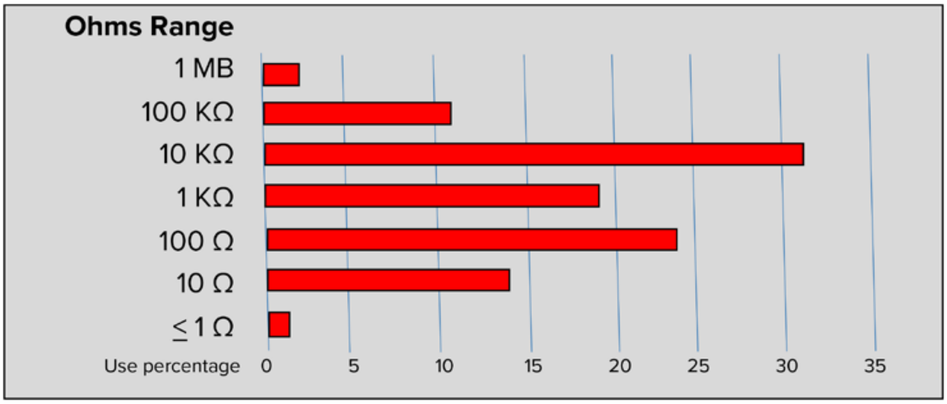
1. Identify resistors for embedding.
2. Establish R-value and target tolerance.
3. Determine the power rating requirement.
4. Define finished element geometry.
5. Select location (layer) and orientation.

When identifying candidate resistors for embedding, the designer must consider the resistor value range, the allowable tolerance range, and the application. The thick-film resistor forming process is employed where tolerances are less critical, primarily used in digital and analog circuit applications for terminating resistors, current limiting, transistor biasing, and for pull-up/pull-down resistors where value tolerances that range between 5–10% will probably meet the operational criteria of the final product.

On most printed circuit board designs, resistor value distribution will vary between 1 ohm at the low end and 10M ohms at the highest. Selecting the most practical composition for the thick-film resistors, the circuit board designer should consider the most prominent base-value usage and select a material that facilitates the lower end of the value range. From a statistical standpoint, the greater number of resistors in a digital or analog circuit will probably fall between 10 ohm and 10K ohm, as illustrated in Table 1. With that in mind, selecting the 10-ohm material as the base value will provide greater flexibility in expanding the resistor geometry to accommodate a wide range of finished resistance values.

The geometry of the resistance material can be a simple rectangle, or a serpentine shape designed to maximize resistor element length while minimizing area. In each case, the resistance material must terminate or overlap with the copper lands furnished within the circuit pattern.

Table 1: Distribution ratio by resistor value



Calculating Formed Resistor Geometry

Both thick- and thin-film resistor materials are formulated to furnish a wide range of primary values. Although resistor element geometry can be developed by the designer mathematically, software tools are also available that can automatically calculate the embedded resistor geometry based on inputs for ohms, power, and tolerance. The calculated values are based on the resistance measured between the opposite edges of a square. For example, a single square of 1KW material printed or deposited between two copper lands will provide a 1KW resistor element, while a pattern of the same 1KW material that is twice the length or two squares furnishes a 2KW resistor, and two- and one-half squares (Figure 2) will provide a 2.5KW.

Suppliers recommend that designers furnish resistor widths and lengths that are no less than 0.25 mm (0.010"). Increasing the resistor elements' dimensions, on the other hand, will reduce print variations and help in achieving the final resistor target values and tolerance accuracy. Additionally, when terminating the thick-film resistor elements, the land pattern geometry provided on the surface for resistor termination should allow for a nominal 0.25–0.50 mm overlap of the deposited resistor material.

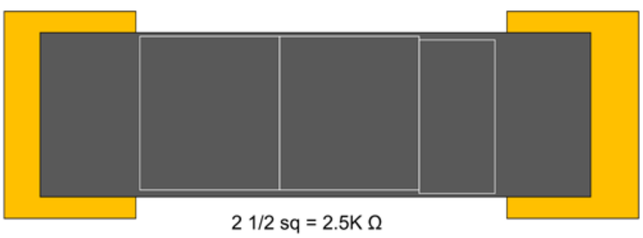


Figure 2: Basic "bar" thick-film resistor element design.

Basic do's for embedding resistor elements:

- Select resistor values that can be developed using the same basic value paste or film material.
- Maintain separation between elements to enable testing and, when required, laser trimming before lamination.
- Locate all the embedded resistor elements onto a single subsurface layer of the multilayer printed circuit board.
- Select material that will match the primary value range and tolerance requirement of the embedded resistor elements.

Don't consider the following:

- Embedding resistors with limited tolerance and that may be subject to value adjustment.
- Distributing resistor elements onto multiple layers of the multilayer circuit board.
- Attempting to provide excessively wide resistor value variations.
- Embedding resistors that may require post-lamination process access for trimming.

Most software developers are currently furnishing software tools to automatically calculate the embedded resistor elements' geometry within the multilayer circuit board. Material suppliers recommend using Mentor, Allegro, Intergraph, and PAD Power PCB with an Excel program to aid in developing the more complex resistor element geometries. While several of the discrete resistor elements will remain on the outer surface of the finished circuit board, the embedded resistors will require a unique reference designator to avoid material procurement errors. For example, a surface-mounted resistor will be defined as "R110" while the embedded "formed" resistor will be designated "ER110" on the schematic diagram and material list to avoid duplication.

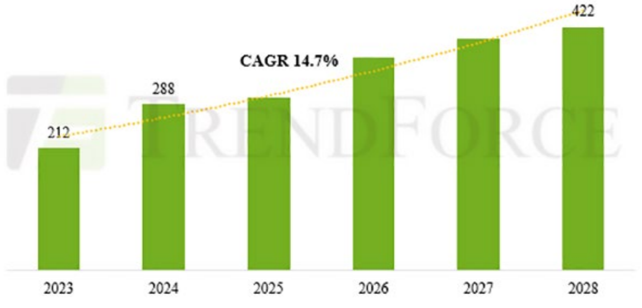
Regarding tolerance control, the physical stresses experienced during PCB lamination can affect target values. When the specified values of the resistor elements require more precise tolerance, 1% or 2% range for example, or are subject to further adjustment (tweaking), I strongly advise circuit board designers that all high-precision resistors (<5%) be retained as discrete surface mount components for placement onto the circuit board's outer surface(s).

Note: To prepare for implementing embedded resistor technology, the designer and/or program manager must first seek an experienced supplier company that can furnish practical guidance in selecting a process that will meet both technical and budgetary (cost) goals established for the end product. Many established circuit board fabricators know the materials and processes for embedding resistor elements, but not all are prepared to alter procedures established for their more conventional multilayer circuit board customer base. For additional guidance in embedding discrete passive and active die elements within the multilayer circuit board, refer to IPC-7092, *Design and Assembly Process Implementation for Embedded Components.* **DESIGN007**

Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns, click here.

Benefited from Enhancing Bio-Sensing Technology, Wearable Device Applications Market to Reach $422M

In a pivotal ruling, the U.S. Court of Appeals for the Federal Circuit has decided against Apple in its patent dispute with Masimo, mandating a halt in sales of the Series 9 and Ultra 2 in the US due to their blood oxygen features. This decision pushes Apple to potentially remove these features via software updates temporarily. Despite this setback, TrendForce maintains a positive outlook on bio-sensing tech in the wearables market. Substantial growth is predicted, with the market value for bio-sensing in smartwatches and smart bands expected to reach US$422 million by 2028, growing a CAGR of 14.7% from 2023.



Market leaders in wearable devices, such as Apple, Samsung, and Google Fitbit, are actively advancing the bio-sensing sector. TrendForce's 2024 forecast suggests a focus by Apple and Samsung on improving the precision of bio-sensing features in upcoming smartwatches. They plan to employ photoplethysmograph (PPG) technology for enhanced monitoring of heart rate and blood oxygen levels, furthering capabilities in personal health management.

TrendForce emphasizes two primary strategies among wearable device brands: Expanding bio-sensor features and enhancing their accuracy. This dual approach not only differentiates products but also boosts customer engagement and market growth. Bio-sensing, especially when merged with health management, shows promise for integration into medical, insurance, and automotive systems. As a result, securing comprehensive patents for both the software and hardware aspects of bio-sensing technology has become a critical focus for these companies.

(Source: TrendForce)

Unleashing the Power of Embedded Components

Feature Article by Stephen V. Chavez
SIEMENS ELECTRONIC DESIGN AUTOMATION

Printed circuit boards (PCBs) are the backbone of electronic devices, facilitating the seamless flow of electrical signals and supporting the functionality of various components. In recent years, the evolution of PCB design has witnessed a significant transformation with the integration of embedded components. This innovative approach not only enhances the overall performance of electronic devices, it brings forth a range of advantages regarding space efficiency, reliability, and manufacturing processes.

Embedded components refer to electronic elements that are directly integrated into the PCB itself rather than being mounted on the surface. Traditional PCB designs involve placing components on the surface, but the embedded approach goes a step further by incorporating elements like resistors, capacitors, and even active components within the layers of the PCB. This integration eliminates the need for additional space on the surface, and provides a compact solution for modern electronic devices.

Unlike a standard PCB design, embedding components add complexity to PCB layout, requiring careful planning to maintain signal integrity as they may affect signal paths, thus requiring analysis and mitigation to preserve electrical performance. This complexity increases due to the component synthesis required to create embedded passive geome-

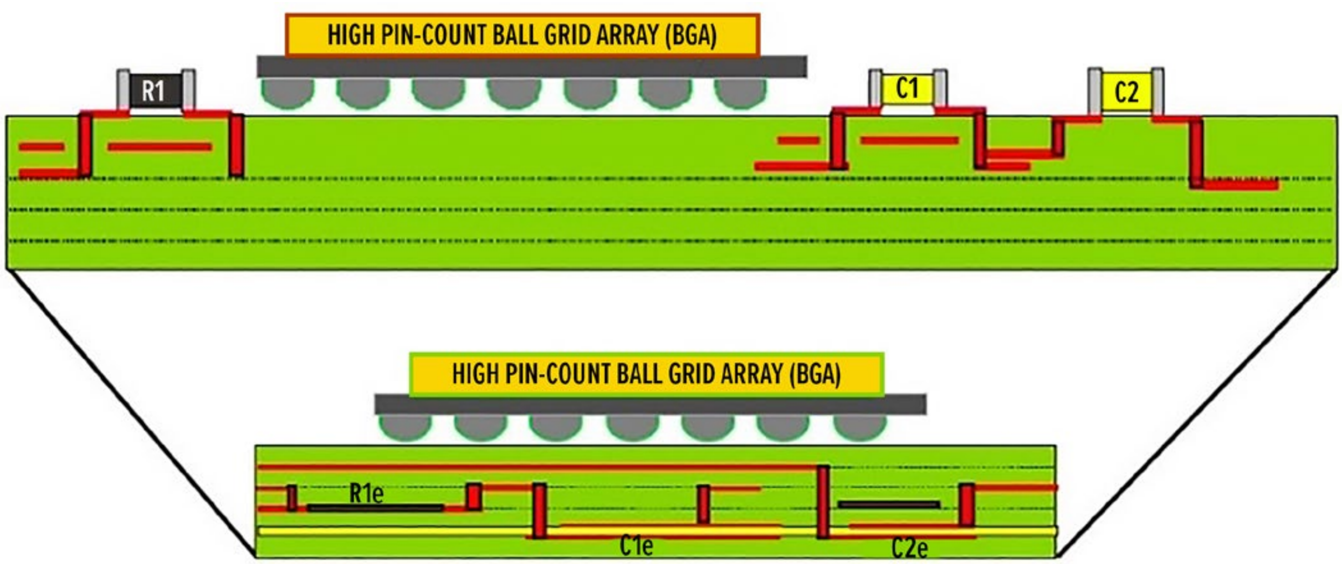


Figure 1: Embedded passive components reduce size and space.

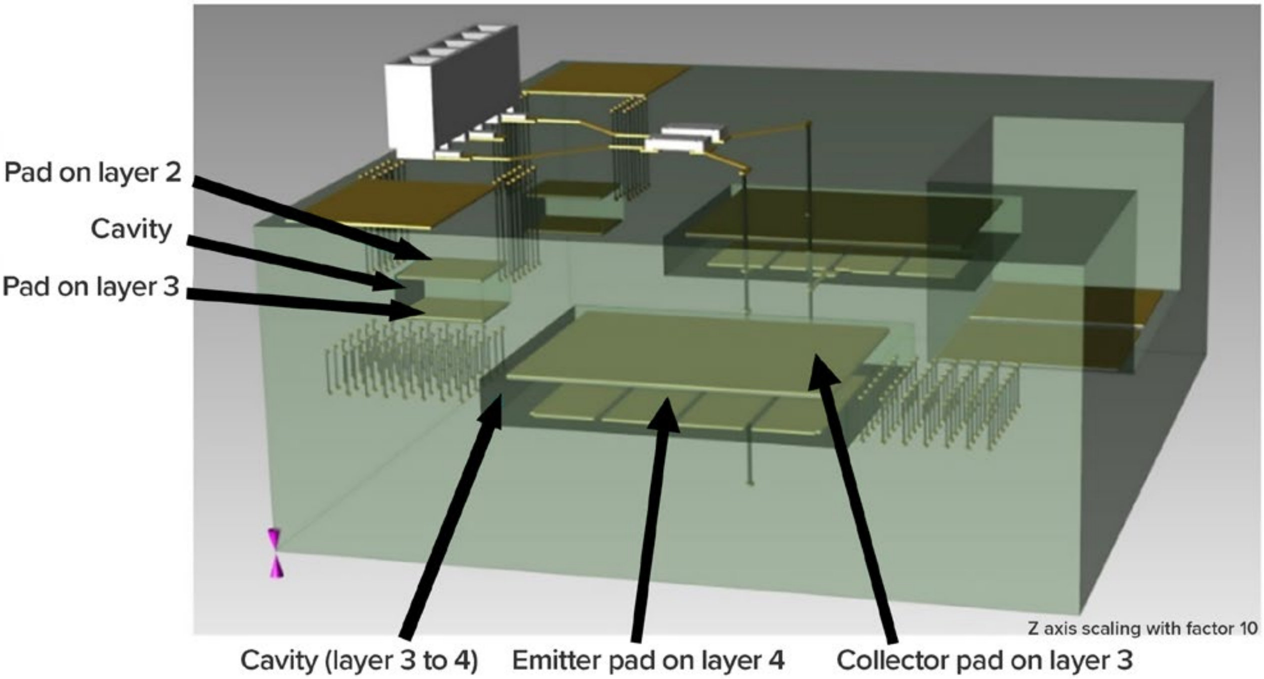


Figure 2: A 3D view of embedded components.

tries, the placement of components on internal layers, and the routing to them.

The reliability of PCBs with embedded components, compared to traditional boards, is a nuanced consideration that depends on various factors. While embedded components offer many advantages in terms of reduced external exposure and enhanced thermal performance, their integration comes with a set of challenges and considerations. Designers need to carefully assess additional factors as they must balance advantages and challenges.

Advantages of Embedding Components

- **Space efficiency:** Integration within PCB layers significantly reduces the overall footprint, which is crucial for compact and portable devices
- **Improved signal integrity:** Shorter signal paths minimize signal degradation, interference, and electromagnetic emissions, especially in high-frequency applications
- **Reliability and durability:** Shielded within the PCB layers, embedded components are less susceptible to external factors and enhance device reliability
- **Enhanced thermal performance:** Proximity to PCB layers allows efficient heat dissipation—especially critical for applications with heat concerns—preventing overheating and potential damage
- **Shorter signal paths:** Improved signal integrity enhances reliability and is crucial in high-frequency applications
- **Manufacturing simplification:** Fewer external components streamline the assembly process, reducing errors, enhancing manufacturing efficiency, and contributing to cost savings

Embedded Component Challenges

- **Accessibility and repairability:** Embedded components pose challenges for test and repairs due to limited accessibility, impacting reliability
- **Material selection:** Careful selection of materials is crucial for longevity and reliability, taking insulation, thermal conductivity, compatibility, and long-term stability into consideration, as these are vital for preventing issues like delamination, warping, or thermal expansion, thus preserving reliability

- **Manufacturability and cost:** Specialized equipment for embedding components can increase manufacturing costs. Shapes and voids may pose manufacturing challenges, which must be considered in fabrication, assembly, and inspection. Complex manufacturing processes can lead to reliability issues if not executed precisely.

As with any design decision, implementing embedded components in PCB designs involves cost tradeoffs. Knowing when to start embedding components and determining the price/technology cutoff requires careful consideration of various factors. The following are the key considerations for making informed decisions.

- **Application requirements:** Evaluate whether the application demands a compact form factor, improved signal integrity, and/or enhanced thermal performance
- **Production volume:** Consider the impact on cost tradeoffs based on production volume, with high-volume production making embedded components more economically viable
- **Component complexity and size:** Assess the cost-effectiveness of embedding simple passive components versus surface mount (SMD) components and consider the size of components
- **Manufacturing capabilities:** Ensure the chosen PCB manufacturer has the expertise and equipment for embedding components. Passive components require an additional material layer that's either subtractively etched or additively printed. Active components are often in bare die form, and inserted mid-stream in the fabrication process.
- **Material costs:** Carefully evaluate material costs and determine whether performance benefits justify additional expenses
- **Design iterations and prototyping:** Account for prototyping expenses during initial stages of implementation
- **Technological maturity:** Consider the maturity of embedded component technology and assess the current state for potential advancements or cost reductions
- **Return on investment:** Evaluate overall ROI to justify higher up-front costs with long-term gains

While embedded component design poses challenges for some designers, modern EDA tools are generally equipped to handle this aspect of PCB design relatively easily. How this is addressed varies from tool to tool regarding features for defining shape, size, and placement as well as capabilities for simulation and analysis. Simulation and analysis must assess electrical and thermal performance considering the presence of embedded components. Utilizing 3D modeling allows visualization of the PCB layout in three dimensions, aiding in identifying interference and manufacturing issues related

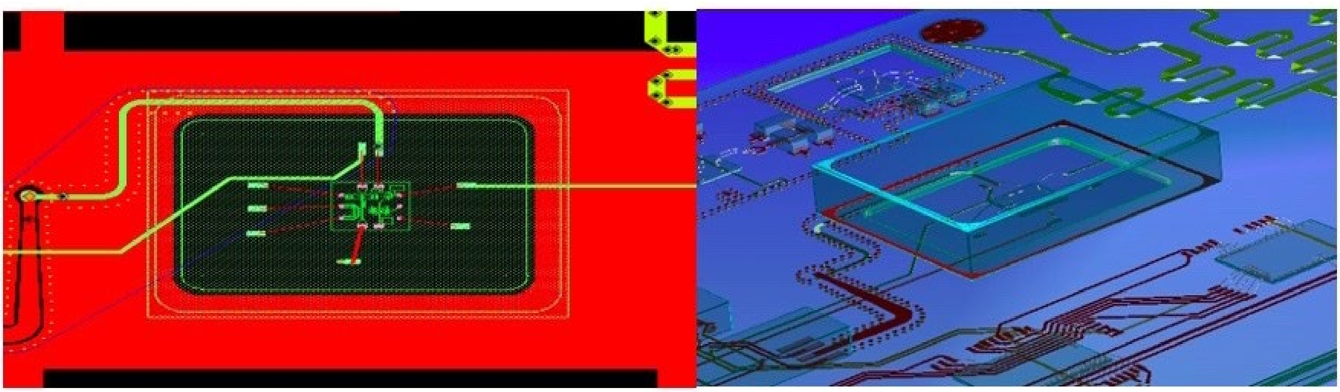


Figure 3: Example of intelligent cavity design object during layout.

to embedded components. Design rule checks (DRC) ensure compliance with manufacturing constraints and design guidelines, including rules specific to embedded component design. With today's EDA tool features and capabilities varying from one another, multidomain tool integration and collaboration are the best practices, as collaborative features facilitate effective interdisciplinary communication between stakeholders.

> **It is highly recommended to consult your PCB fabricator at the earliest stages of the PCB design process...**

By adopting best practices and leveraging simulation and analysis features, designers can integrate embedded components into PCB designs with confidence, optimizing both electrical and mechanical aspects of the final product. It is highly recommended to consult your PCB fabricator at the earliest stages of the PCB design process—even more so when implementing embedded components in your PCB design to increase the potential for high reliability.

Best Practices for Designing With Embedded Components

1. **Early planning:** Incorporate cavity design considerations early in the design process.
2. **Collaboration:** Foster collaboration between different teams involved in the design process.
3. **Simulation and prototyping:** Leverage simulation tools and prototypes to assess and validate the design.
4. **Comprehensive design reviews:** Conduct thorough design reviews to identify and address potential issues.

The reliability of PCBs with embedded components depends on careful consideration of design choices, material selection, manufacturing processes, and the specific requirements of the application. While embedded components can provide advantages in terms of reduced external exposure, enhanced thermal performance, and improved signal integrity, challenges related to accessibility for testing and repairs, material compatibility, manufacturing complexities, and cost-driven decisions should be addressed to ensure long-term reliability. Designers should conduct thorough testing and validation processes to assess and guarantee the reliability of embedded component designs in their specific applications.

Embedded components offer a transformative approach to PCB design, providing space efficiency, reliability, and performance. Despite the challenges, advances in materials and manufacturing processes make them a compelling choice for the next generation of electronic devices. Implementing embedded components involves balancing benefits and costs and understanding application requirements, production volume, component complexity, manufacturing capabilities, material costs, design iterations, technological maturity, and ROI. To get accurate cost estimates for implementing embedded components in a specific PCB design, it is highly recommended to consult with PCB manufacturers or assembly service providers. They can provide detailed quotes based on the project requirements and specifications. **DESIGN007**

Stephen V. Chavez, CID+, is principal technical product marketing manager with Siemens Electronic Design Automation and a master PCB design instructor.

Electronics Industry Mourns Loss of Colleague and Visionary Michael Ford

Sadly, longtime I-Connect007 columnist, industry visionary, and friend Michael Ford passed away Saturday, Jan. 27, 2024. “In this time of sorrow, we can take solace in the knowledge that Michael leaves a great legacy of contribution to the electronics industry,” according to a statement from Aegis Software.

Michael was senior director of emerging industry strategy at Aegis. He was a prolific writer and speaker whose work and ideas put him at the forefront of electronics manufacturing. Working for Aegis gave him the opportunity to apply his software for electronics manufacturing experience to further drive technology solution innovation.

In the statement from Aegis, Michael was described as “always envisioning what was needed to achieve an improved manufacturing future before others could see it. What new system, standard, or concept could help move things forward for the better? Michael could move those ideas to the forefront and was always seeking the views and ideas of others in the process. He had a singular gift in helping everyone he encountered see the future with him in his articulate and compelling way that brought everyone into the process, whether an individual or a full conference hall.”

He started his career with Sony, including eight years working in Japan. He was instrumental in creating and evolving software solutions for assembly manufacturing that meet the most demanding expectations. He was an established thought leader for Industry 4.0 and digital Smart factories, and an active contributor to industry standards.

In 2020, Michael was given the IPC President’s Award as recognition for contributions, including CFX, traceability, secure supply-chain and digital twin standards.

In 2021 Michael was awarded the Dieter Bergman IPC Fellowship Award and chose Villanova University’s engineering department as the recipient of the grant which in turn awards a scholarship to benefit the promotion of opportunities for women in the industry.

His column for I-Connect007 was titled Smart Factory Insights, and he frequently took commonly-held ideas and pushed the boundaries of current thinking. He often found ways to improve business operations or create new business models that built off current frameworks.

“Michael has been such a generous and knowledgeable columnist for so long,” says Pete Starkey, a technical editor for I-Connect007. “He was a genuinely lovely man and a worthy recipient of our ‘Good for the Industry’ award. I can’t believe he’s gone.”

One time we asked him for his sage advice, and he said, “Always keep an open and progressive mind. Listen to and understand perspectives from all of those around you.”

MilAero007 Highlights

RTX Raytheon's GhostEye MR Proves Operational Readiness During U.S. Air Force Exercise ▸

GhostEye MR was designed and developed by Raytheon, primarily through internal research and development investments. During the recent exercise, GhostEye MR was successfully integrated with NASAMS' Air Defense Console and the Battlespace Command and Control Center (BC3), a command-and-control element used by the U.S. Air Force.

Global Deep-Space Advanced Radar Capability Extends AUKUS Partnership ▸

Northrop Grumman Corporation is developing the Deep Space Advanced Radar Capability (DARC) that will track objects in the geosynchronous orbit, protecting critical U.S. and allied satellites. DARC is a global network of three advanced ground-based sensors to be operated in collaboration with AUKUS alliance partners, the United States, Australia, and the United Kingdom.

Airbus Helicopters to Expand Unmanned Aerial System Portfolio with Acquisition of Aerovel ▸

Airbus Helicopters and Aerovel have signed an agreement regarding the acquisition of Aerovel and its unmanned aerial system (UAS), Flexrotor, as part of a strategy to strengthen its portfolio of tactical unmanned solutions. Flexrotor is a small tactical unmanned aerial system designed for intelligence, surveillance, target acquisition and reconnaissance (ISTAR) missions at sea and over land.

Leidos Deploys New Flight Service Voice Communications System ▸

Leidos has announced the successful deployment of a new Flight Service Voice Communications System (FSVCS) using Voice over Internet Protocol (VoIP) technology, developed in coordination with Rohde & Schwarz USA. The flexible and scalable system includes interfacing with legacy analog connections and new digital voice communication. The design minimizes dependency on traditional point-to-point communications and increases voice availability with the general aviation community.

Lockheed Martin Awarded Contract for 18 Space Development Agency Tranche 2 Satellites ▸

The Space Development Agency (SDA) has awarded Lockheed Martin a contract to build 18 space vehicles as part of its Tranche 2 Tracking Layer constellation. Lockheed Martin will provide 16 wide field of view missile warning/missile tracking space vehicles with infrared sensors and two space vehicles with missile defense infrared sensors that can generate fire control-quality tracks to provide preliminary missile defense mission capabilities.

DARPA Moves Forward on X-65 Technology Demonstrator ▸

DARPA has selected Aurora Flight Sciences to build a full-scale X-plane to demonstrate the viability of using active flow control (AFC) actuators for primary flight control. The award is Phase 3 of the Control of Revolutionary Aircraft with Novel Effectors (CRANE) program.

DESIGN TIPS #124:

ETCH COMPENSATION

What is minimum space and trace? The answer depends on the starting copper weight.

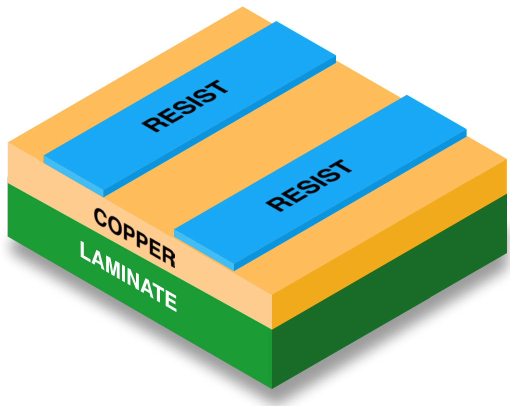
This is because we must do an etch comp on the traces in CAM to compensate for known etch loss. The space between traces after compensation will play a role in whether a board can be manufactured.

The lower the spacing width, the higher the cost. Designers don't always account for the proper starting copper weight after edge compensation.

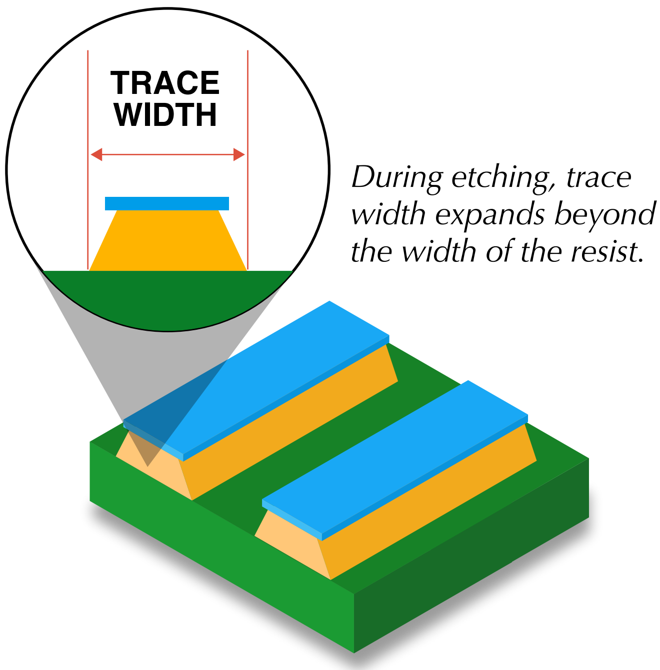
Design tips:

- For accurate starting copper weight, **add a half mil (.0005″) to all copper features**.
- **Start with 3/8 or 1/4 oz. foil**, reducing etch comp and less likely to cause a spacing issue.
- **Boards that call for full body electrolytic gold are not comped** to avoid gold slivers occurring during the etching process.

Before etching



After etching



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Reassessing Surface Finish Performance for Next Generation Technology, Part 2

Article by Frank Xu, PhD, Martin Bunce, and John Coonrod

The introduction of 5G/6G has created a growing demand for faster rates of data transfer and operation at higher frequencies, pushing signals to travel toward the outer edges of conductors. As a result, the surface finish applied over the copper circuitry is now gaining more attention.

It has previously been shown that the low conductivity and magnetic properties of the electroless nickel (EN) layer negatively affect electrical signals as they travel along the conductor's outer surfaces, leading to insertion losses. Subsequent studies show that reducing the EN thickness can offset some insertion losses observed. In more recent times, nickel-free finishes, such as EPIG (electroless palladium, immersion gold, no EN), thin EN ENEPIG, silver-gold (immersion silver followed by immersion gold), have been promoted as solutions for improving signal integrity at higher frequencies.

In Part 1 of this article[1], we reported the signal loss properties of the new nickel-free surface finishes, along with immersion silver, organic solderability preservative (OSP), and ENIG/ENEPIG surface finishes. As expected, ENIG and ENEPIG are challenged by signal losses at higher frequency, with OSP and immersion silver demonstrating no contribution to the signal losses. The new generation surface finishes (silver-gold, thin EN ENEPIG, and EPIG) perform similarly—outperforming


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standard ENIG/ENEPIG finishes but still contributing slight signal loss compared to immersion silver and OSP.

One of the concerns for nickel-free finishes is the solder joint reliability with removed or greatly reduced nickel diffusion barrier layer thickness. This article will address this concern and focus on various solder joint reliability testing, including high-speed ball shear, drop shock, and solder joint reliability electromigration tests.

Work Program

As mentioned in Part 1, the test candidate surface finishes selected are:

- Standard ENEPIG (4 µm electroless nickel/0.1 µm palladium/0.05 µm gold)
- Standard ENIG (4 µm electroless nickel/0.05 µm gold)
- Thin EN ENEPIG (0.2 µm electroless nickel/0.1 µm palladium/0.05 µm gold)
- Ultra-Thin EN ENEPIG (0.1 µm electroless nickel/0.1 µm palladium/ 0.05 µm gold)
- EPIG (0.1 µm palladium/0.05 µm gold)
- Silver-Gold (0.15 µm silver/0.05 µm gold)
- Immersion Silver (0.3 µm)
- OSP (0.4 µm)

As mentioned in the introduction, the following tests were performed:

- High-speed ball shear
- Drop shock evaluation
- Solder joint electromigration

After the data was collected, it was summarized, and a decision matrix was constructed to allow designers to compare performance requirements against each surface finish's capabilities.

Experimental Methodology

High-Speed Ball Shear Test

Ball shear tests were performed to evaluate the solder joint reliability. Testing was done on ball grid array (BGA) test coupons with solder mask defined pads with solder resist openings at 250 µm. The ball shear test at low-speed shear conditions (0.3–0.5 mm sec) were reported in Part 1[2]. In this article, only high-speed ball shear data is presented. It was tested at 1000 mm/sec and the spacing between the shear head and board surface was 20 µm.

Drop Shock Test

The dummy CTBGA84 components were used for the drop shock test. The drop shock table height and striking surface were adjusted to obtain a half-sine shock pulse with 1500 Gs and 0.5 msec peak, following the JESD22-B111 standard. Failures were defined as a drop of 1V or more in the applied potential for at least 0.5 msec, based on the IPC/JEDEC-9706 standard, being detected and recorded using a high-speed data acquisition system. The interval plot of the drop shock performance are presented.

Solder Joint Electromigration Test

Solder joint electromigration is a phenomenon that can occur in electronic devices where electrical current flowing through solder joints causes metal atoms to migrate, leading to the degradation or failure of the joint[3]. Electromigration is influenced by several factors, including the magnitude and direction of the current, the temperature, the composition of the solder alloy, as well as the microstructure of the joint. Higher current densities, higher temperatures, and the presence of defects or impurities in the solder can accelerate electromigration. To study the effects of the various surface finishes on electromigration, the current and temperature were fixed at 5A and 100°C. SAC 305 solder alloys were used for the test.

Results and Discussion

High-speed Ball Shear Test

The high-speed ball shear test was done at 1000 mm/sec using the DAGE 4000HS instrument. The ball grid array (BGA) with 250 µm solder resist open (SRO) was used as the testing substrate. A 250 mm SAC 305 solder ball and ALPHA WS-608 paste flux were used to form the solder bumps. Each test condition was repeated twenty times to ensure good statistical significance. Figure 1 shows the interval plot of high-speed ball shear strength of various surface finishes. It can be seen that the standard EPIG finish has the lowest ball shear strength. It is also interesting to note that silver-gold, immersion silver and OSP showed higher ball shear strength compared to other finishes, thanks to the copper-tin solder joint.

Drop Shock Performance

As pad sizes continue to shrink, the significance of the drop shock performance has increased, particularly in mobile phone applications. In Figure 2, the number of drop shocks for each finish is displayed. The first three

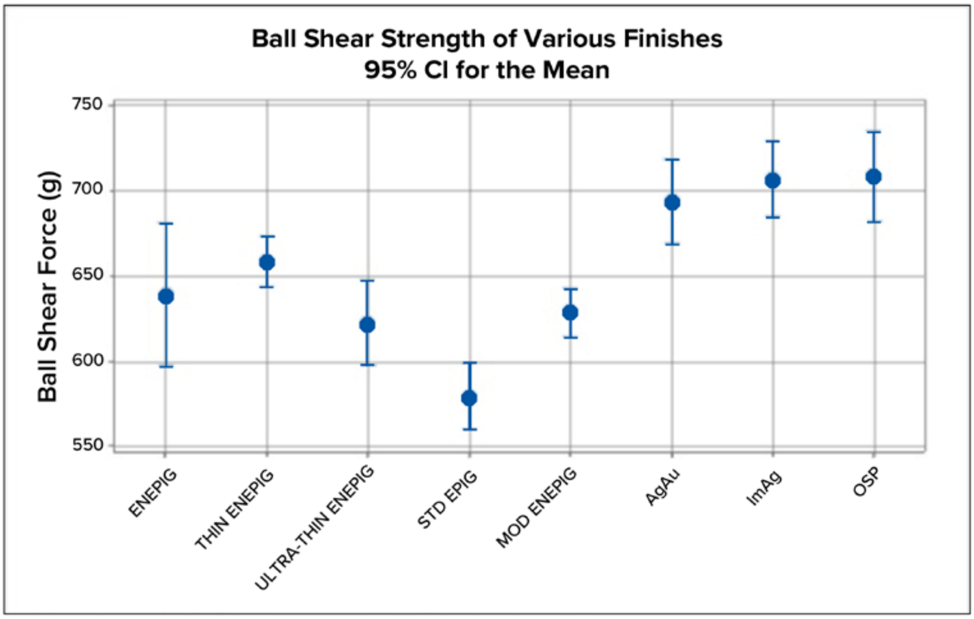


Figure 1: Interval plot of high-speed ball shear strength of various surface finishes.

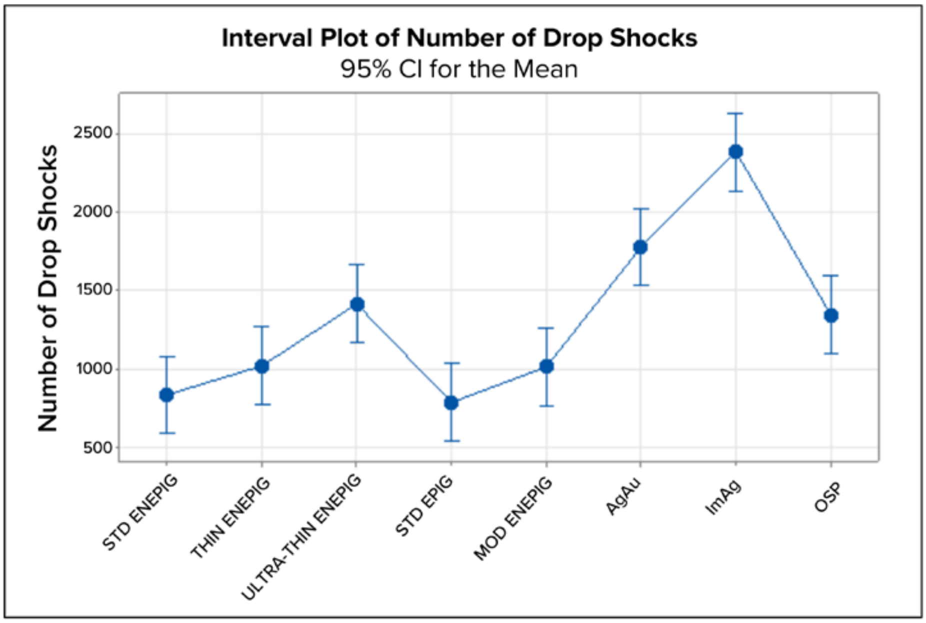


Figure 2: Interval plot of drop shock performance of various surface finishes.

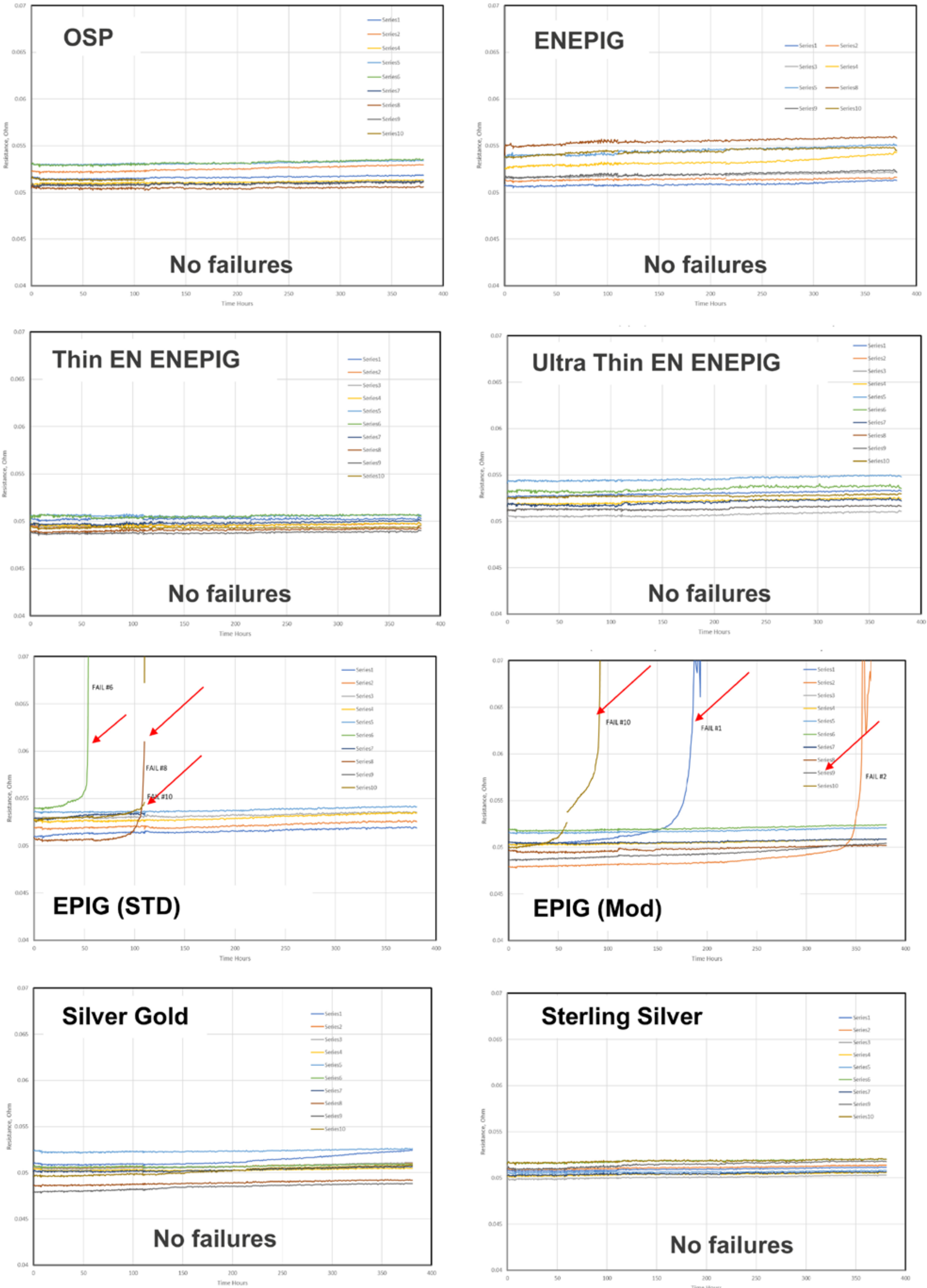


Figure 3: Resistance vs. time in electromigration test in the test vehicle plated with different surface finishes.

finishes shown are standard ENEPIG, thin nickel ENEPIG, and ultra-thin nickel ENEPIG. Interestingly, it can be observed that as the nickel interlayer thickness decreases, the drop shock performance improves, primarily because of an increasingly higher proportion of copper-tin solder joint.

Initially, it was believed that the complete elimination of nickel, as seen in EPIG or modified EPIG finishes, would further enhance the drop shock performance. However, this is not the case. The reason lies in another deposition mechanism utilized during the plating process for EPIG finishes, which results in microvoid formation[5].

Silver-gold, immersion silver, and OSP finishes all provide robust drop shock performance, which is linked to the preferred copper-tin solder joint formation in those finishes, compared to more brittle nickel-tin solder joint in nickel-containing finishes.

Solder Joint Electromigration Test

As described in the experimental methodology section, the solder joint electromigration tests were done at constant current (5A) and temperature (100°C). The resistance was monitored throughout the testing period (400 hours). If there was a 20% increase over initial resistance, it was considered a failure.

Figure 3 presents the electromigration results for the solder joints of all the surface finishes tested, displaying the resistance plotted against the testing time for up to 400 hours. With the exception of standard EPIG and modified EPIG, consistent resistance is observed throughout the entire test duration for all surface finishes. However, both standard EPIG and modified EPIG exhibit a sharp increase in resistance after approximately 50 to 100 hours of testing, indicating that the solder joints have been compromised during the high current/high temperature test.

X-ray imaging was employed to examine the alterations in solder joints before and after the electromigration test, indicated by the red arrow in Figure 4a. As the X-ray images clearly display, it is evident that the solder joints in standard EPIG have collapsed following the test.

To conduct a detailed examination of the solder joints, a cross-section sample was made based on the X-ray imaging results. Figure 4b displays a scanning electron microscope (SEM) image of a standard EPIG solder joint (cathodic side) after undergoing the electromigration test. The inset provides an overview of the cross-section. The red circles indicate voids that appear in the solder joint when subjected to high current density, leading to collisions between electrons and metal atoms. These collisions cause the metal atoms to move in the direction of electron flow. Over the course of the electromigration testing, this movement of metal atoms

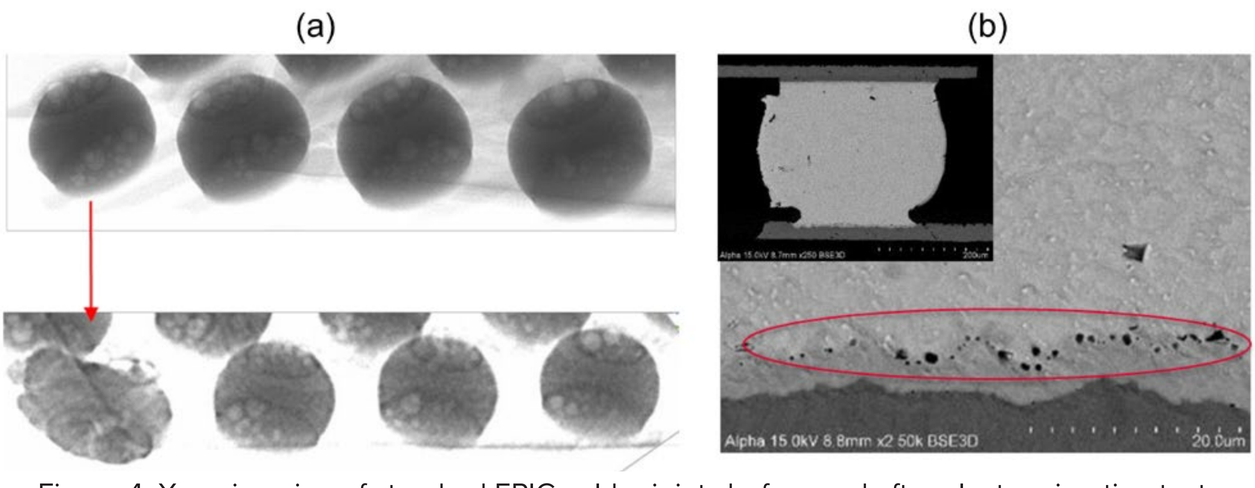
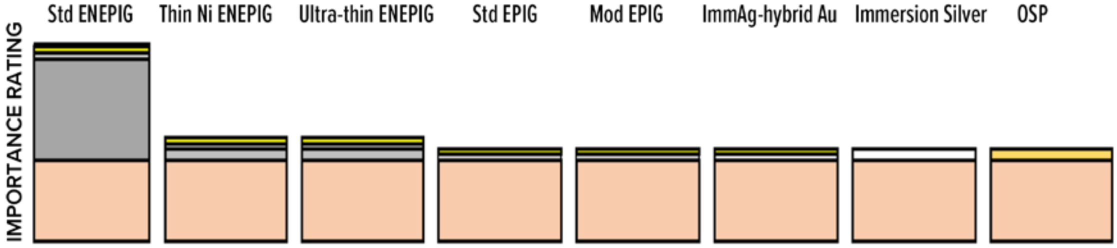


Figure 4: X-ray imaging of standard EPIG solder joints before and after electromigration test.

Correlation Key	
Strong Correlation	9
Medium Correlation	3
Weak Correlation	1
No Correlation	0



Performance Criteria	Importance Rating	Std ENEPIG	Thin Ni ENEPIG	Ultra-thin ENEPIG	Std EPIG	Mod EPIG	ImmAg-hybrid Au	Immersion Silver	OSP
Micro-strip Insertion Loss	9	1	3	3	3	3	3	9	9
Drop Shock	9	1	3	3	1	3	9	9	9
Low-speed Ball Shear (0.25 mm)	9	9	9	9	9	9	9	9	9
High-speed Ball Shear (0.25 mm)	9	9	9	9	1	1	9	9	9
Wirebond Capability	9	9	9	9	9	9	9	1	0
Solderspread	9	9	9	9	9	9	3	9	3
Electromigration-SJ Reliability	9	9	9	9	1	3	9	9	9
Mixed Flowing Gas	9	3	3	9	9	9	3	1	3
Final Finish Score		50	54	60	42	46	54	56	51
Final Finish Relative Score		450	486	540	315	414	486	504	459
Final Finish Ranking		6	3	1	8	7	3	2	5

Figure 5: Quality function deployment (QFD) matrix of various surface finishes.

results in the formation of voids, primarily on the cathodic side of the solder joint.

Conclusions

As the nickel-free finishes exhibit similar high-frequency signal loss properties, it becomes important to evaluate other characteristics of these finishes. In this article, high-speed ball shear, drop shock performance and solder joint electromigration tests have been thoroughly undertaken for standard ENEPIG, thinner EN ENEPIG's, standard and modified EPIG (no EN) as well as immersion silver, OSP, and a new silver-gold surface finish.

All surface finishes were compared across the performance requirement matrix and a quality function deployment (Figure 5) was constructed to produce a data-driven tool to align surface finish performance against design needs. As it shows, there is no one perfect surface finish that fits every application. Fabricators would pick the performance criteria with corresponding importance rating and evaluate the surface finishes according to their specific needs. **DESIGN007**

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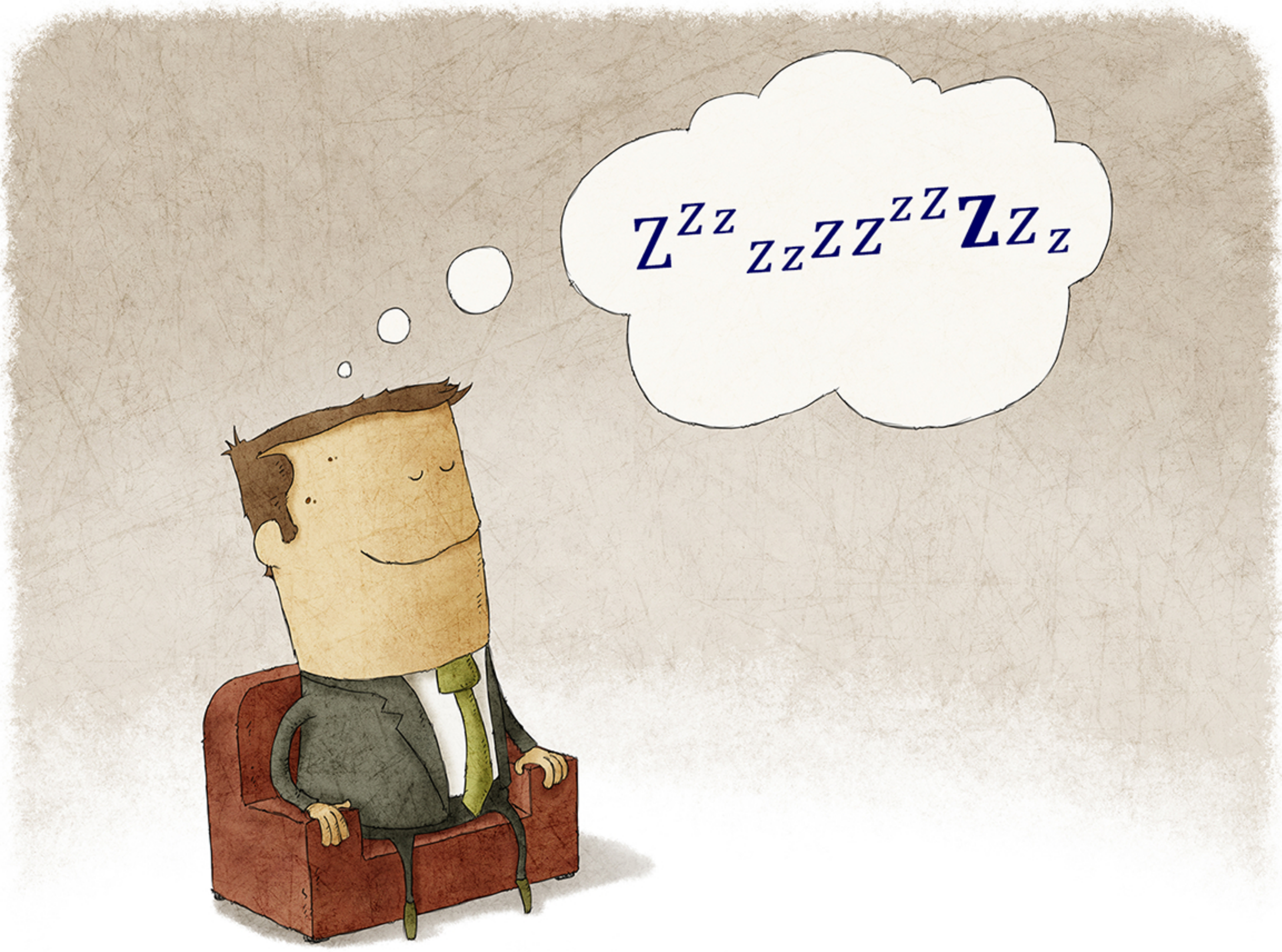
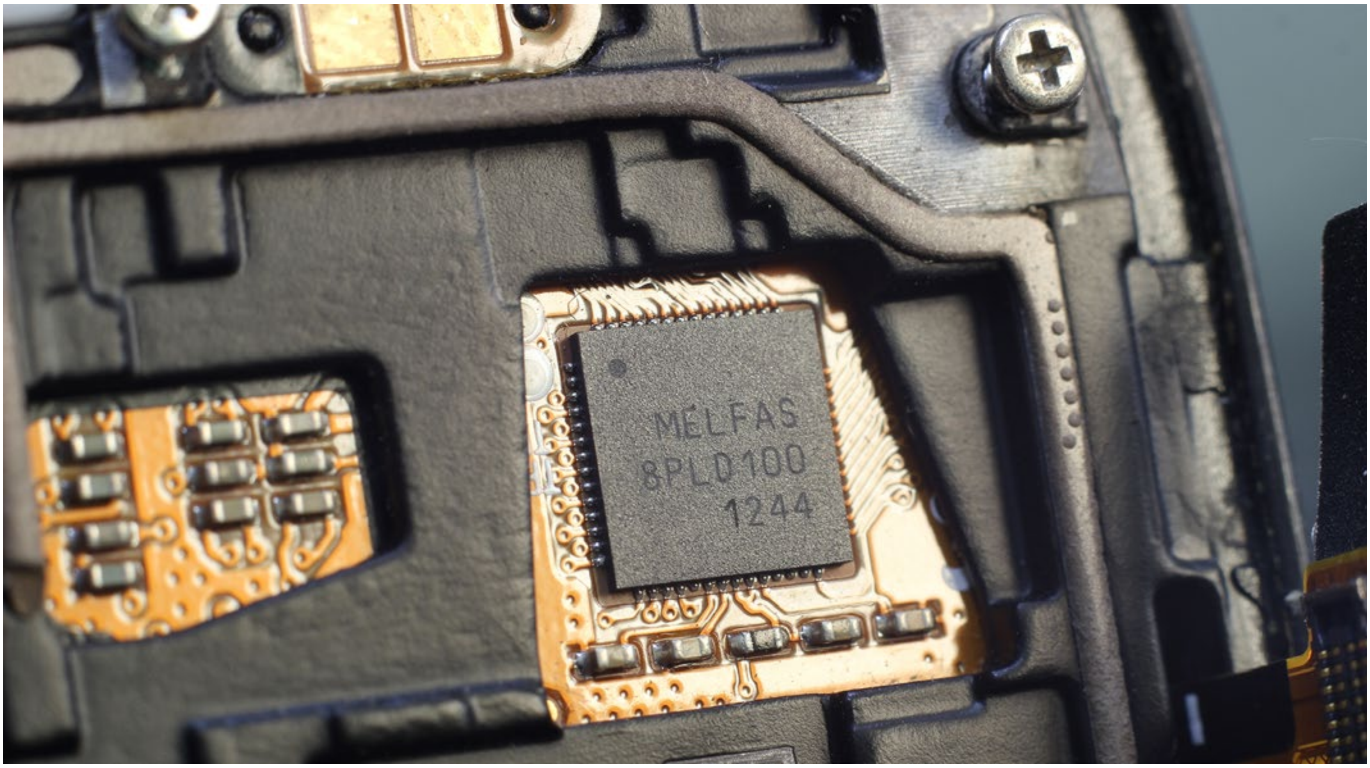
John Coonrod is technical marketing manager for Rogers Corporation.





Embedded Capacitors for PCBs, Chips, and Packages

Feature Article by Cody Stetzel
CADENCE DESIGN SYSTEMS

Decoupling capacitors are the first place for systems designers to start building digital systems with sufficient power integrity. While decoupling/bypass capacitors are still a standard strategy for ensuring power integrity in single digital ASICs, the entire system power bus also needs to be approached throughout broader frequency ranges. The approach combines power integrity design at low frequencies, where discrete caps dominate, and up to GHz frequencies where discrete caps have trouble providing the required capacitance.

Package designers and chip designers assist the PCB layout engineer by including embedded capacitors on-chip and in-package to address the entire range of frequencies where decoupling is needed. As more electronics companies take a leading role in chip and package design, there is a need to determine the appropriate amount of capacitance needed to ensure low PDN impedance throughout broad frequency ranges. This article will look at the different types of capacitors that can be used as embedded components in PCBs and in chips/packages.

The various types of embedded capacitors that can be used in PCBs, on a semiconductor die, and in-package are summarized in Figure 1. There is some overlap among these options for system

	PCB	Package	Die
Discrete embedded capacitors	X	X	
Embedded capacitance material	X	X	
Embedded dielectric foils		X	X
Embedded ceramics		X	
Trench capacitors		X	X

Figure 1: A range of available embedded capacitors and their applications.

designers, and each targets different frequency ranges in PCBs, die, and packages.

Discrete Embedded Capacitors

Discrete capacitors are often placed on packages for some advanced processors. In addition to direct placement and assembly in a processor package, these components can be embedded in a PCB or package substrate.

It is possible to embed small capacitors in an organic substrate, including the organic materials used to build PCB stackups and package substrates. Discrete capacitors placed in PCBs and substrates are off-the-shelf components, designated low-profile MLCCs. While not specifically designed for embedding in substrates or PCBs, they can be embedded in these materials thanks to their lower-than-normal profile.

The target frequency range is 100 MHz to 1 GHz, or higher for specialty RF capacitors.

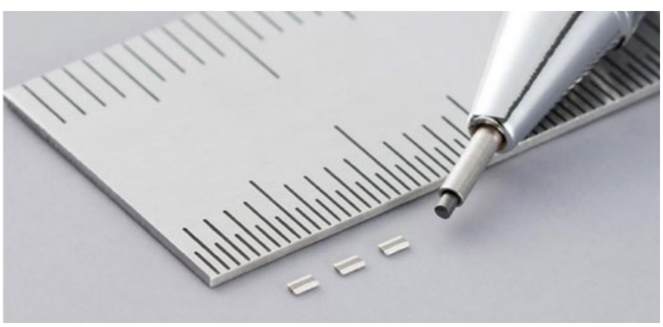


Figure 2: These low-profile Murata MLCCs can be embedded.

Embedded Capacitance Material (ECM)

This class of organic materials offers high capacitance density through the material's high dielectric constant. Noise/power fluctuations are damped at high frequencies because these materials are very lossy, having high loss tangents (~0.02 or higher) at lower frequencies than in PCBs/packaging materials. They are very thin materials (~1-mil thickness) but they can be used in standard lamination and buildup processes with other materials for packaging and PCB stackups.

These materials are probably the simplest class of materials for providing low PDN impedance and damping power fluctuations simultaneously. They can also help lower the overall PDN impedance curve over a broad frequency range.

The target frequency range for embedded capacitance materials is ~1 MHz to 1 GHz.

Embedded Dielectric Foils and Ceramics

Other embedded capacitor materials are inorganic, and thus they cannot be used in a standard lamination process with other organic materials in PCBs and substrates. However, these can be used in two areas:

- Capacitor dielectrics (non-ceramic) used in inorganic packaging and on-die

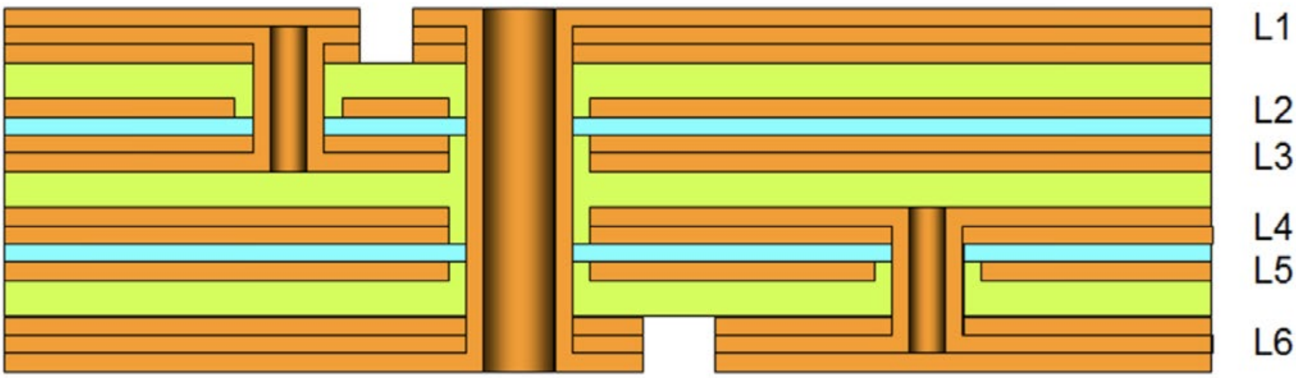


Figure 3: This 6-layer PCB stackup can use an ECM between L2 and L3, or between L4 and L5, to form a large embedded capacitor. A similar strategy could be used with packaging.

- Ceramic insulators bonded to package substrates or embedded in interposers

Embedded dielectric foils like tantalum can be used on-die as a sintered layer. This enables a thin layer over a large area, giving a low-profile embedded capacitor film integrated into a semiconductor die.

Following the same approach as embedded dielectric foils, ceramics can also be used in substrates and interposers as an embedded capacitive film when a standard organic ECM is not suitable. While ECMs target both PCBs and packaging, embedded ceramics currently sit in the packaging domain and are compatible with multiple substrate/interposer materials. An example is shown in Figure 4. These ceramic films are placed as a thin metal-insulator-metal (MIM) structure. The target frequency range is up into GHz frequencies.

Trench Capacitors

These structures are fabricated directly into silicon, either in a die or in interposers. They can have unique vertical structures that attempt to maximize the exposed surface area that defines a trench capacitor, thereby maximizing the capacitance of each trench. Multiples of these trench structures act like a large group of capacitors in parallel, so they collectively provide high capacitance without decreasing the self-resonant frequency of the structure.

The target frequency range runs into the GHz frequencies.

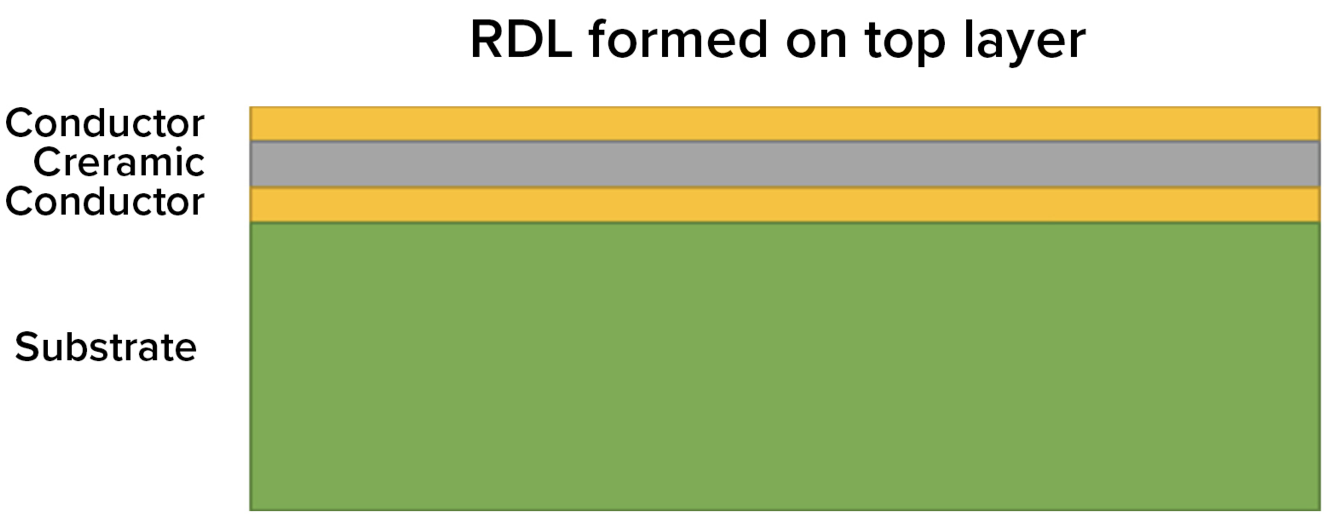


Figure 4: Embedded ceramic film structure for a package substrate/interposer.

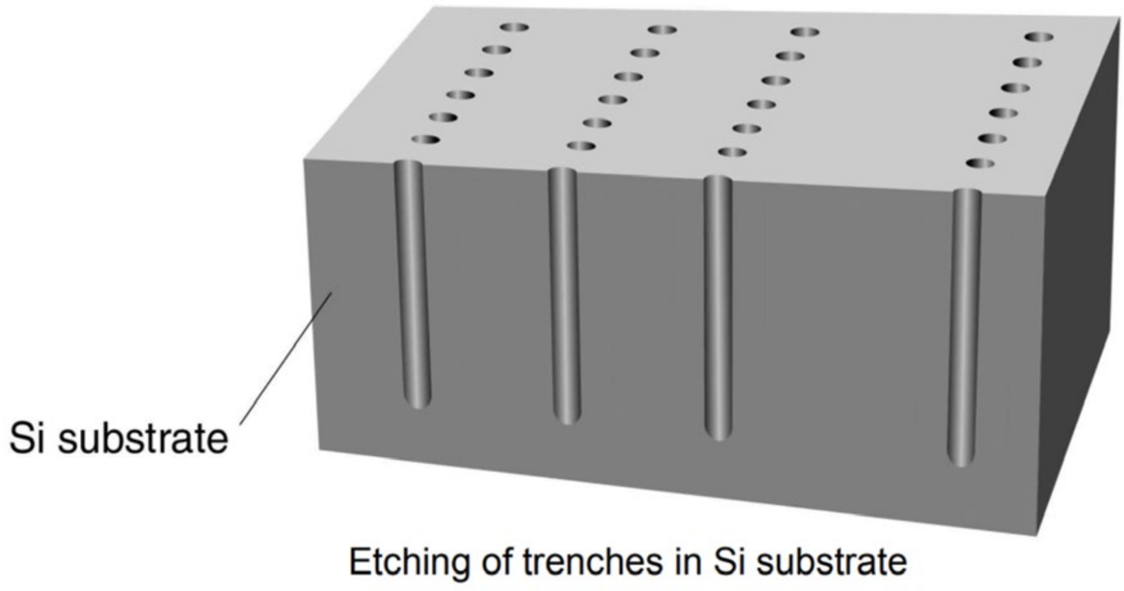


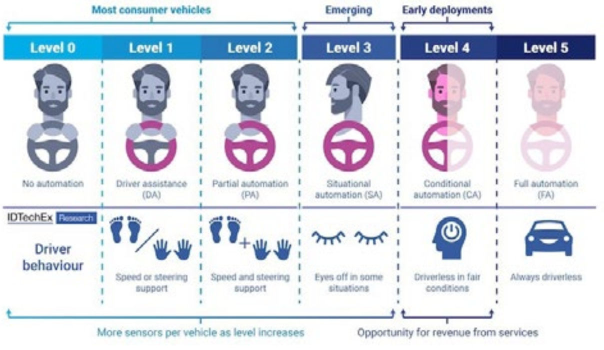
Figure 5: Silicon trench capacitors on Si substrate.

These options target decoupling into the GHz range, leaving PCB designers to focus on the lower end of the frequency range with discrete capacitor selection and PCB stackup design. By working with packaging designers, a team can produce more advanced substrates that maintain power stability up to very high frequencies. **DESIGN007**

Cody Stetzel is a technical marketing engineer at Cadence Design Systems. This article originally appeared as a blog post on the Cadence Design Systems website.

New Vehicle Tech Will Be Worth $1.6 Trillion by 2034, Says IDTechEx

Autonomous driving, electric vehicles, connected and software-defined vehicles, and in-cabin monitoring are all megatrends reshaping the automotive industry. Together, these technologies combine to form a $1.6 trillion opportunity by 2034, nearly a 10-fold increase compared to 2023. The new report from IDTechEx, "Future Automotive Technologies 2024-2034: Applications, Megatrends, Forecasts", brings together a portfolio of IDTechEx's research into a single summary of the biggest changes and opportunities coming to the automotive industry. Much of this potential market revenue will be coming from components required for electrification and automation, but the report predicts that services offered by autonomous and connected vehicles have the most room for growth.



Autonomous cars are still in the early days, with commercial testing starting to scale in the US and China, but recent events involving Cruise show that the industry still needs to be apprehensive. There is hope though. In December, Waymo announced it had surpassed 7 million driverless miles across San Francisco, Los Angeles and Phoenix. In this time, it claims to have shown that its vehicles are 6.7 times less likely to be involved in an injury-causing accident compared to human drivers. Despite this success, any incident should and will be scrutinized, and it will take time for regulations and public trust to build.

(Source: PRNewswire)

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Source: IPC

Embedded Capacitance Material

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Embedding components into the multilayer PCB substrate can have many benefits, including reduced board size and improved signal integrity. However, embedded capacitance material (which is not really a component but rather part of the substrate) can improve power integrity dramatically by reducing AC impedance and generally enhancing the performance of the product. It takes up no additional space, is easy to implement (because it is compatible with standard FR-4 processes), and can be cost-effective.

A combination of components is generally required to optimize the power distribution network (PDN). Figure 1 shows how each component has a specific resonant frequency at which point the impedance will be low. The voltage regulator module (VRM), bulk bypass and decoupling capacitors, plane, die capacitance plus BGA via, and via spreading inductance all influence the PDN at different frequencies. The goal is to keep the AC impedance low over the entire signal bandwidth. However, decoupling capacitors are only effective up to a few hundred megahertz. Above that, only on-die capacitors or planar capacitance can reduce the impedance significantly due to their low inductance.

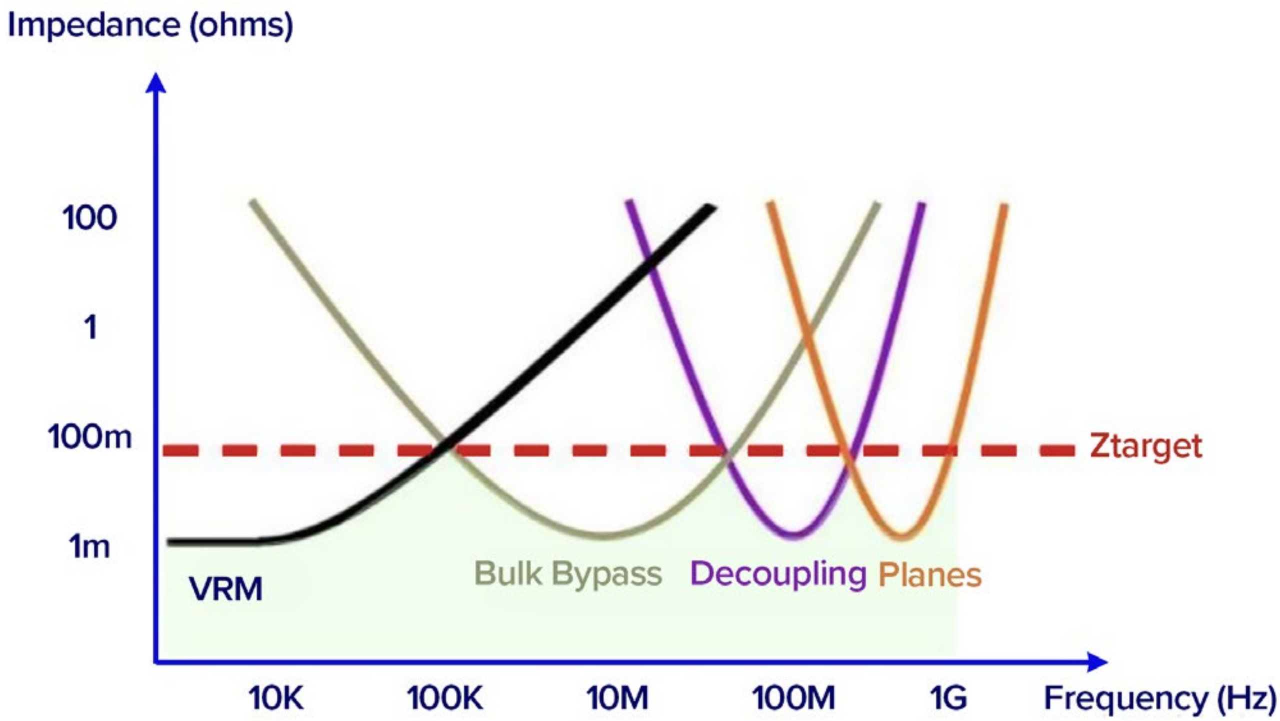


Figure 1: Target impedance, VRM, capacitor, and plane profiles of a PDN.

With the trend to smaller feature sizes and faster signal rise times, embedded capacitance material (ECM) is becoming a cost-effective solution to improve power integrity further. This technology provides an effective approach for decoupling high-performance ICs while reducing electromagnetic interference.

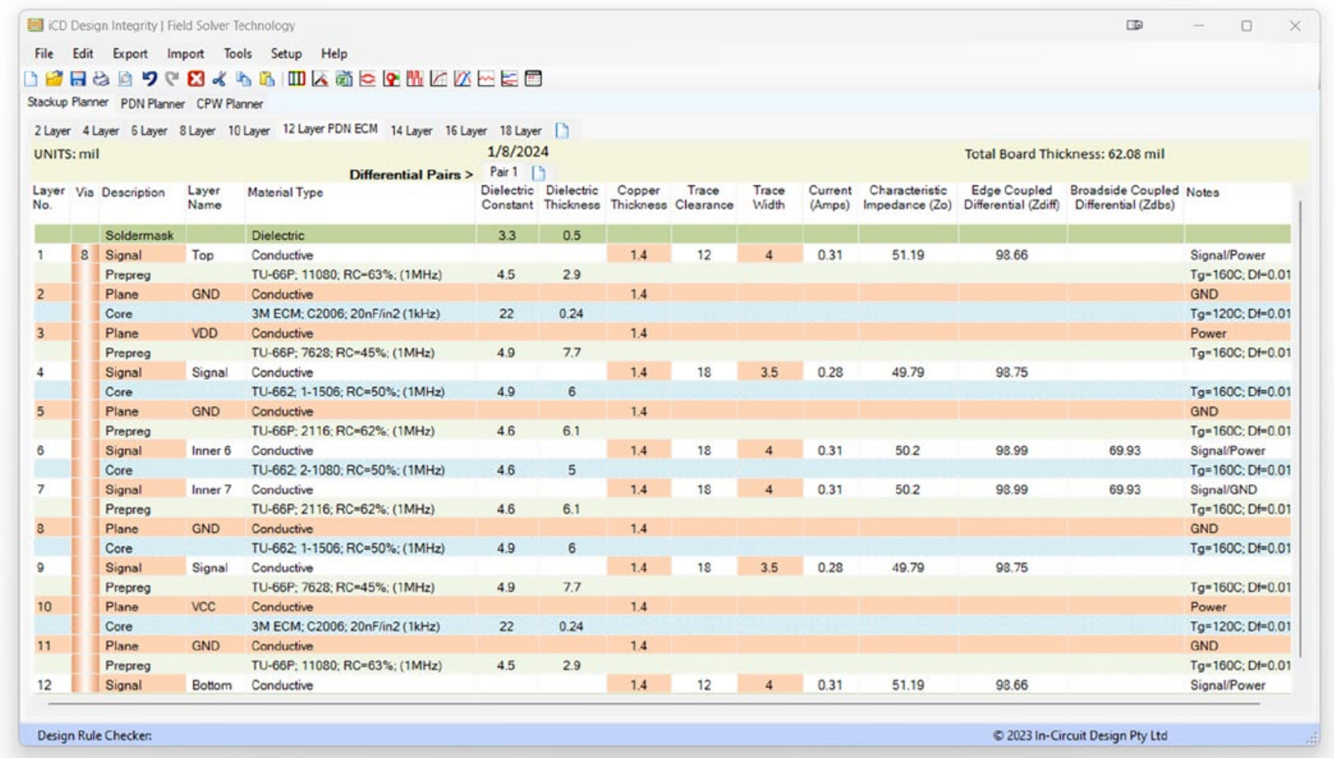
Plane pair cavity resonances contribute to emissions. Smaller plane separation implies less area of equivalent magnetic current at the plane pair edge, or equivalently less local fringing field volume, and therefore lower emissions for a given field strength. However, the smaller the plane separation, the higher the Q of the cavity can be, resulting in higher field strength at the plane pair edges.

Embedded capacitance material comprises copper-clad laminates with very thin dielectric thickness and high dielectric constant. These materials can replace the standard power and ground planes, thereby providing additional capacitance embedded into the PCB stackup. Embedded capacitance materials are defined and described in IPC 4821, *Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards.*

Contrary to normal high-speed design practices, the material has a high dielectric constant (Dk), which increases capacitance, and a high dissipation factor (Df), which dampens electromagnetic energy through the relatively high loss of the material.

Embedded capacitance technology has a very thin dielectric layer (0.24–2.0 mil), which provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1 GHz. These ultra-thin laminates replace conventional power and ground planes and have excellent stability of dielectric constant and dielectric loss up to 15 GHz. The thinner layers of ECM also significantly reduce the capacitor mounting inductance.

The embedded capacitor layer can be placed anywhere in the board stackup (including outer layers if desired). Multiple layers can be used to increase capacitance and lower inductance. Placing the embedded capacitor layer closer to the surface (closer to the ICs as in Figure 2) will reduce via inductance and make the capacitance material more effective, especially



Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	0.5								
1	8	Signal	Top	Conductive			1.4	12	4	0.31	51.19	98.66		Signal/Power
		Prepreg		TU-66P; 11080; RC=63%; (1MHz)	4.5	2.9								Tg=160C; Df=0.01
2		Plane	GND	Conductive			1.4							GND
		Core		3M ECM; C2006; 20nF/in2 (1kHz)	22	0.24								Tg=120C; Df=0.01
3		Plane	VDD	Conductive			1.4							Power
		Prepreg		TU-66P; 7628; RC=45%; (1MHz)	4.9	7.7								Tg=160C; Df=0.01
4		Signal	Signal	Conductive			1.4	18	3.5	0.28	49.79	98.75		
		Core		TU-662; 1-1506; RC=50%; (1MHz)	4.9	6								Tg=160C; Df=0.01
5		Plane	GND	Conductive			1.4							GND
		Prepreg		TU-66P; 2116; RC=62%; (1MHz)	4.6	6.1								Tg=160C; Df=0.01
6		Signal	Inner 6	Conductive			1.4	18	4	0.31	50.2	98.99	69.93	Signal/Power
		Core		TU-662; 2-1080; RC=50%; (1MHz)	4.6	5								Tg=160C; Df=0.01
7		Signal	Inner 7	Conductive			1.4	18	4	0.31	50.2	98.99	69.93	Signal/GND
		Prepreg		TU-66P; 2116; RC=62%; (1MHz)	4.6	6.1								Tg=160C; Df=0.01
8		Plane	GND	Conductive			1.4							GND
		Core		TU-662; 1-1506; RC=50%; (1MHz)	4.9	6								Tg=160C; Df=0.01
9		Signal	Signal	Conductive			1.4	18	3.5	0.28	49.79	98.75		
		Prepreg		TU-66P; 7628; RC=45%; (1MHz)	4.9	7.7								Tg=160C; Df=0.01
10		Plane	VCC	Conductive			1.4							Power
		Core		3M ECM; C2006; 20nF/in2 (1kHz)	22	0.24								Tg=120C; Df=0.01
11		Plane	GND	Conductive			1.4							GND
		Prepreg		TU-66P; 11080; RC=63%; (1MHz)	4.5	2.9								Tg=160C; Df=0.01
12		Signal	Bottom	Conductive			1.4	12	4	0.31	51.19	98.66		Signal/Power

Figure 2: High-speed 12-layer stackup using 3M, ECM of 0.24 mil core thickness.

Table 1: Embedded capacitor materials available in the ICD dielectric materials library

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded Capacitance Material (ECM)	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra-thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High Tg Epoxy Based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi Tg	1.0
Integral Technology	Zeta Cap	Hi-performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Samina	ZBC1000	Buried Cap, hi-performance decoupling	1.0
Samina	ZBC2000	Buried Cap, hi-performance decoupling	2.0

at high frequencies. If more than one embedded capacitance layer is used, they should be distributed so there is a balanced stackup and board warping is kept to a minimum. This also provides decoupling of ICs on the bottom side of the PCB.

The ZBC-2000 laminate uses a single ply of either 106 or 6060 style prepreg, yielding a dielectric thickness after lamination of 2 mils as measured by cross-sectioning. Similarly, ZBC-1000 results in a 1-mil dielectric distributed capacitance material. FaradFlex and Interra buried capacitance products utilize a durable resin system for non-reinforced dielectrics for 1 mil thickness and below. This eliminates the skew associated with the fiber-weave effect in standard materials. Also, with a product range of up to 20 nF per square inch in capacitance density, 3M ECM is the highest capacitance density embedded capacitance material on the market.

These ultra-thin laminates allow a significant layer count reduction in PCBs with better signal performance. With a high withstanding voltage, these glass-free films change the design rules for via diameter and trace width, while still conforming to the manufacturing needs of the fab. Three traces between vias, at a 0.4 mm pitch, are possible and very manufacturable, according to Integral Technology.

It is a common belief that solid power and ground planes act as large, perfect, lumped element capacitors. However, they actually encompass a distributed system of surprising complexity. The distinction between a lumped element and a distributed system involves the relationship between the time delay of the system and the rise time of the signals.

For instance, for a PCB of six square inches, the signals entrapped between the VCC and GND planes create a standing wave, resonating as they reflect from side-to-side, and have a delay time of about 1 ns. If the rise-time of the signal is 5 ns, the lumped condition is satisfied. However, with a much faster rise-time or if the plane is very small (typically one-inch square), then the driver perceives the VCC and GND structure as a distributed object with significant delay. This often occurs on mixed signal/power layers.

This delay causes two issues:

1. During the rising and falling edge, only the portion of the planes and decoupling capacitors located within the close vicinity of the driver can react before the edge has vanished. This frequently results in the noise spike being larger than anticipated.

2. The residual PDN noise from the first event reflects in the cavity (which resembles an unterminated transmission line) a couple of nanoseconds later, back to the driver. If at that precise moment, the driver switches a second time, both pulses (first and second) are superimposed. If the phases are added and the driver has a repetitive pulse (as clocks do), the reflected pulse may build significantly into a standing wave.

One could avoid this potential failure by comparing the round-trip delay across the plane in question to the clock period. If it is close, then an adjustment in the plane size may be an appropriate solution. This may not eliminate all plane resonances but can serve to shift the resonances to other frequencies. Also, adding stitching vias or terminating RC networks in appropriate locations can reduce the extent to which the signal energy spreads through the plane cavity and raises the frequency of structural resonances.

Replacing conventional power/ground planes with an embedded capacitance layer allows for tighter component density, reduced via count, and thus increased signal routing channels. ECMs provide higher capacitance in a PDN, resulting in lower AC impedance and greater damping for power bus ripple. This leads to less intense power plane cavity resonances at gigahertz frequencies due to the material's higher dielectric constant and loss tangent. This lossy property is what makes these materials so useful for power integrity, even when there are insufficient decoupling capacitors. It dampens signal propagation beginning at a lower frequency cut-off and can reduce the signal level if the core voltage is low and/or the routing channel is long.

Key Points

- Embedded capacitance material can improve power integrity dramatically by reducing AC impedance and generally enhancing the performance of the product.
- Decoupling capacitors are only effective up to a few hundred megahertz. Above that, only on-die capacitors or planar capacitance can reduce the impedance significantly due to their low inductance.
- ECM comprises copper-clad laminates with very thin dielectric thickness and high dielectric constant and loss. These materials can replace standard power and ground planes.
- The high Dk increases capacitance and the high Df dampens electromagnetic energy through the relatively high loss of the material.
- These ultra-thin laminates replace conventional power and ground planes.
- Placing the embedded capacitor layer closer to the surface of the stackup will reduce via inductance and make the capacitance material more effective.
- The distinction between a lumped element and a distributed system involves the relationship between the time delay of the system and the rise time of the signals.
- If the plane is very small, then the driver perceives the VCC and GND structure as a distributed object with significant delay.
- If the phases add and the driver has a repetitive pulse (as clocks do), the reflected pulse may build significantly into a standing wave.

Resources

1. Beyond Design by Barry Olney: "The 10 Fundamental Rules of High-Speed PCB Design Part 3," "Plane Crazy, Part 2."
2. "Fabrication of Embedded Capacitance Printed Circuit Boards," by Joel S. Peiffer, 3M.
3. "Embedded Capacitance Material Properties," by Cadence PCB Solutions.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.

UHDI FUNDAMENTALS:

Talking UHDI With John Johnson, Part 3

Interview by Steve Williams
FOR ASC

Editor's note: This is the final installment in a three-part series. View Part 1 and Part 2.

American Standard Circuits is an early adopter of Averatek's A-SAP™ process for its ultra high density interconnect (UHDI) products. In this final part of my interview with industry veteran John Johnson, vice president of business development at American Standard Circuits, we use photos, slides, and materials to discuss what he learned from his previous role at Averatek.

Steve Williams: John, let's talk about the design benefits of UHDI technology.

John Johnson: It's really amazing what you can do with UDHI technology. There are some things you have to watch out for in a design and because you can do the ultra-fine lines and spaces, a designer has a lot of things in their toolkit. You have via-in-pad plated over microvias, stacked and staggered microvias, and other different structures. But when designing with A-SAP, you first need to focus on using that ultra-fine line and then going to the other design aspects. Maybe use staggered microvias or several levels of staggered microvias and then use a stacked microvia if you really have to. That removes some reliability traps we've had to deal with because we couldn't reach those ultra-fine lines.

Figure 1 shows what happens when you can achieve ultra-fine features with this technology. Current subtractive technology is around 75

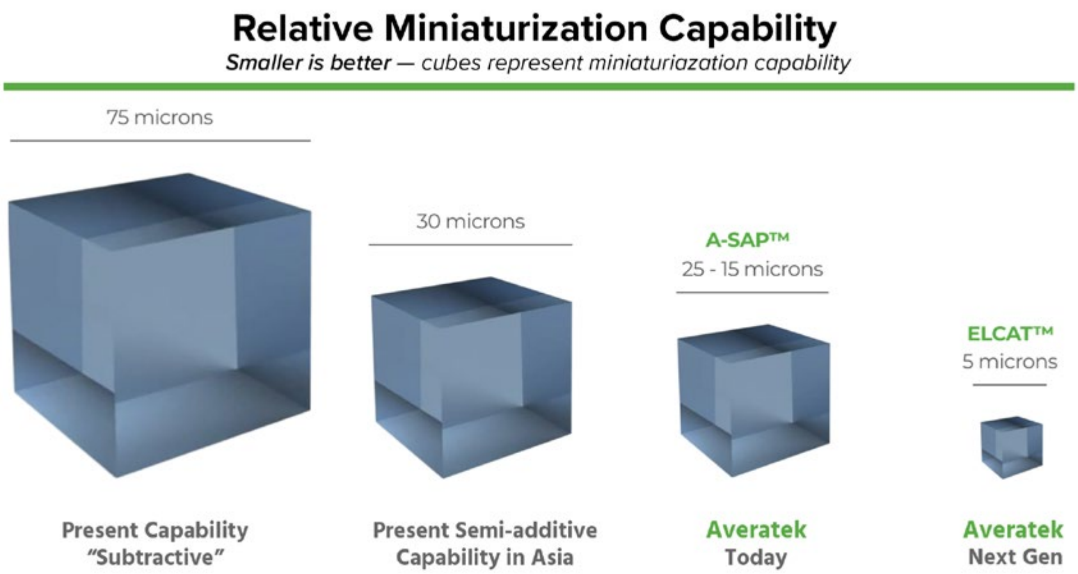


Figure 1.

microns, or 3-mil line and space. Some folks can get down to 2 and 2, but it isn't without some challenge and yield penalty. This technology allows us to get below 25 microns, a present semi-additive capability in Asia. From what we hear, they tend to struggle at 25 microns; it's certainly not a slam dunk. This technology allows us to take it even further into the 15- to 12 ½-micron range. Ultimately, Averatek is working on the next generation of products in the 5-micron range—the semiconductor range. With packaged substrates, they would all love to have that capability today.

John Johnson

So, 25 microns is 1-mil?

Yes.

Then sub-1-mil is 15 microns down to 5. It's almost hard to believe that we can get there. How long until this process comes out?

I've already run down to 15 microns in a fab facility. It's doable and certainly with yield. That's the amazing part. We're actually headed that way ourselves in the not-too-distant future.

Is Figure 2 a visual reference of what you just talked about?

Right. The first spiral is a representation of the 3-mil line and space and that's done in a subtractive format. With the 25-micron, you now get a 9x increase in density. You can see that line is pretty uniform and then you go to the 12.5-micron—a half-mil line and space. You look at that under a scope, and it is beautiful.

I've seen some of your samples and you're right that you have to use some high magnification to even see this definition.

Absolutely. It is very hard to see. You can't use a 10-power eyepiece and expect to see it very easily.

How has the design community accepted and used this, putting out new designs that fabricators like American Standard have to build?

That's where things are still largely in the development stage. There are a lot of designers who are looking at it. The DoD already has designs out there, but it's about bringing this to the marketplace with designs geared for the fine

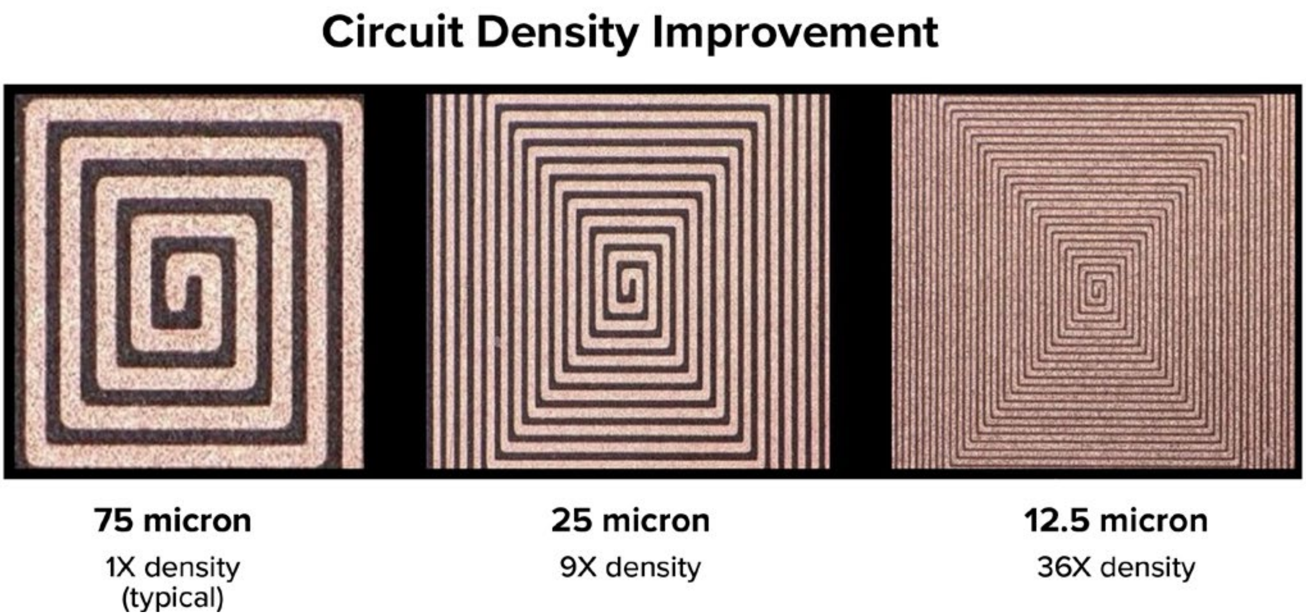


Figure 2.

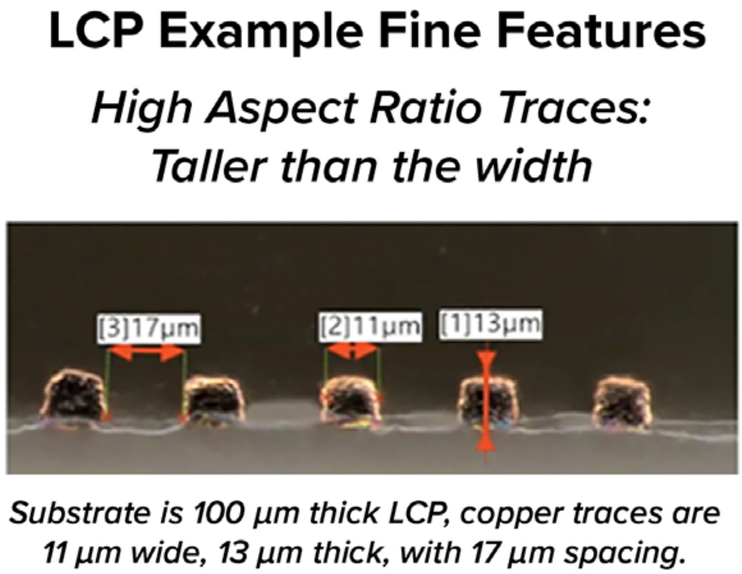


Figure 3.

line and space features. There are many cases where people are trying to get over that hurdle in routing out the fine-pitch devices. As soon as they start utilizing this technology, they will find out how easy it really is.

Interesting. John, tell me about Figure 3. What are we looking at?

This is a sample on liquid crystal polymer material: a 4-mil (100-micron) thick substrate, and how far away these traces can be from a plane layer. They can actually be very tight and close to each other. In this case, it's 17-micron, 11-micron wide traces, and 13 microns high. They can have a lot of electrical effect with each other with differential pairing because they're so tight. That ground plane is so far away that it has very little effect at that point.

Earlier you talked about biocompatibility.

That's the beauty of using noble metals that are stable inside the body. If it's on an LCP or polyimide material, folks are using it in neural probes, glucose monitors, and other types of implantables. Glucose monitors are out there, but when you get something without copper or nickel, it makes it easier to stay longer in the body.

We both work with FreedomCAD and we talked about UHDI at the last webinar we did with them. They're always looking to reduce footprints or improve performance. How do you get the word out to everyone who needs to know this is a viable design option?

We've had several seminars with our customers—discussions like we're having here. That's part of the key, but we're also putting together design guidelines, recommendations, and other things you need to watch out for when you're building parts. ENIG is a great finish, but when you have a 1-mil line and space, you put two-tenths of nickel down, and all of a sudden, it's six-tenths of a mil space, and it gets a little more interesting.

I found it incredible that from a design standpoint, you can eliminate virtually 70% of the ball or solder connections.

Right, and when you start looking at it, you can get rid of that redistribution layer and solder right down to the chip. It's pretty amazing.

John, this has been a fantastic discussion. This technology is truly amazing, and it's something that even 10 years ago nobody could have even dreamed about. You guys are making it happen.

It's very exciting, and that's the fun part. I enjoy what I'm doing. In this part of my career, the ability to bring this to the point of reality is just fabulous.

I appreciate your time and your expertise on this, and we'll be talking to you soon.

Thanks Steve, I welcome every opportunity to talk about this technology. DESIGN007

Steve Williams is president of The Right Approach Consulting. To read past columns, click here.

Are You Ready for 2024?

Connect the Dots

by **Matt Stevenson**, SUNSTONE CIRCUITS

After an eventful 2023, we are excited to begin 2024 with new partners, challenges, and opportunities. I see 2023 as one of the most exciting and significant years at Sunstone Circuits since I began my career with the organization. We joined forces with American Standard Circuits (ASC), an organization that excels in producing ultra HDI, metal-backed/core, RF/microwave, flex, and rigid-flex PCBs for diverse industries.

We are excited about what this strategic alliance will bring in 2024, and with our universe expanding, I've taken another look at some of the topics we covered during the past year. My goal for these articles is to help connect the dots from concept to design to prototyping in order to help designers of every experience level get the most out of their PCBs by:

- Prioritizing high-payoff activities
- Avoiding parts-related manufacturability pitfalls
- Designing for efficient drilling
- Choosing the right CAD tool

With the expansive capabilities ASC brings to the table, we will engage designers on a wider range of projects and larger-scale production. It is worthwhile to review key topics from 2023 that are vital to a smooth process from design to assembly.

Prioritizing High-payoff Activities[1]

High-payoff activities (HPAs) are vital to achieving production excellence and fall into five categories:

- Safety
- Quality
- On-time delivery
- Cost reduction/efficiency gain
- Continuous improvement

Safety

Safety should be the top priority for every PCB manufacturer. Key HPAs in the safety arena include:

- Utilize engineering controls to error-proof (Poka-Yoke) safety standards.
- Use personal protective equipment (PPEs) to improve the safety of a working environment, especially in departments where chemical processes are used.
- Offer ongoing training to both new and current employees to ensure safety on the production floor.

Quality

Quality should be top of mind with respect to every aspect of production and embedded in the organization's culture. The quality cycle begins with process development and persistent evaluation of production output data in search of process variances. This will help to determine where in the manufacturing cycle process quality output meets or exceeds expectations.

On-Time Delivery

Quality products do not arrive late. To ensure on-time delivery, manufacturers should focus on the following HPAs:

- Process the order correctly the first time
- Know the capacity limitations of the facility
- Continuously learn to overcome processing challenges using root cause analysis

Cost Reduction/Efficiency Gain

Efficiency gains and cost reductions sound like the same thing, but they are more like two sides of the same coin.

- Cost reduction is measured by use of fewer consumables
- Efficiency gains are the result of utilizing less labor

To improve both, manufacturers need meaningful, granular metrics in place to measure how much of each is being used. It is essential to understand labor costs at a granular level, including how process and technology impact operational efficiency down to the individual level.

Continuous Improvement

Continuous improvement is arguably the most important of the five HPAs. Manufacturers who implement and sustain quality management systems (QMS) will realize continuous improvement across the production floor.

Common elements of successful continuous improvement programs include:

- Utilize Lean, Six Sigma, 5S, and 5-Why root cause analysis.
- Perform daily process walks, known as Gemba in the Lean Manufacturing philosophy. These provide daily observation of processes occurring in real-time and can uncover resource gaps.
- Set the stage for solid countermeasures with processes like Plan-Do-Check-Act (PCDA), a method to continually improve and measure results that will prevent reoccurrence of an observed weakness or gap in the process.

Putting the five HPAs into daily practice in any production process will help keep the production team laser focused on achieving production excellence through the continual improvement cycle.

Avoiding Parts-Related Manufacturability Pitfalls[2]

Issues with parts fit are one of the most frequent causes of delay and cost overruns. These are five methods to avoid common, parts-related manufacturability issues.

- **Pay close attention to pinhole size.** It's important to check component physical dimensions, take dimension tolerances into consideration, and account for variation that can impact fit. In addition to watching part sizes, pay close attention to the minimum, nominal, and maximum material conditions for the original part.
- **What to do when the land pattern differs from pin size.** One of the most frustrating mismatches with alternate through-hole parts is when the land pattern matches, but the pin size is off. When designing the land pattern, the pin size and tolerance range for components can be found in the product datasheet. Use that information to plan the proper hole size.
- **Datasheets can disagree with CAD software.** Third-party CAD libraries can contain millions of different parts, so discrepancies are inevitable. When the datasheet and the library part don't match up, address the delta before submitting the design. Always check any library part for accuracy before using it the first time.
- **Pay attention to pinouts when using alternate vendor parts.** Even if pin size and through-hole size are a con-firmed match, and even if solder joints appear sound, a part can still not work as expected. Similar parts with the same footprint might look like they should act identically, but they won't always have the same pinout. Each transistor has a gate, drain, and source, but different manufacturers can differ in what goes where.
- **Be aware of mechanical fit.** Physical size of a component can keep parts from fitting into designated spaces. MMC body size should be the rule, so pay close attention to the tolerance range. As parts get larger or are sourced from multiple vendors, footprint size may need to expand considerably to accommodate all dimension and tolerance variables.

Designing for Efficient Drilling[3]

Drilling is one of the most fundamental steps in printed circuit board manufacturing. Designers can take several steps to improve the efficiency of drilling and help cut down on errors:

- Reduce the variety of through-hole sizes from the PCB design, allowing fewer tool changes.
- Avoid unnecessary design elements that can increase the chances for burring. Among these are higher copper weights and anything that can keep layered boards from sitting flat against each other.
- Minimize hole sizes to reduce the amount of material that needs to be drilled and removed from a board. In addition, a clever design can optimize spacing between the holes, which reduces the amount of motion a drill needs between drilling. These design optimizations might seem minimal, but their savings can add up for large manufacturing runs.
- Optimize the through-hole and pad sizes to facilitate the drilling process and ensure high-quality PCB manufacturing.

Accurate drilling is key to a reliable and efficient board, and by focusing on these essential elements, designers can produce PCBs with fewer errors and failure rates.

Choosing the Right CAD Tool[4]

Each designer has different needs from a CAD tool, and needs can vary by project. We recommend evaluating CAD software using the following criteria:

- **Price:** When evaluating tools, make sure they are actively maintained and have an acceptable level of user support. CAD tools funded and developed by PCB manufacturers are built to work with their manufacturing process, so make sure their capabilities match your design requirements not just their capabilities. Commercial packages can become expensive quickly, so pay attention to the limits placed on products with multiple tiers of pricing to be sure important features are not locked behind an expensive paywall.

- **Component libraries:** A typical designer might need a library of about 10,000 parts. When looking at the library offered by a CAD tool, confirm that the requisite parts are available. Look for commonly used parts and check if the tool comes with access to specialized libraries required for the project.
- **Ease of use:** CAD tools should be intuitive and easy to use. Ease of use is an area where less expensive, open-source software tends to lag behind. If price is an important factor in the decision-making process, the result can be a balancing act between price and usability.
- **Help and documentation:** Ensure that the CAD tool provider offers user support early in the process. CAD tool software providers should make their documentation available online; quality documentation can be a huge help to designers who need questions answered in a hurry.

The most important part about picking a CAD tool, though, is that it shouldn't make designing too much of a chore. You want designing to be productive and efficient, and in the end, maybe that's the most important element to evaluate when you're trying out different tools.

Ready for 2024

As we move into 2024, I look forward to exploring best practices on a variety of PCB design and manufacturing topics. Sunstone's alliance with ASC has expanded our PCB universe and opened the door for a more in-depth look at the PCB designer's role in ensuring the smooth manufacturing of really cool stuff, from design to prototype to large-scale production. DESIGN007

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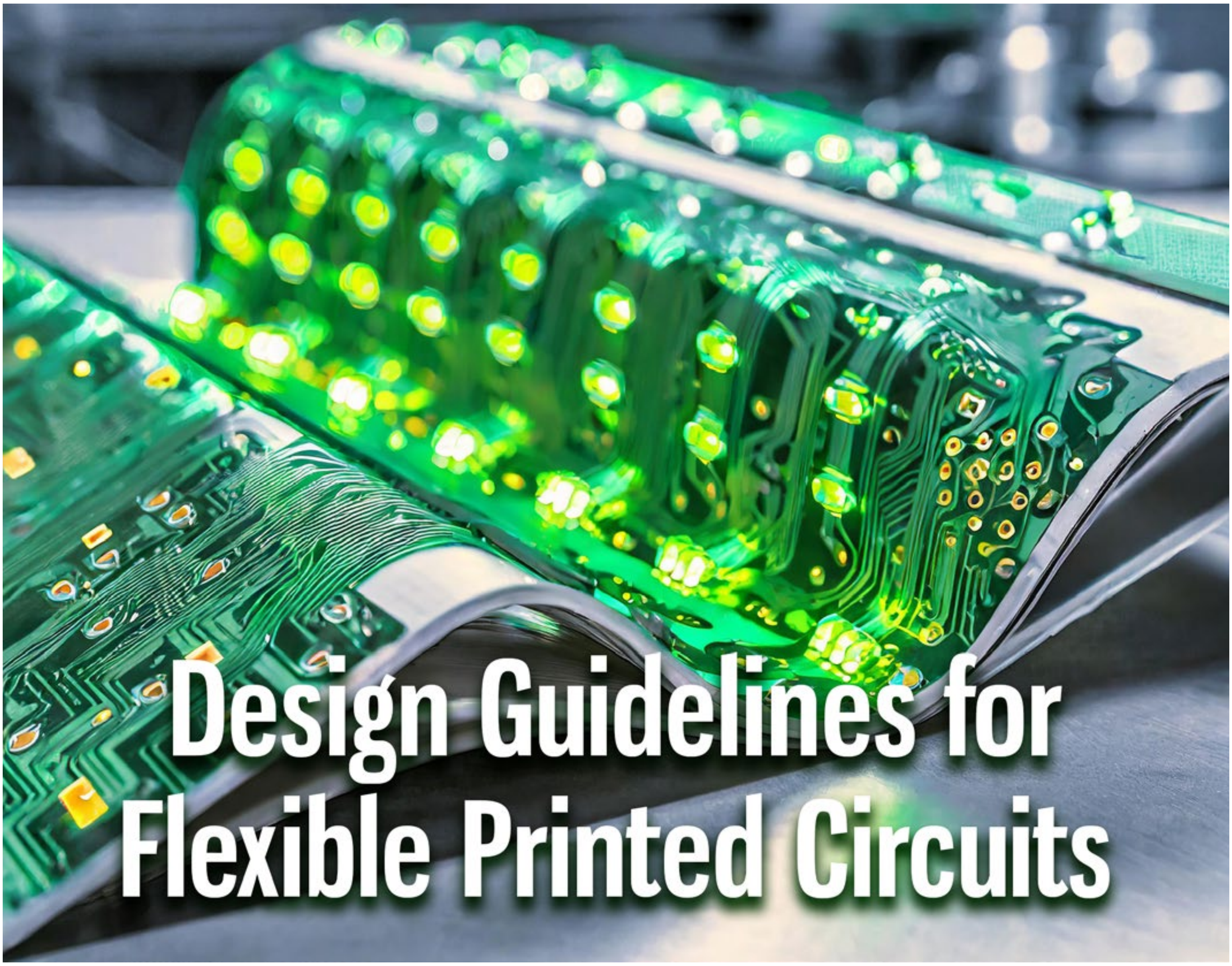
4. "Choosing the Right CAD Tool," by Matt Stevenson, *Design007 Magazine,* October 2023.

Matt Stevenson is vice president and general manager of ASC Sunstone Circuits. To read past columns, click here.

Download Matt's book, *The Printed Circuit Designer's Guide to... Designing for Reality* and listen to the podcast here. You can view other titles in the I-007eBooks library.



Design Guidelines for Flexible Printed Circuits

Article by Chris Keirstead
PFC FLEXIBLE CIRCUITS

An important but sometimes overlooked aspect of flex and rigid-flex fabrication and assembly is the flex circuit tail, which is attached to a rigid PCB with pressure-sensitive conductive adhesives. This sub-assembly is becoming very common. We often see this applied to glass displays and microelectronic applications.

But this method of attachment without connectors is not as straightforward as one may think. The wide varieties of circuitry to be bonded create many attachment challenges. The best track configuration is not always possible, so one must be familiar with the optimum layouts as well as what is not recommended when considering these trade-offs. Less than optimum trace and pad layouts result in the need for more customization and smaller processing window variations for the bonding process.

Here are some common configurations that flex assemblers have developed, and the preferred approach for the method of bonding.

Interposer Effect and Co-planarity Adjustment

Bonding imbalance results from either bad co-planarity between the bonder head and stage or a thickness deviation of the flex and PCB materials. The interposer will absorb these discrepancies to some extent and help bring the

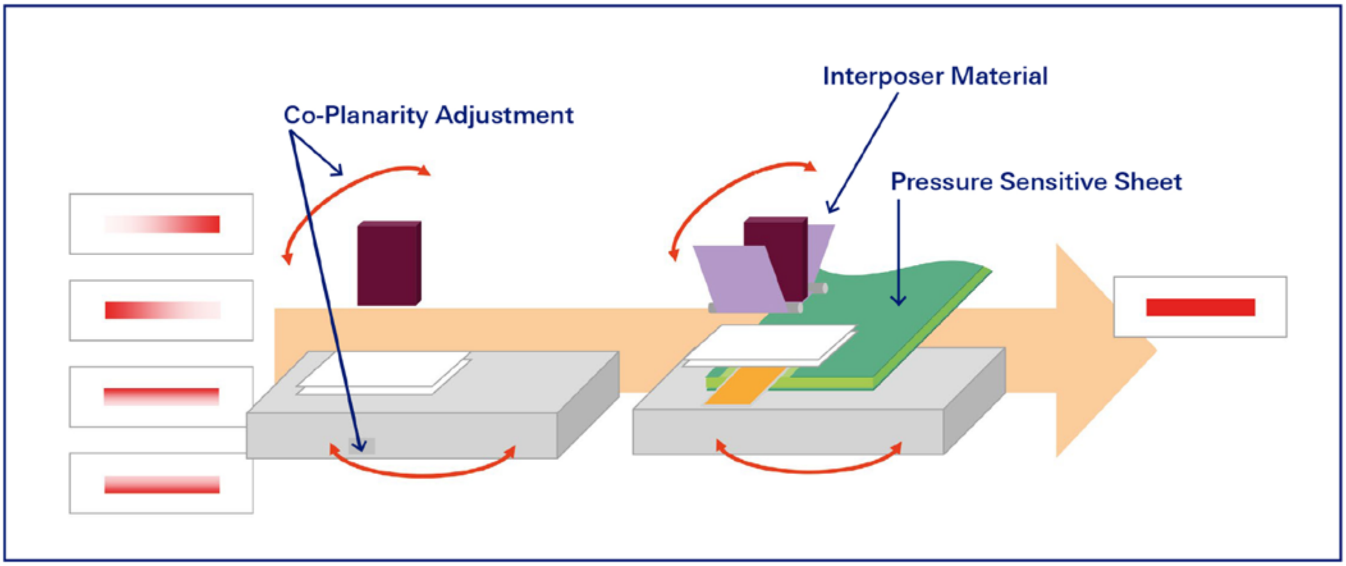
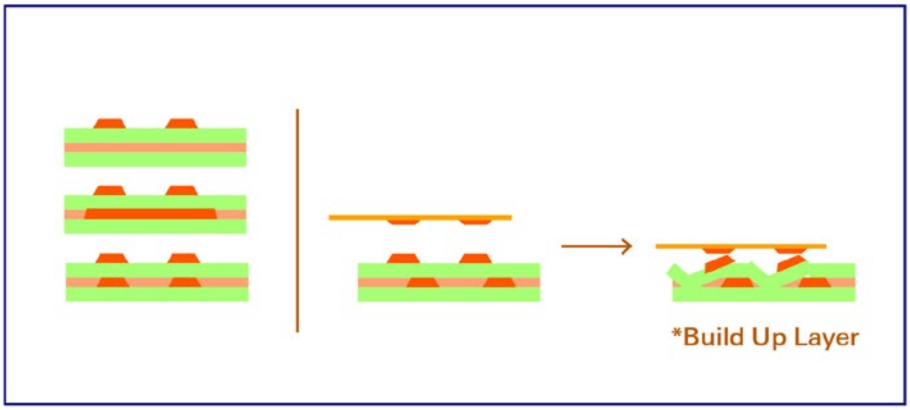


Figure 1: Prescale pressure measurement film can help operators address bonding imbalance issues.



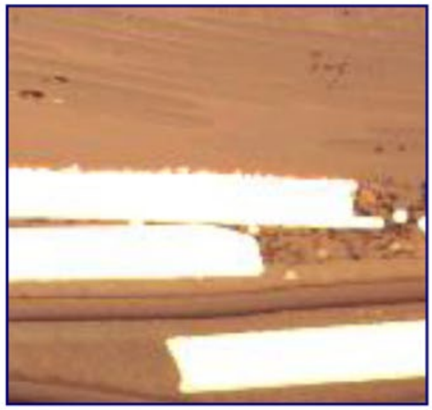


Figure 2: The preferred design (left), and not preferred (right). Alignment is critical.

bonding results in parallel. A homogeneous red color on the Prescale pressure measurement film shown in Figure 1 provides the result.

If bonding is imbalanced, the developed color will also be uneven; adjust the bonder tool or stage until you achieve uniformity of color. Since Prescale will turn color with heat and pressure, confirm the color in short bonding time and low pressure. To confirm the condition of equipment, please do not use cushion materials.

Preferred Layer Structure for Flex and Rigid Circuits

Any circuitry running below the bonding lead is not desirable, and can prevent stable compression from the bonding head.

Design Guidelines for Flex and Rigid PCBs

An appropriate design is shown in Figure 3. The line width should not be too large.

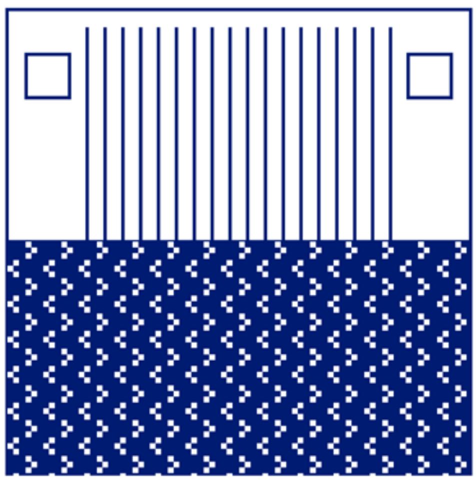


Figure 3: Example of an appropriate design.

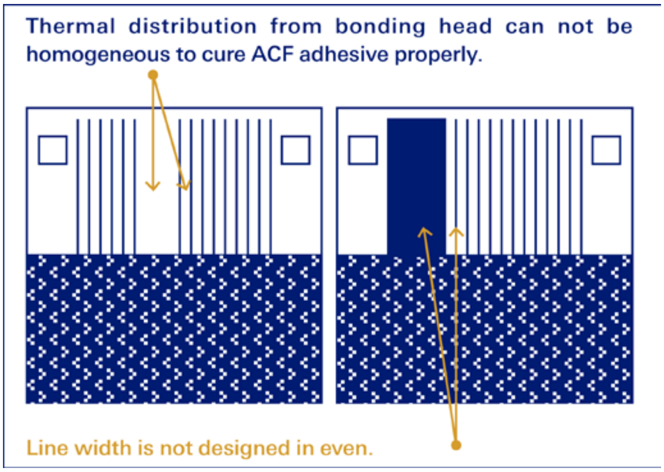


Figure 4: A poor design. Different thermal conductive lead widths will complicate temperature verification.

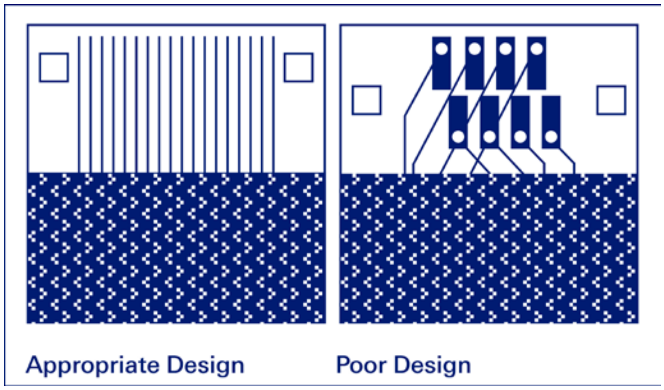


Figure 6: A good design (left) and a poor design (right). The poor design may cause partial compression, because only the crossing point could be compressed on the back side of the flex circuit.

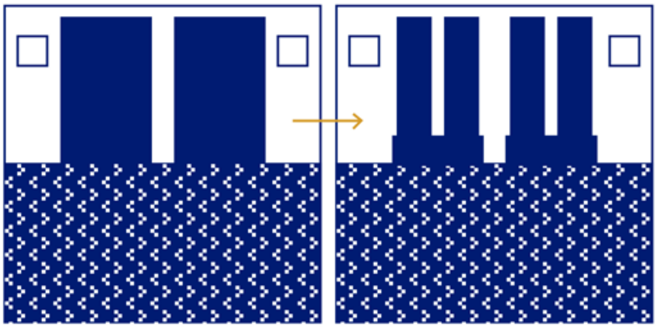


Figure 5: With large line widths, large gold areas are not necessary.

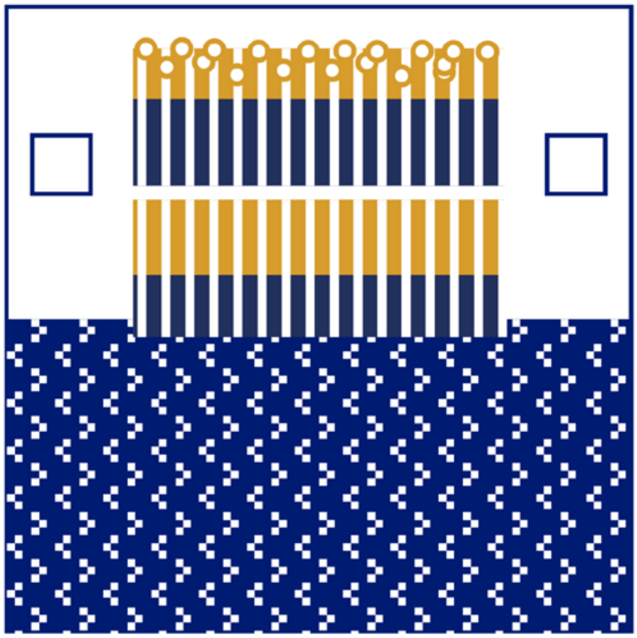


Figure 7: Example of the ACF bonding area on the center of two bonding lines, which can affect peel strength.

A poor design is shown in Figure 4. Note that the line and space ratio is not designed to be even. Thermal distribution from the bonding head must be homogeneous for ACF adhesive to cure properly.

An example with a large line width is shown in Figure 5. Large gold areas are not necessary; adhesives actually have lower adhesion on a gold surface. Large leads can be divided among multiple leads.

In Figure 6, we see a comparison of an appropriate design and a poor design. Leads should be designed in a straight and simple line to provide enough thermal compression from the bonding head.

When the ACF bonding area is to be applied on the center of two bonding lines with the design shown in Figure 7, seepage of the ACF adhesive will not be good enough to pass the peel strength test. The rear lead running on the back side of the flex circuit should not be located on the center of a lead on the front side.

Figure 8 shows two similar but less than optimum designs. The back side lead should not be designed between leads on the front side (left). Avoid any circuit design that may cause a short by allowing conductive particles to become jammed in between leads (right).

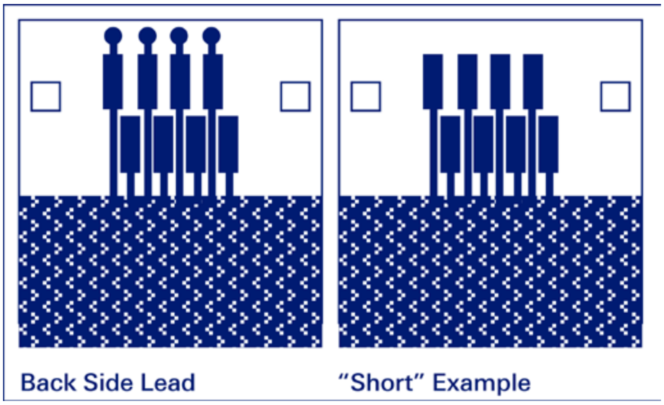


Figure 8: Two examples of problematic designs.

Coverlay and Resist Coating on PCBs

Finally, be sure to remove coverlay and resist around the leads and bonding area to apply optimum bonding pressure during thermal compression. Figures 9 and 10 show comparisons between a preferred design and one that is not.

Summary

Rigid-flex circuits have become almost ubiquitous, and they're now found in all kinds of everyday electronic devices. Designing and attaching a flexible circuit to a rigid PCB presents a variety of challenges, but designers who follow the guidelines in this article should have very few issues. As always, speak to your flex fabricator before you begin the design process; they can probably help you save time and money on your rigid-flex circuits. **DESIGN007**

Chris Keirstead is a sales manager with PFC Flexible Circuits.

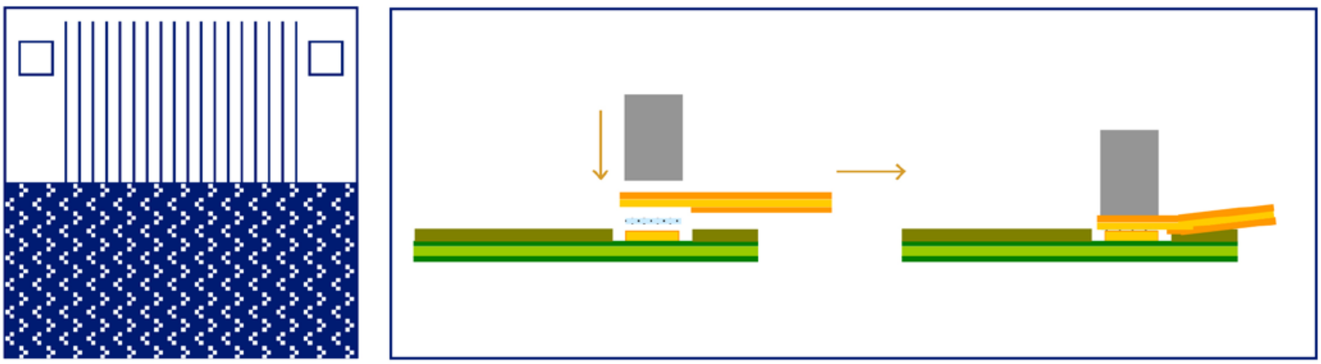


Figure 9: A preferred design with coverlay and resist removed from space around leads and bonding area.

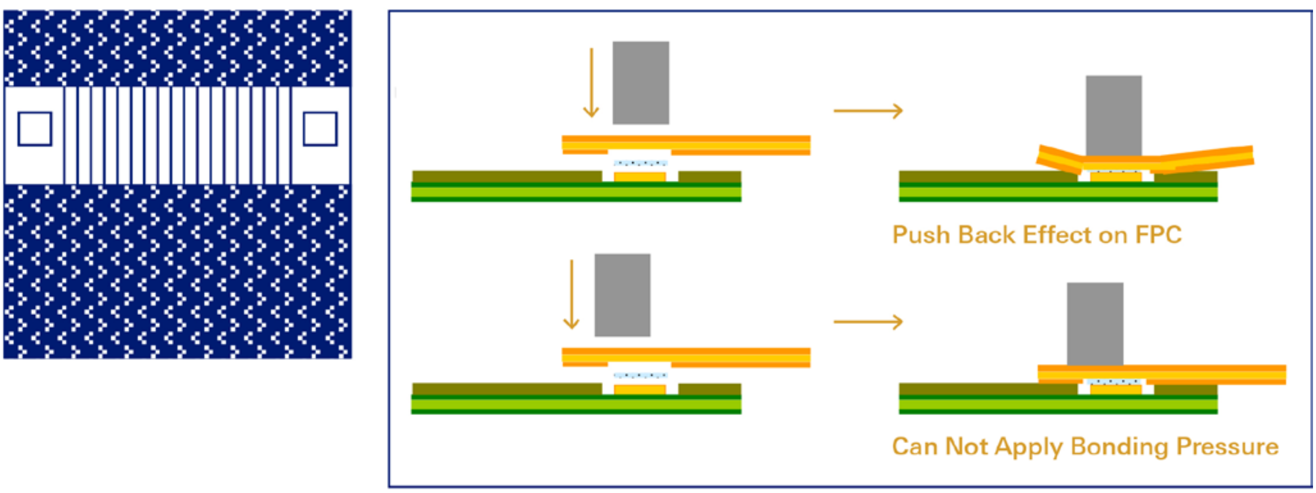


Figure 10: An example of a non-preferred design showing the results when coverlay and resist are not removed correctly.

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PCB Design II section 1	Mar. 18–May 15	M/W	8 am PT/11 am ET/5 pm CET	8
PCB Advanced Design Concepts	Mar. 18–May 15	M/W	3:30 pm PT/6:30 pm ET	8
PCB Design II section 2	Mar. 19–May 16	T/TH	3:30 pm PT/6:30 pm ET	8
PCB Design I (Brazil)	Apr. 22–May 29	M/W	7 pm BST/ 6 pm ET	6
Top Lead-free Production Defects & Issues – Causes, Remedies & Prevention	Apr. 23–May 2	T/TH	8 am PT/11 am ET/5 pm CET	2

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Embedded Design: A Term With Multiple Meanings

Flexible Thinking

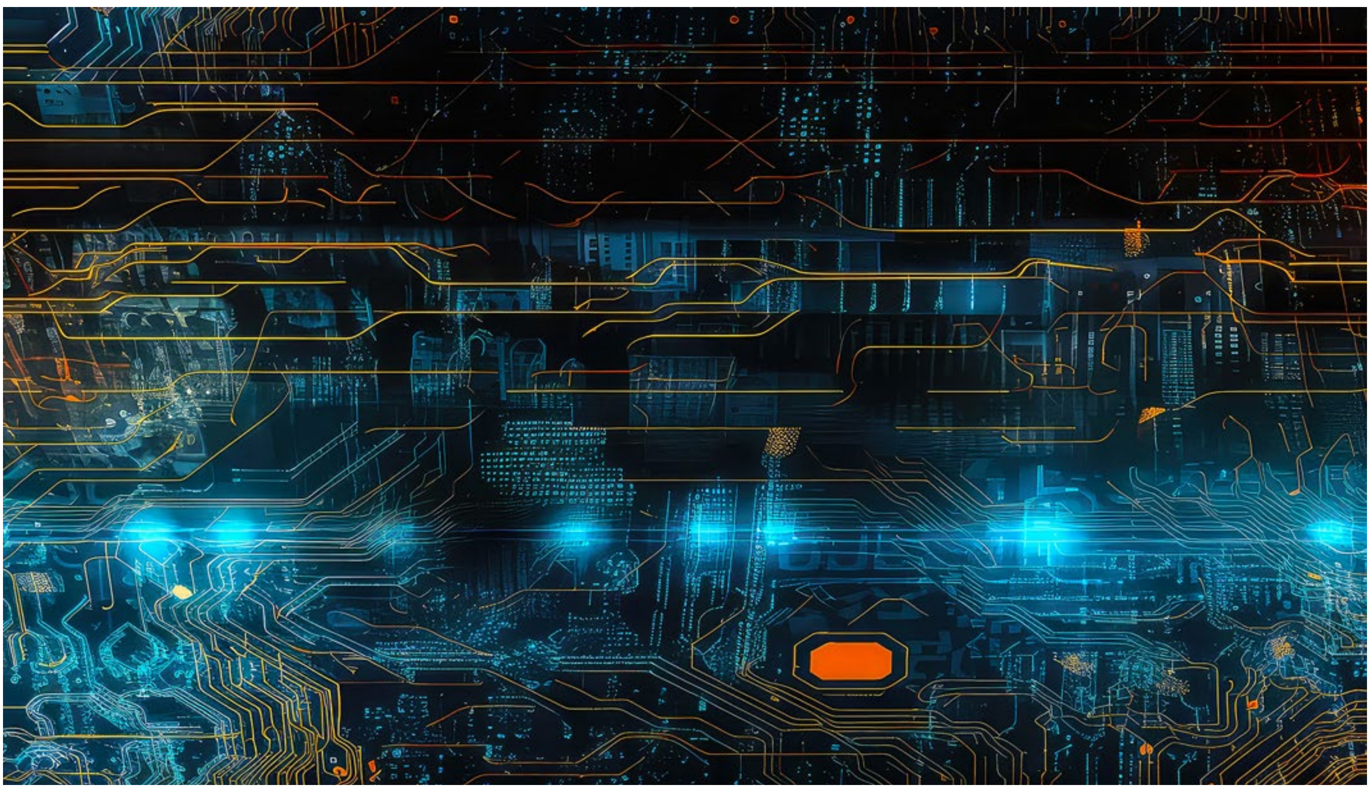
Feature Column by Joe Fjelstad, VERDANT ELECTRONICS

With the seemingly endless ways that electronic products are worming their way into our lives, what was once “nice to own” is increasingly considered indispensable. The capabilities of these products have been driven by relentless improvements at every level of the manufacturing chain, from individual transistors (which are approaching Angstrom levels) to systems the size of buildings supporting Bitcoin mining and increasingly distributed AI products.

Along that chain of electronically interconnected products, the term “embedded design” is used at several points. Among high-level product developers, embedded design commonly refers to a process of designing and integrating end-product-specific computer systems into next-level systems to perform a chosen set of functions within the larger system, often with hardware and software also integrated, where the end products cover a wide spectrum of applications, everything from consumer electronics to automobiles, medical devices, military/aerospace products, and beyond.

A Little Background

Of greater interest here is the concept of the integral integration or embedment of electronic components (or electrical/electronic



function) into the actual electronic interconnection substrate (typically a printed circuit). The concept of embedded/integrated devices and/or their function has deep roots in the printed circuit industry. Seventy-five years ago, the U.S. government published "Printed Circuit Techniques" to promulgate knowledge gained in electronics research during World War II. It was also meant to jumpstart the post-war electronics industry in the U.S., as it described methods for making resistors in situ and trimming them to value in place. Such methods have been employed ever since, though more often on the inner layers of multilayer boards.

The concept of distributed capacitance evolved with the introduction of multilayer PCBs in the 1960s and '70s when it was realized that the stacking of multiple layers of circuits, including ground and power, provided an opportunity to incorporate distributed capacitance intrinsically embedded and made possible by the built-in parallelism of adjacent layers which naturally contributed to the capacitance between them. Material suppliers recognized the opportunity and began to explore the use of alternative materials for use in multilayer boards, including the use of high-permittivity dielectric materials to improve and better control distributed capacitance. Designers soon began considering capacitance a key factor in signal integrity and power distribution. The terms "buried capacitance" and "embedded capacitance" are much a part of the current printed circuit industry lexicon.

The concept of embedded/integrated devices and/or their function has deep roots in the printed circuit industry.

Embedded discrete components also have a long history, depending on how rigid one wants to define embedment. One of the first volume applications was "chip on board" (COB) products that ushered in the video game console industry in the mid-1970s. These structures could arguably embrace both ends of the spectrum described thus far. They were programmed chips attached to PCBs, wire-bonded to make interconnections, and encapsulated with epoxy. The method obviated the need for the packaging and subsequent solder assembly of the chip. The assembly was then given a housing identifying the game, and edge card connections were used to plug the module into the game player system.

Common Approaches

Turning attention to the embedment of other passive functions to provide discrete components, including discrete capacitors (as distributed capacitance as discussed earlier), resistors, and inductors, the most common approach has been the attachment of the component to etched lands on inner layers of the multilayer PCB using solder. This approach requires cavities be made in the prepreg and/or the inner layer materials used in constructing the board. Yet unstated but presumed to be understood, the purpose of embedding discrete devices has typically been to free up space on the outer surfaces of the printed circuit.

Beyond embedment of components, several techniques have been developed for forming the components in situ on inner layers. This was seen as an opportunity in the 1970s, as special laminates having bimetallic foils of copper and more resistive metals or coatings were developed to produce chosen resistor values by selectively etching the different foils to create the number of squares required in the resistive layer. However, the printing of a resistive material between ends of copper traces is a long-time practice. The resistor value can be "roughed in" by choosing the right value for the ink and the value "fine-tuned" by laser trimming the material to the desired value.

I had the notion 20 years ago that it would also be possible to create vertical resistors by drilling from one layer to another and filling the hole with a resistive material. The depth and diameter of the via would account for the number of squares and the resistive ink would be selected by the designer and the needs of the design. Once filled, copper would be plated over the top of the resistor material and a relatively small footprint resistor could be had. They could potentially be quite useful for termination resistors. (U.S. Patent No. 7049929B1)

Inductors are the other final passive function adapted for embedment into printed circuits. Inductors are well understood and follow a few established rules. The features that define inductance can be readily produced by standard printed circuit processing. In general, inductance is determined by the length of the spiral and number of turns. The spacing between turns will control the resonant frequency of the inductor. In general, a wider spacing will typically reduce capacitance and raise the inductance frequency. In a multilayer board, a multiple-layer inductor can be produced, increasing the number of turns without increasing the footprint.

In conclusion, the concept of embedded design is claimed by more than one segment of the electronics industry, though I believe that embedded component design in PCB construction predates the more recent interpretation of meaning. No matter, in the context of the application, the meaning should be clear to all. DESIGN007

Resources

For those wishing to take a deeper dive into the subject matter, Vern Solberg, an industry veteran and IPC Hall of Fame Award recipient, provides better understanding with additional detail and graphics.

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."

After Three Years on Mars, NASA's Ingenuity Helicopter Mission Ends

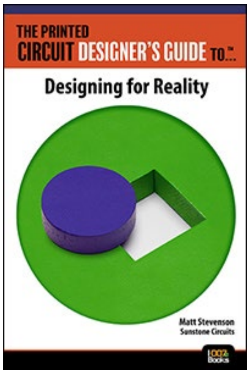
After its 72nd flight on January 18, 2024, NASA's Ingenuity Mars Helicopter captured this color image showing the shadow of a rotor blade damaged during a rough landing. NASA's history-making Ingenuity Mars Helicopter has ended its mission at the Red Planet after surpassing expectations and making dozens more flights than planned. While the helicopter remains upright and in communication with ground controllers, imagery of its January 18 flight sent to Earth this week indicates one or more of its rotor blades sustained damage during landing and it is no longer capable of flight.

Originally designed as a technology demonstration to perform up to five experimental test flights over 30 days, the first aircraft on another world operated from the Martian surface for almost three years, performed 72 flights, and flew more than 14 times farther than planned while logging more than two hours of total flight time.

"The historic journey of Ingenuity, the first aircraft on another planet, has come to end," said NASA Administrator Bill Nelson. "That remarkable helicopter flew higher and farther than we ever imagined and helped NASA do what we do best—make the impossible possible."

(Source: NASA)

TOP TEN EDITOR'S PICKS



Book Excerpt: *'The Printed Circuit Designer's Guide to... Designing for Reality,'* Chapter 4

With an understanding of the overall manufacturing process, we can dive into the most important design-for-reality areas. Most front-end CAM tooling departments can do a great deal to help turn a marginal design into a manufacturable product, but even these superheroes have limitations to the ir powers. Some of the most common edits that a CAM tooler makes will not be visible to most people but can drastically improve the yield and reliability of the product in manufacturing and beyond.

Mya Gatzke: Mapping Out Her Future


Mya Gatzke

At PCB Carolina, I spoke with several engineering students from the Class of 2027, and their excitement about this industry was contagious. One such freshman, Mya Gatzke, sat down for an interview. As she points out, an electrical engineering degree will come in handy in a wide variety of careers.

What Do You Know About PCB Manufacturing?


Tony Bell

Much of a designer's job involves creating a product that is compatible with the capabilities of their chosen fabrication and assembly providers. But very few PCB designers have visited a board shop or assembly facility in decades, if ever, and seemingly simple DFM problems continue to dog our industry. What manufacturing concepts are designers missing?

Synopsys to Acquire Ansys, Creating a Leader in Silicon to Systems Design Solutions

Synopsys and Ansys have entered into a definitive agreement under which Synopsys will acquire Ansys. Under the terms of the agreement, Ansys shareholders will receive $197.00 in cash and 0.3450 shares of Synopsys common stock for each Ansys share, representing an enterprise value of approximately $35 billion based on the closing price of Synopsys common stock on December 21, 2023.

Altium Launches Altium 365 BOM Portal

Altium has launched the BOM Portal within the Altium 365 platform. The BOM Portal is engineered to dramatically enhance collaboration between engineering and procurement teams, offering a unified approach to managing bills of materials (BOMs) in electronics design.

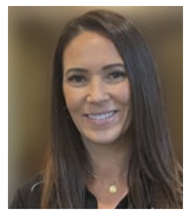
Dana on Data: Nuke the Netlist

I bet that title caught your attention. Has Korf finally lost his mind? The central theme of my I-Connect007 columns, as well as presentations at PCB technical meetings, has focused on improving data package quality sent from designers to manufacturers. The goal is to transfer the design information to manufacturing and build the PCBs as-is. No semi-automated DFM, stackup generation, CAM editing, or data quality analysis should be needed.

IPC's Advanced PCB Design Concepts Training Course

The Advanced PCB Design Concepts course, 6:30 to 8:30 p.m. EDT March 18 to May 15, 2024, with virtual classes held on Mondays and Wednesdays, will start with the design of HDI and advanced packaging concepts. This will be followed by embedded component design and the students will see how concepts from HDI are used in the implementation of embedded components.

Save Your Design by Understanding Fab Processes



I recently met with Laura Martin, director of applications engineering for Summit Interconnect. Laura has been at Summit for about a year, moving into the role from a similar position at Insulectro. She has now become Summit's go-to design for manufacturing (DFM) expert, and she's working to move DFM further up in the design cycle, eliminating unpleasant surprises at CAM.

Beyond Blueprints: Early Involvement Shapes Superior Fab Outcomes

As technology advances, the demand for reliable PCBs with ever-increasing circuit density surges and highlights the pivotal role of fabrication in shaping the electronics landscape. In this intricate dance between innovation and execution, a symbiotic relationship emerges between designers and fabricators. This forms the core of success.

Designers Notebook: What Designers Need to Know About Manufacturing, Part 1

The designer needs to have a working understanding of two key manufacturing operations: basic circuit board fabrication procedures and assembly process practices. For printed circuit board manufacturing, the number of steps required to produce the printed circuit board correlates to the circuit board's complexity.

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- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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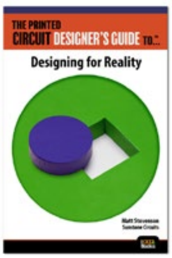
Educational Resources

I-007eBooks The Printed Circuit Designer's Guide to...

Manufacturing Driven Design

by Max Clark, Siemens

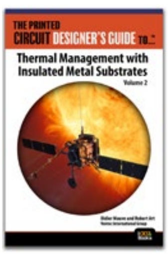
This book introduces a new process workflow for optimizing your design called Manufacturing Driven Design (MDD) and is a distinct evolution from DFM. Manufacturing certainly plays a critical role in this process change, and manufacturers do certainly benefit from the improved process, but it is design teams that ultimately own their overall product workflow; they are the ones who need to drive this shift. Get empowered now!



Designing for Reality

by Matt Stevenson, Sunstone Circuits

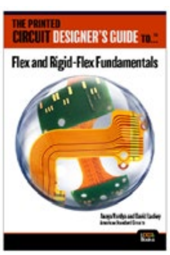
Based on the wisdom of 50 years of PCB manufacturing at Sunstone Circuits, this book is a must-have reference for designers seeking to understand the PCB manufacturing process as it relates to their design. Designing for manufacturability requires understanding the production process fundamentals and factors within the process. Read it now!



Thermal Management with Insulated Metal Substrates, Vol. 2

by Didier Mauve and Robert Art, Ventec International Group

This book covers the latest developments in the field of thermal management, particularly in insulated metal substrates, using state-of-the-art products as examples and focusing on specific solutions and enhanced properties of IMS. Add this essential book to your library.



Flex and Rigid-Flex Fundamentals

by Anaya Vardya and David Lackey, American Standard Circuits

Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

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