NOVEMBER 2023

I-Connect007

DESIGN007 MAGAZINE

A Distinct Evolution from DFM

Look Inside

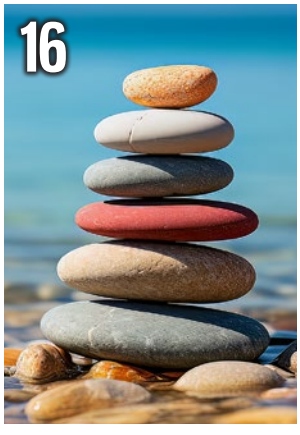
"In an industry racing against time, MDD is the key to staying ahead."

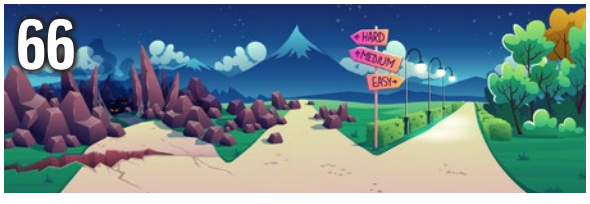
Ammar Abusham
DFM Integration Engineer (AR EE Team)
Meta Reality Labs

DESIGN007 MAGAZINE

Simplfication

In this month's issue, our expert contributors explain how to design PCBs without making them complex and over-constrained—whatever the level of technology. We also discuss the effect your decisions and tradeoffs have on design complexity, as well as the need to thoroughly understand how electrical and manufacturing limitations can lead to over-constraining your board.





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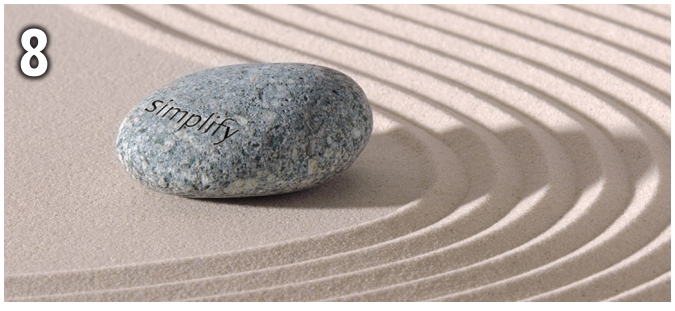

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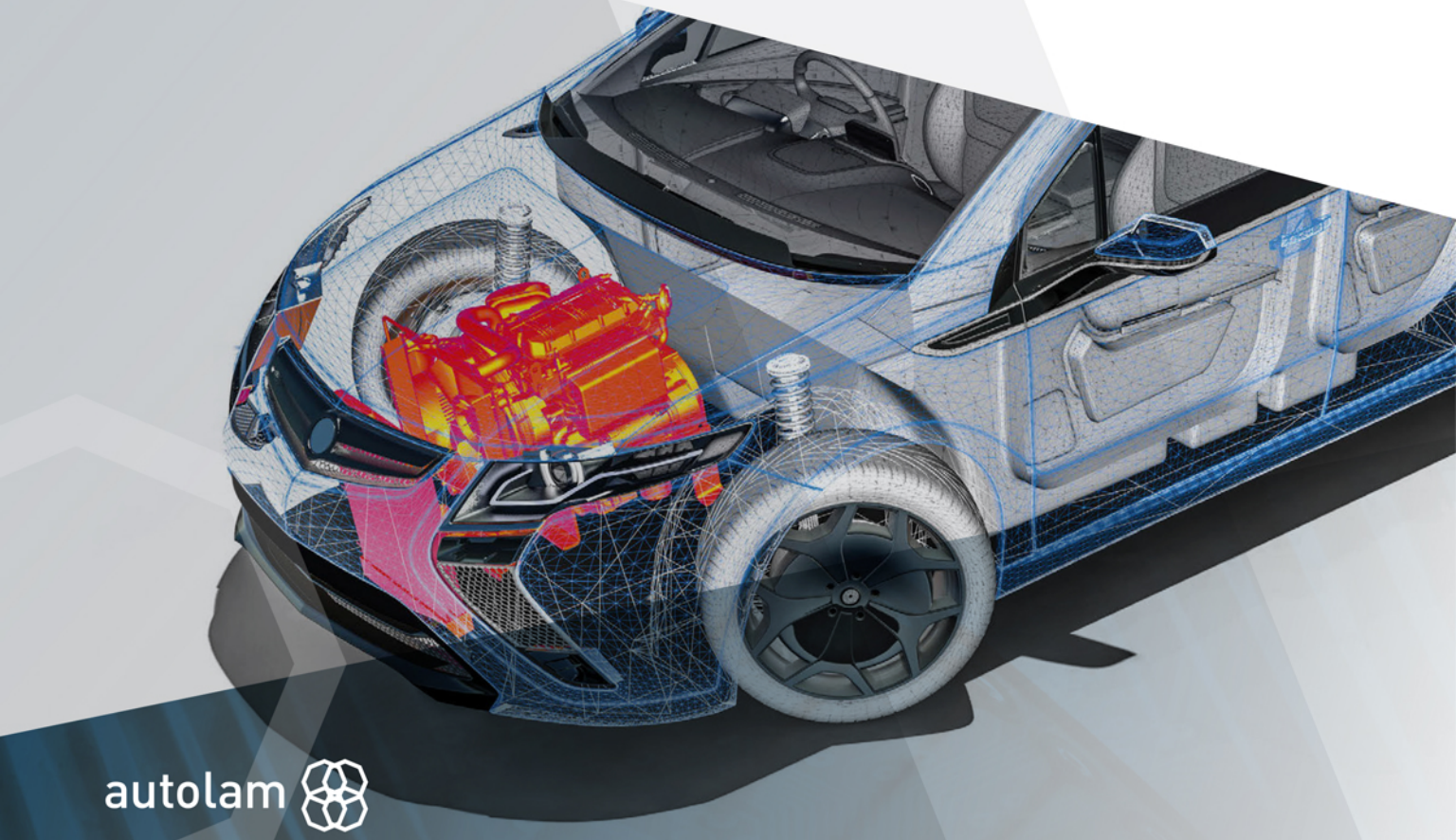

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Simply Speaking

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

During a recent trade show, a group of us were wondering how much money and labor is wasted annually because of PCB designs that are over-constrained or otherwise needlessly complex. It had to be millions of dollars, or maybe even tens of millions.

Like a lot of long-running challenges in PCB design, this issue didn't pop up overnight. It's not like anyone wants to make their designs more complicated than is necessary. As we'll see in this month's issue, this happens for a variety of reasons, such as increasing signal speeds, faster rise and fall times, and shrinking silicon technologies.

If your documentation template is too constrained, but the system has been in place for years, you may have already spent hundreds of thousands of dollars in extra fab costs and wasted labor resources, along with jobs put on hold unnecessarily.

Some designers over-constrain their entire boards when only a handful of features actually require tight tolerances. Every dimension specifically called out is bought and paid for, because it has to be inspected, and that can be an expensive habit.

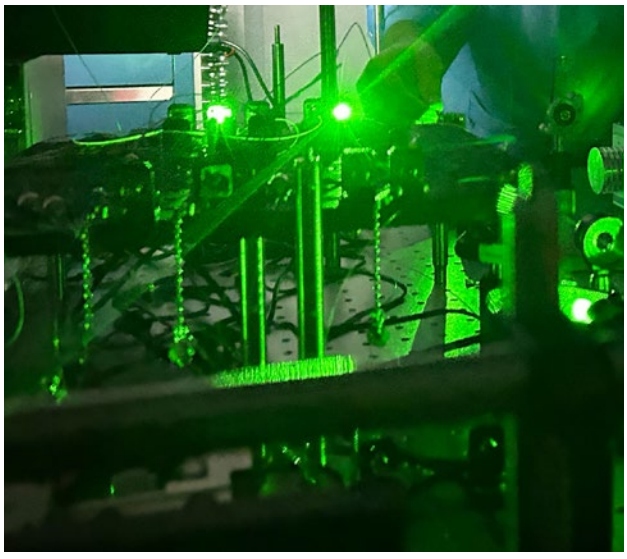
So, in this issue, our expert contributors explain how to design PCBs without making them complex and over-constrained—whatever the level of technology. We also discuss the effect your decisions and tradeoffs have on design complexity, as well as the need to thoroughly understand how electrical and manufacturing limitations can lead to over-constraining your board.

We start off with a conversation with Kris Moyer, who explains why "one size fits all" is not a great plan for setting board constraints. Next, Martyn Gaudion discusses various ways to design the simplest—and best—stackup possible. Doug Brooks and Johannes Adam tell us why thermal vias are usually ineffective at dissipating heat, but do a great job of blocking potential routing channels. Chris Young has a great set of guidelines called "8 Simple Rules for Streamlining Your Design."

Zach Peterson explains why designers should stop designing PCBs like Ferraris, the famously complex Italian supercars. Tim Haag describes why designers should follow the lead of "Star Trek's" Montgomery "Scotty" Scott and keep their designs simple, and Joe Fjelstad points out why the simplest design is usually the best. We also have columns by Matt Stevenson and Barry Olney, and Steve Williams has a conversation with American Standard Circuit's John Johnson on UHDI.

Trade show season is here, and we'll be covering productronica next week. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 23 years. To read past columns, click here.



Processing Quantum Information Reliably

Using laser light, researchers have developed the most robust method currently known to control individual qubits made of the chemical element barium. The ability to reliably control a qubit is an important achievement for realizing future functional quantum computers.

This new method, developed at the University of Waterloo's Institute for Quantum Computing (IQC), uses a small glass waveguide to separate laser beams and focus them four microns apart, about four-hundredths of the width of a single human hair.

The researchers created a waveguide chip that divides a single laser beam into 16 different channels of light. Each channel is then directed into individual optical fibre-based modulators which independently provide agile control over each laser beam's intensity, frequency, and phase. The laser beams are then focused down to their small spacing using a series of optical lenses similar to a telescope. The researchers confirmed each laser beam's focus and control by measuring them with precise camera sensors.

The new waveguide method demonstrates a simple and precise method of control, showing promise for manipulating ions to encode and process quantum data and for implementation in quantum simulation and computing.

(Source: University of Waterloo)

Simplifying Your Design

Feature Interview by the I-Connect007 Editorial Team

It's safe to say that millions of dollars, not to mention man-hours, are wasted each year because of over-constrained, overly complicated PCB designs. Much of this is due to the increase in signal speeds and rise times, even in "mature" PCBs, and the extra cost is already part of the budget.

For this issue on simplifying PCB designs, the I-Connect007 Editorial Team spoke with IPC instructor Kris Moyer about ways that designers can avoid overconstraining their designs and making them needlessly complex. As Kris says, streamlining your design comes down to having a solid understanding of fab and assembly processes and the silicon trade-offs that can simplify or overcomplicate your design, as well as the need to start working with fabricators early in the cycle.

Andy Shaughnessy: What are some typical snafus and missteps that you see designers make to overcomplicate their designs?

Kris Moyer: Here's what often happens: Let's say you have one connector on your board that needs tight tolerance. But rather than dimensioning to just that connector, locally, designers will do a tight tolerance to the data from the global dimensioning system, which now constrains the entire board.

Or, if they need perfect coplanarity on a BGA part for good BGA mounting, they'll put co-planarity back over the entire board where they don't need it, because regular chips, gull-wings, and so on don't need the same amount of coplanarity as a BGA—or they'll try to hold layer tolerances: "I need a 2-mil layer plus or minus 10%," because they know that 10% is

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normal for tolerance, but they missed the part of the spec that says 10% or 1 mil, whichever is greater. Fabricators can't hold that tight a layer-to-layer tolerance when it's below a certain layer thickness.

Below about a 10-mil thickness, the best fabricators can do layer-to-layer is 1 mil for nominal processing. If you want to hold a tighter tolerance, you're paying for 100 to get five boards. That's just a couple of examples. Another is overly tight hole tolerances: "I want to have 150-mil diameter hole plus or minus one mil." Again, it's unreasonable, right?

At several companies where I've worked or consulted, they still have mechanical engineers do the documentation for the boards. So, the board designer designs the board and passes it over to let the ME do the documentation and follow their standard documentation template. But the designers don't realize that a machine shop that's milling a chunk of aluminum can absolutely hold plus or minus 1 or 2 mils of tolerance. There's not a lot of understanding of what the manufacturing capabilities are. They tried to hold the manufacturing nuances that they're used to in mechanical engineering, apply those to board design and board manufacturing, and find themselves overly constrained.

> The solution is to learn the standards and learn the manufacturing processes.

Shaughnessy: How did the MEs end up in this position?

Moyer: If you go back to the early days of CAD tools, the MCAD tools were set up from day one to create good documentation packages. The ECAD tools would output a document, but it didn't have good documentation capabilities like GDT control frames. In early ECAD tools, if you had 3D at all, it was simple extruded rectangles. "Here, put a box on your board where your part is extruded up, so you know what the thickness is." That represented your part, whereas the MEs had full 3D modeling to build very complex, realistic structures, so they can do all of that. A lot of companies just said, "You know what? Just send the board to the ME." They already had a template defined and the ME could do all of these little detailed views and so on.

Shaughnessy: What's the solution here?

Moyer: The solution is to learn the standards and learn the manufacturing processes. Take all the IPC training classes that you can to learn these processing capabilities and where the limitations are. Then the board designer can have intelligent, knowledgeable discussions with the other stakeholders—the EEs, MEs, managers, and so on. You have to be able to say, "I understand where you're coming from. However, this is the manufacturing limitation. If you spec it this way, it's a big cost-adder to the board. But if we document it this way, we will get the same effect that we want, but now we've simplified our board design and constrained it just enough for what we need without overconstraining."

Happy Holden: Andy, I think what's complicating the idea of simplifying your design is that BGAs and other part miniaturization and the shrinking pitch of connections all sneak up on designers. A lot of times, they design the whole board and get everything connected except for the last 5%. Then they run into via starvation, and they're forced to go with laser-drilled blind vias. I can always tell that, if it's a complex board with 127 laser-drilled blind vias, that's a clear indication that the designer never intended this to be an HDI board. He didn't know about the simple models they can use that would have told him ahead of time that the size of the board, the pitch that he's work-

ing with, and the netlist indicates that this will require HDI. Instead of using 127 vias, you should have used 5,000 microvias, because that would have reduced the layer count and everything else. But now, he's all the way through the design, and he's got via starvation.

People mistakenly believe that HDI costs too much. Well, HDI costs too much because designers don't know how to use it, and they've never been properly trained that if you go with blind or buried vias, then you have to start out from the very beginning and use one of the models to indicate how many signal layers you'll need.

Shaughnessy: This sort of thing is in the IPC standards, so familiarity with the standards would definitely go a long way.

Holden: Oh, yes, absolutely. That's why we wrote the first HDI Design Guide, which is not a standard. We included some of the different density modeling equations so that before you ever start, do some of these equations to see whether you will need blind and buried vias. If you think you will do HDI without it, then you will get trapped at the very end of the process, and it will be expensive.

Moyer: I will give you a perfect example. I recently consulted with a company that builds products that go in one direction really, really fast and don't come back. They had designed a coplanar transformer for their board, which was rigid-flex, using their magnetics software. Their magnetics software said that the arc here should be this wide, and you should have this much gap to the next arc, and so on. All was good. They said that to carry this much current, it should be this thick. From a purely theoretical physics point of view, everything they did was correct. What they came up with was a coil transformer design, set to adjacent layers, so you'd have primary and secondary. The traces were 5 mils wide with 4-mil spaces, and they designed it out of three-ounce copper.

Kris Moyer

This was physically impossible to build. With three-ounce copper, you need at least 10 to 15 mils of gap between traces. The narrowest copper feature that most fabricators will touch is about 10 mils, but they prefer about 12 mils with three-ounce copper. The software that the engineers used gave them some numbers and they designed the whole thing, and they could not get a fab shop anywhere in the world to touch this. I told them what they needed to do to change it, but they didn't listen to me, so I stopped consulting with them.

Shaughnessy: So, there are probably hundreds of ways that a board can be made overly complex.

Moyer: The fun thing about a printed circuit board is that you can overconstrain it and overdesign it and it will still work. But my favorite question is, "What's the definition of optimal design?" That's really difficult to answer, because given a bill of material and a schematic, there's an almost infinite number of ways that the board can be physically designed.

On the board side, we tend to be over-constrained and on the assembly side, we tend to be under-constrained, so we need to find a happy medium. One thing I see in assembly is that the board designer does not often consider the mechanical side of the design. Assembly requires access for tools, and so on. Fortunately, IPC standards such as the 6012s cover both fab and assembly, if designers actually read them.

Shaughnessy: I've heard SI engineers half-jokingly say that signals should be as dirty as they can be and still pass margin, because of all the over-constraining going on in high speed.

Moyer: Well, yes. But unfortunately, there is a caveat to that. I agree about designing it just enough to pass margin. The problem is not the board designer; it's the silicon designers who keep shrinking silicon technology and silicon geometry.

Now we have chips coming out with edge rates on the order of 100 picoseconds, or even faster. In order to achieve those kinds of square edges to pass the timing, even my digital traces, I now have frequency content up into the gigahertz range, which is approaching RF geometry. I have to worry about insertion losses, emissivity, and susceptibility and all of these RF-level issues, which never used to be a thing. It's insane, and the board designer has zero control over it.

Shaughnessy: Is there else anything you'd like to add?

Moyer: Number one, learn the IPC standards, whether it's through taking classes or just getting hold of standards and reading them yourself. I teach some of these IPC classes (for a little shameless plug here). Also, talk to your fabricator. Don't be afraid to call your fabricator and have those kinds of technical discussions: "Hey, I've got this challenge on my design. Do you have any suggestions?" Your fab might have some recommendations that you never thought about that could be implemented in a much more cost-effective manner than the way you're thinking about doing. I tell my students that all the time, "Your fabricator is your friend."

Shaughnessy: This has been really good. Thanks for your time, Kris.

Holden: Very interesting, Kris.

Moyer: Always a pleasure, Happy. **DESIGN007**

Q2 Revenue for Top 10 IC Houses Surges by 12.5%

Fueled by an AI-driven inventory stocking frenzy across the supply chain, TrendForce reveals that Q2 revenue for the top 10 global IC design powerhouses soared to US $38.1 billion, marking a 12.5% quarterly increase. In this rising tide, NVIDIA seized the crown, officially dethroning Qualcomm as the world's premier IC design house, while the remainder of the leaderboard remained stable.

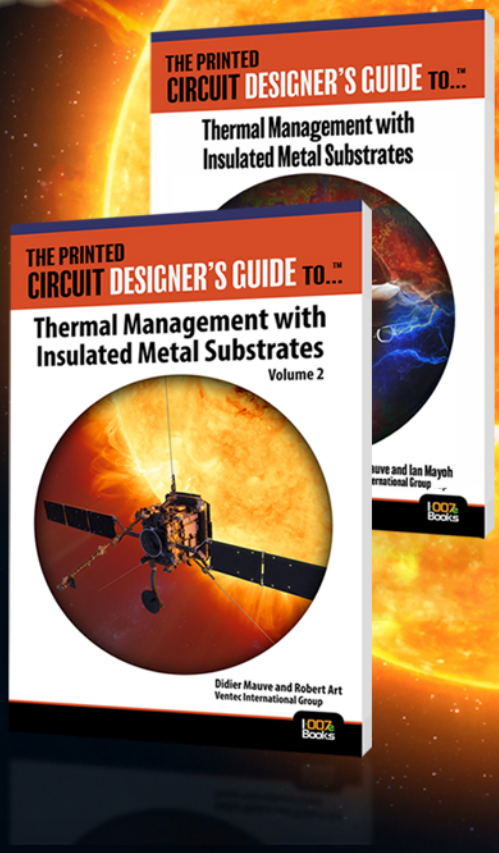
NVIDIA is reaping the rewards of a global transformation. Bolstered by the global demand from CSPs, internet behemoths, and enterprises diving into generative AI and large language models, NVIDIA's data center revenue skyrocketed by a whopping 105%. A deluge of shipments, including the likes of their advanced Hopper and Ampere architecture HGX systems and the high-performing InfinBand, played a pivotal role.

AMD's Q2 performance plateaued at about $5.36 billion, weighed down by a slump in gaming GPU sales and its embedded segment operations. Conversely, MediaTek, after several quarters of inventory recalibration, witnessed a resurgence with components like TV SoCs and Wi-Fi stabilizing.

Peering into Q3, while inventory levels across companies paint a rosier picture than H1, a pervasive end-user demand slump urges caution. However, a silver lining emerges with CSPs, internet titans, and private firms flocking to generative AI and large language models.

(Source: TrendForce)

Companionship at its Best



Look Inside

This sequel to Ventec's book series on Thermal Management describes the applications, IMS products and support services to help you understand and overcome thermal management challenges.

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Simplest Stackups Specified

The Pulse

Feature Column by Martyn Gaudion, POLAR INSTRUMENTS

"Everything should be made as simple as possible, but not simpler." —Albert Einstein

Einstein advocated for describing complex theory in the simplest way possible, but not so simplified that key information is lost. We often see this when the media is criticised for "dumbing down" information. However, from an engineering perspective, if a design can be engineered to perform the required application in a simpler or more economical way, then simplification is truly a valuable goal.

But in the Real World

Often, complex solutions are the only way to realize a design. In these circumstances, the information surrounding a design should be as clear as possible for the people who interact with it during the product's design and lifecycle.

Small Is Beautiful

It's also simpler where signal integrity is concerned. Signal integrity becomes more challenging when interconnects are long in comparison to the rise time or maximum frequency component of the signals you are handling. If you keep your traces short enough, then reflections or impedance mismatch become a non-issue; they still exist but the effects are too small to cause trauma to your signals.

For GHz designs, where loss becomes even more of a concern than reflections, the "keeping it short makes it simple" mantra also holds

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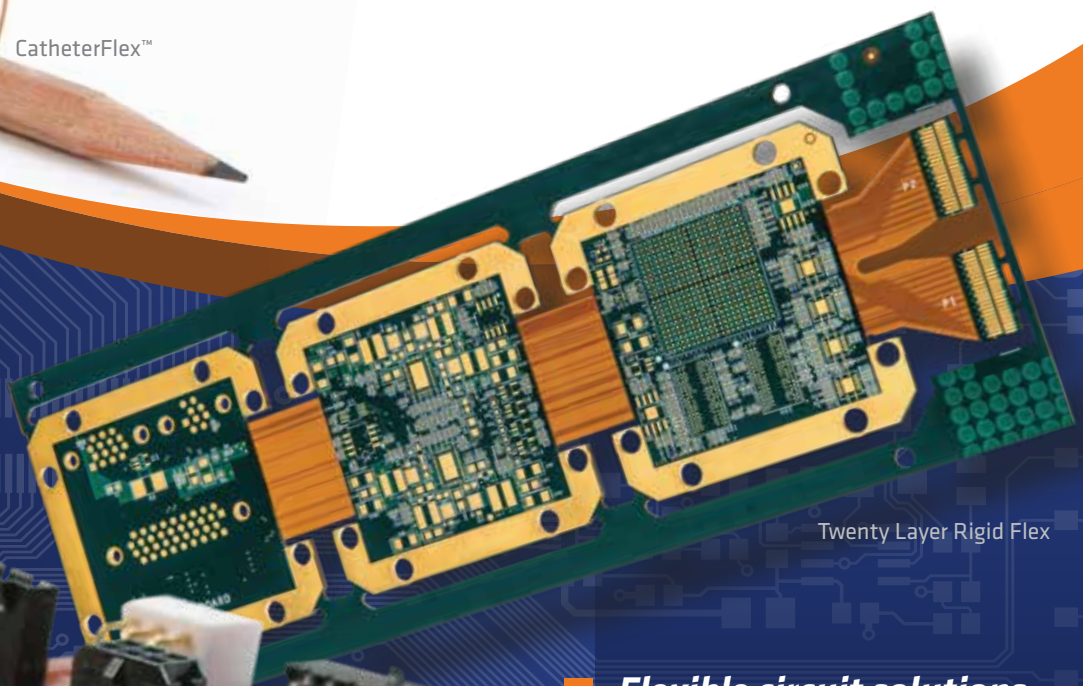

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true. With insertion losses being directly proportional to the line length, then halving your line lengths (where possible) will halve your losses: simple and free. I sometimes see questions about line impedance on very short lines, where the frequency of interest is relatively low, and the interconnect at each end of the line is a significant portion of the length. It pays to check whether impedance or loss is an issue in these circumstances. There is a simple Microsoft Excel tool called a critical trace length calculator, which helps check the critical length.

Whilst on the subject of small or short, moving from the X-Y to the Z-axis, the same is true for vias: Keep them short. If you can't keep them short, keep the stubs short. Let's drill down (sorry) on all the possibilities for minimising the signal integrity challenges of vias. Remember that, in most cases, the vias are short compared with the trace length unless it is a really thick board.

Thinner boards (where possible) have inherently shorter vias. Where the PCB is necessarily thick because of high layer count, there are several approaches:

- Minimise the stub length
- Use microvias
- Back-drill the offending stubs

Why are via stubs a problem? Simply put, it is because a signal arriving as a stub sees it electrically twice as long as it is mechanically. A signal arriving from the top layer of the PCB traversing down the via to a trace on an inner layer can't tell the difference between propagating further down the via (the stub) or continuing along the trace, so it does both—the part propagating along the intended trace continues unimpeded. But the part of the signal that chances to propagate down the stub finds an open circuit at the end of the stub and 100% of that diverted signal will reflect and rejoin the main trace, at which point part of the stub reflection will return toward the source and the rest will rejoin the signal headed toward its intended destination. Using buried vias, backdrilling the stub, or using microvias are all technical solutions to this, but an alternative is to (where possible) route so that the stubs are as short as possible—say, on a 10-layer board route a signal from L3 to L8 rather than L1 to L5, which would leave a far longer stub. Sometimes a rapid check to see whether a feature, such as a stub, is a cause for concern can rapidly put you at ease or flag if more attention is needed. Figures 1, 2, and 3 depict differing stub lengths and their relative impact, from "safe to ignore" (green 28-mil stub) to "do something about it" (red 200-mil stub) when the stubs are in a 4Gbit/s data channel.

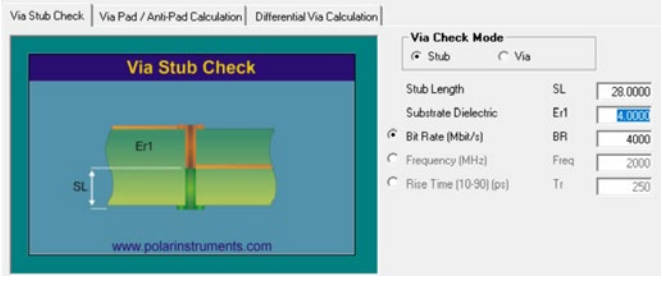

Figure 1: Via length of 28 mils causes no concern at 4 Gbit/s data rate.

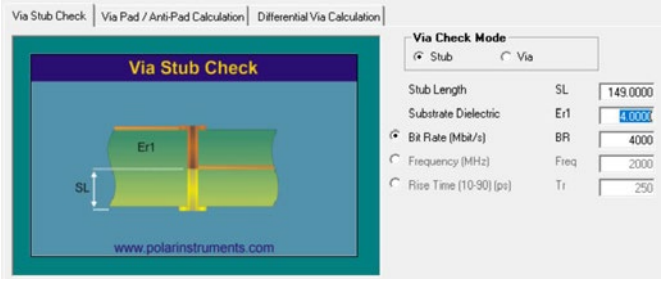

Figure 2: Via length of 149 mils causes some concern at 4 Gbit/s data rate.

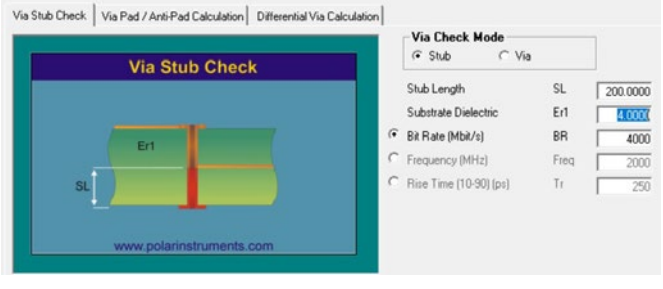

Figure 3: Via length of 200 mils requires attention at 4 Gbit/s data rate. (Find the math behind this in "Signal and Power Integrity Simplified" by Dr. Eric Bogatin)

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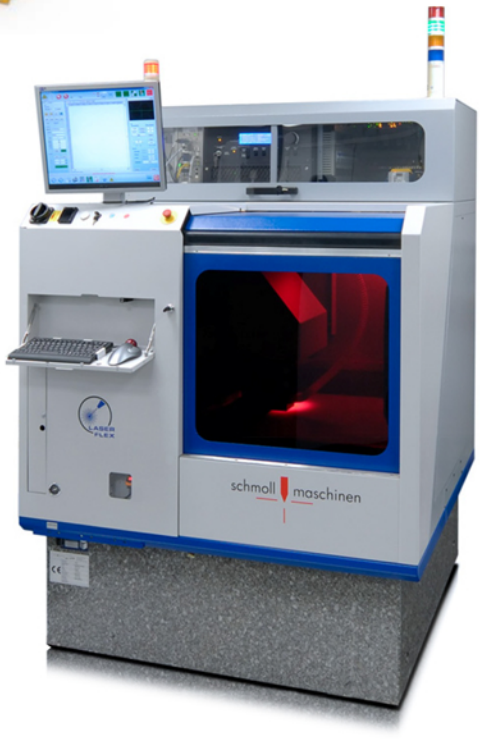

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Modelling Single-ended and Differential Via

Modelling vias is one of the most frequently searched terms driving traffic to the Polar website. One of the counterintuitive points on via modelling is that it is easier to obtain an estimation of a differential via's characteristics than that of a single-ended via. Why? Because differential vias are inherently an out-and-return path, there are no discontinuities in the return path (or at least they are minor) compared with single-ended vias. This is a key advantage for designs with ultra high-speed digital signaling in making them easier to design. While you can model a single-ended via with a 3D solver, it only goes to prove the design is compromised. To get the best signal integrity for a single-ended via, it can be necessary to place it next to a ground via which spans all the intermediate planes. Plane pairs to single-ended vias act as slot antennae and cause reflections out and back to the edge of the board. Transitioning a signal from L1 to L3 with a ground on L2 would minimize this, but at same time, you have to check that the stub is still short enough not to be troublesome.

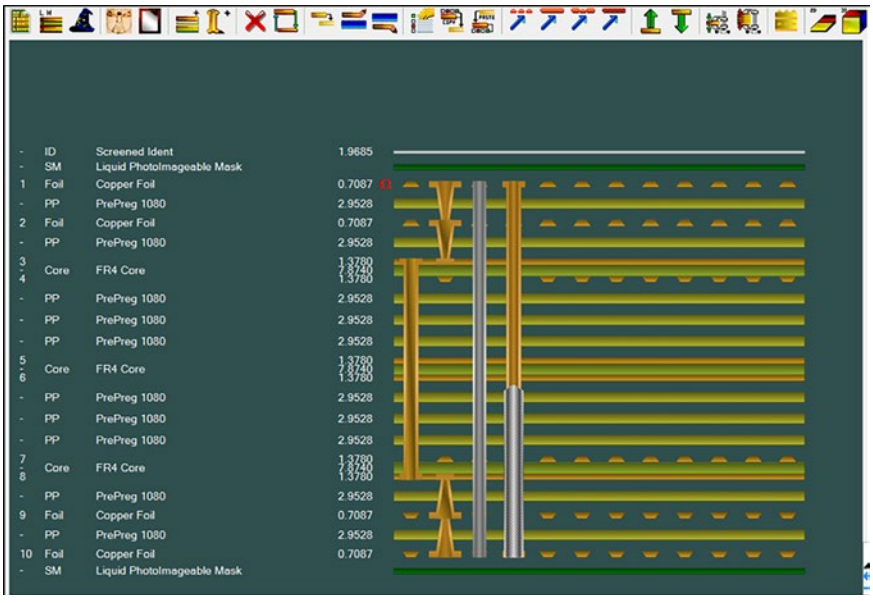

Figure 5: Stackup with microvia/back-drilled vias and buried vias. (Source: Polar Speedstack)

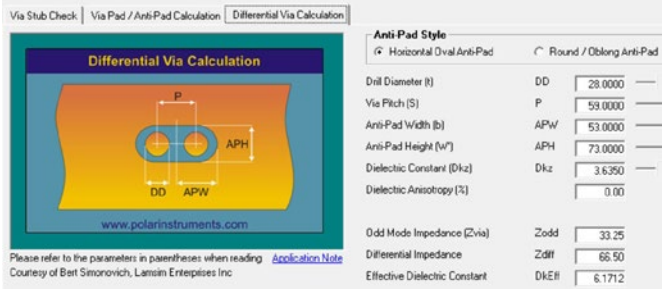

Figure 4: Differential via property calculation, Polar Si9000e. (Courtesy: Bert Simonovich Lamsim Enterprises)

Communication

Once your stackup design is completed, then ensure it is documented and make it clear to your fabricator, broker, or shop floor that you are a PCB apps engineer so that drills/back-drills, layer separation, and any transmission lines are clearly identified and associated with the relevant net classes.

Conclusion

Keeping high speed line length as short as possible, stubs short, and careful attention to via interconnects can ease your signal integrity challenges at minimum cost. Use simple tools to flag areas where more detailed modelling or more advanced materials may prove necessary and remember that in most cases engineering is about delivering to your employer and customer the most appropriate solution for the specific application at the lowest cost. Find more information about signal integrity on our website and YouTube channel. **DESIGN007**

Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns, click here. Martyn is the author of *The Printed Circuit Designer's Guide to… Secrets of High-Speed PCBs, Parts 1 and 2.*

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Your Thermal Designs Are Inefficient

Feature Article by Douglas Brooks
and Dr. Johannes Adam

Your thermal designs are (probably) inefficient. The inefficiencies are unnecessarily taking up board area and blocking routing channels. This is likely true in at least three areas:

1. Your high-current-carrying traces are probably too wide.
2. You probably use too many vias in your high-current-carrying traces.
3. Any thermal vias you use are (almost) worthless.

Trace Width

Most designers rely on the trace widths suggested in IPC-2152[1], the "bible" for calculating high-current trace widths (unless you have read our book[2]). IPC-2152 is the best, most thoroughly researched study of trace currents and temperatures available. But it does have some weaknesses. One weakness is that it (by necessity) studies 6-inch-long traces in isolation. But traces are not all 6-inches long nor in isolation. There are nearby design and material parameters that impact trace temperatures, most of them in a downward direction[3]. Perhaps the most important parameter lowering trace temperature is the presence of a plane underlying the trace. Most boards nowadays have such a plane.

Figure 1 shows the impact a plane can have on trace temperature. It is a simulation[4] of two 1-ounce traces carrying 14 amps each; the top one is 120 mils wide, the bottom one is 200 mils wide. The board is normal FR-4 mate-

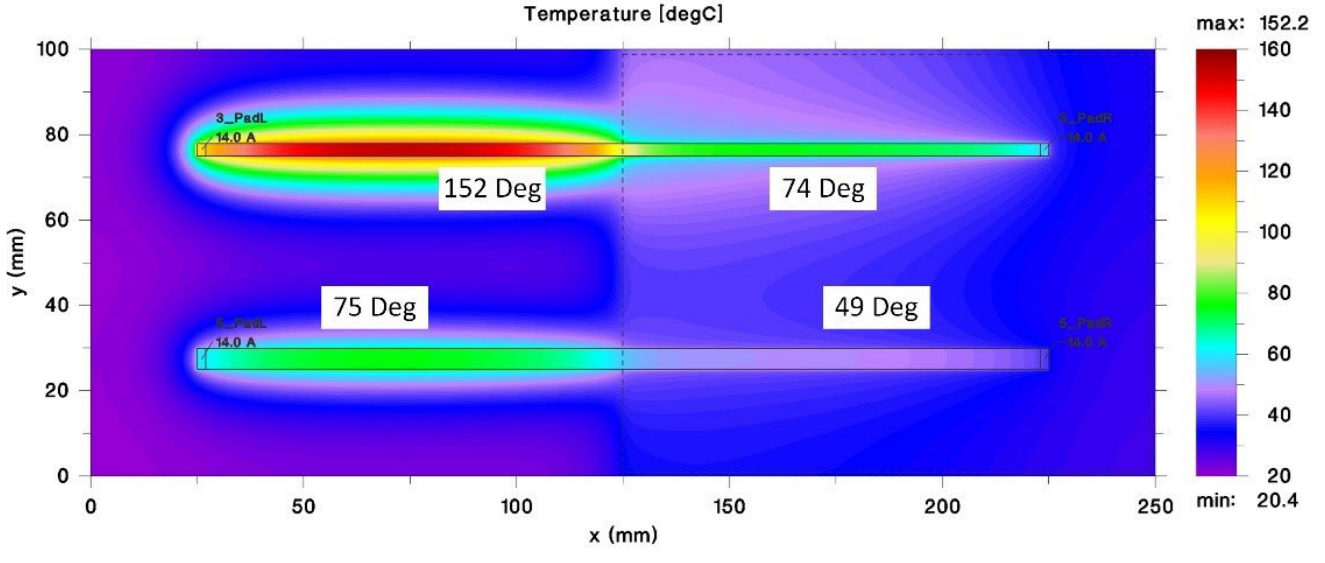

Figure 1: Planar impact on trace temperatures.

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rial, 10" x 4", with a full plane on the bottom layer of the right-hand half of the board. The 200-mil 1-ounce trace carrying 14 amps rises to about 75°C, consistent with what we would find in the IPC tables. The temperature lowers to about 49°C over the plane. But the *smaller* 120-mil-wide trace is the same temperature (at 14 amps) over the plane as the 200-mil-wide trace is without the plane. The presence of the plane drops the temperature by roughly 50% (a result that is very situation specific).

Now, if your trace temperature specification is 75°C and you use the usual (IPC) method for determining trace size, you would design with a trace width of about 200 mils. But if you know there is a plane under the trace (or even just part of the trace), you can reduce the trace width (in this case by about 40%), opening up some additional board area for additional routing.

Vias

Even a large trace carrying a high current often only needs a single small via to connect to another trace segment. The specific example we simulated and experimented with was the comparison of a 27-mil trace carrying 4.75 amps and a 200-mil-wide trace carrying 8.55 amps, each using a single 10-mil diameter, one-ounce plated via[5]. The 27-mil-wide trace via rose to a temperature of 70° while the 200-mil-wide trace via only rose to a temperature of 48°C, even though it was carrying almost twice the current[5].

Figure 2 shows the result of another simulation[6]. This is of a 120 mm x 16 mm (4.7" x 0.65"), 1.55-mm (60-mil) thick board with a pair of 5-mm (200-mil) wide traces carrying 14 amps. The traces are connected with 10-mil 1-ounce plated vias. Conventional wisdom is that we should use as many vias as necessary

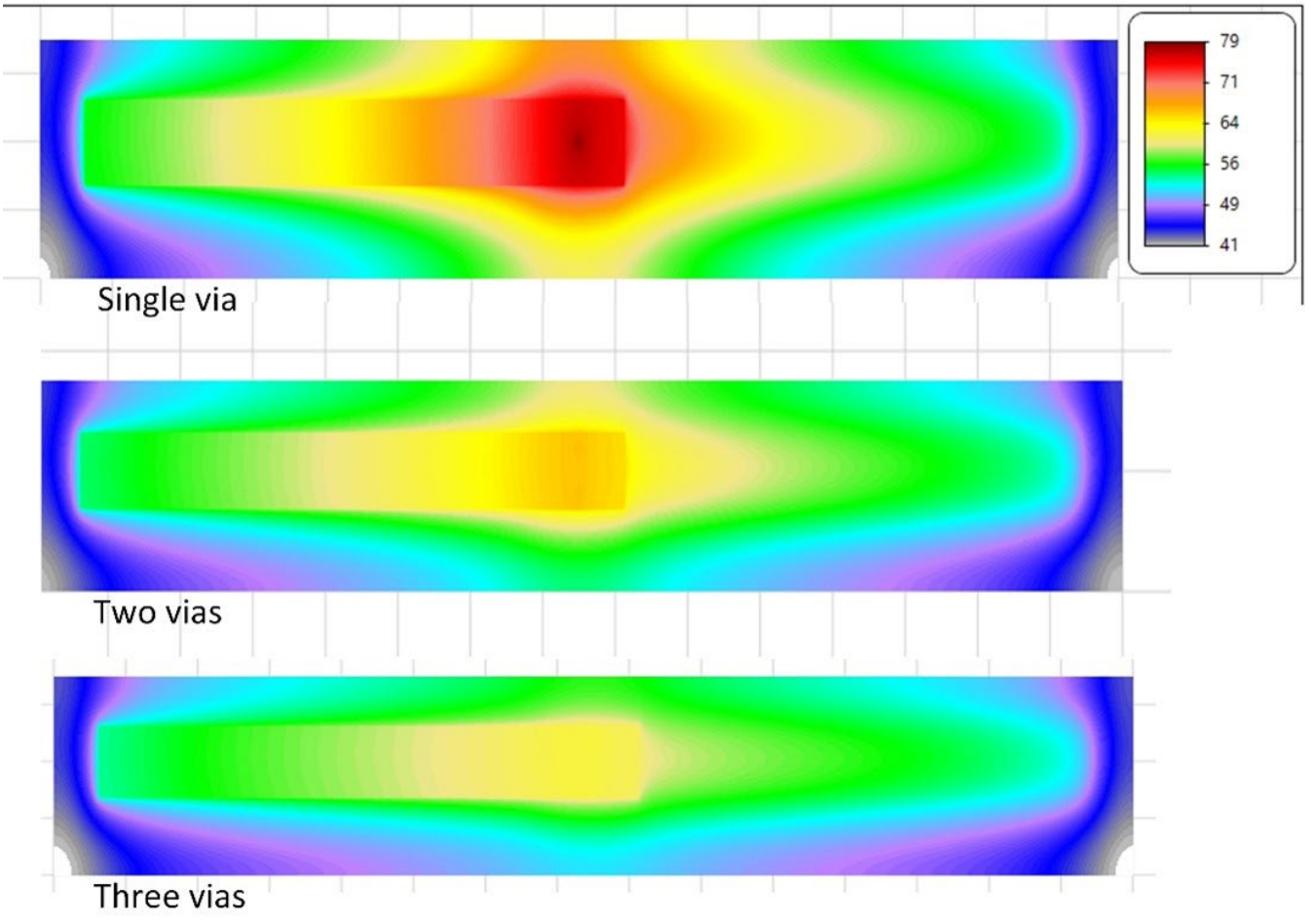


Figure 2: Adding vias lowers temperature to a point.

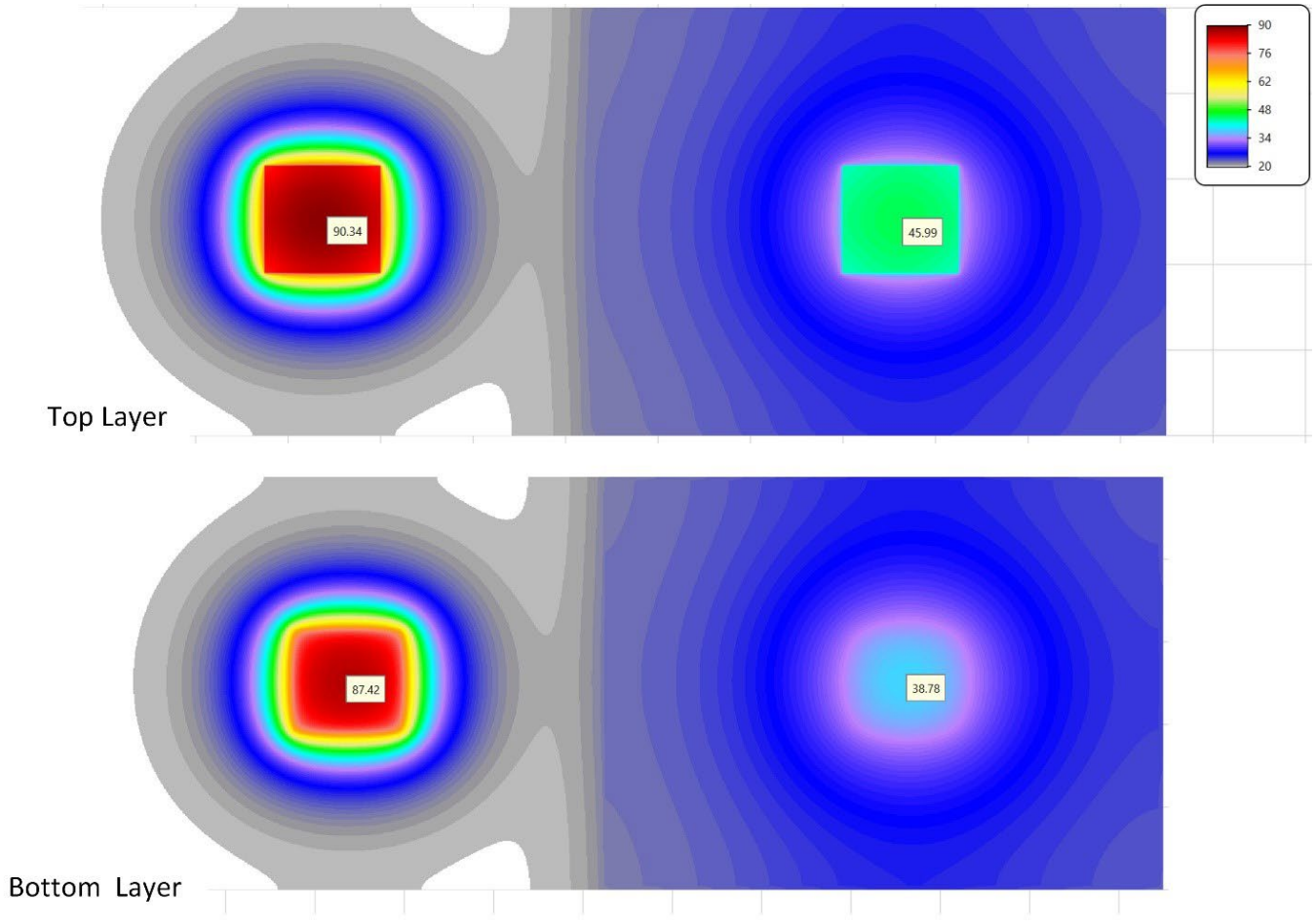


Figure 3: Heated pads, top and bottom layers.

for the total conducting cross-sectional area of the vias to equal the trace's conducting cross-sectional area. In this example, that would mean 14 vias.

The top image shows the results for a single via, the middle image for a pair of vias, and the bottom image for three vias. The trace itself (without any vias) heats to about 56°C. The single via results in a via temperature of approximately 80°C, 24°C above the board temperature. This might be tolerable in some consumer applications. The use of two vias lowers each via temperature to about 67°C, 11°C above the board. Three vias results in individual via temperatures of about 62°C, only ~6°C warmer than the trace temperature itself. Adding 11 more vias only gains us about 6°C in temperature closure but locks up quite a few more routing channels.

Bottom line: We don't need nearly as many vias as our common (mis)understanding would have us believe.

Rules of Thumb

Unfortunately, these illustrations are all case-specific. That is, there are no general rules of thumb that reliably flow from them. The only way to determine with any precision what gains can be made, and where, is with thermal simulations using good thermal simulators.

Thermal Vias

Figure 3 shows a simulation using the same board as in Figure 1, but with two one-inch square heated pads instead of traces. The pad on the right is over a plane on the bottom layer. Each pad is heated by a two-watt source.

The top-layer pad on the left heats to about 90°C, while the plane on the right lowers the temperature of the top-layer right-hand pad to about 46°C.

Now suppose we have the opposite situation and want to lower the pad temperature. One might think this was an application where thermal vias might be used. But thermal vias have to go somewhere, typically a plane (or at least another pad) on a lower layer, and here there is no such resource. So, thermal vias are not an option. But since there is a plane under the right-hand pad, thermal vias are an option there.

But here is the problem. Figure 3 also shows the thermal pattern on the bottom layer. What most of us fail to realize is that the thermal profile of a bottom layer of a board looks a lot like the thermal profile on the top layer. That is because the boards are typically very thin (compared to other dimensions). In this simulation the bottom board area under the top left pad is only about 3°C cooler than the pad on the top layer. The board area under the right-hand pad, even though this layer is a solid copper plane, is only about 7°C cooler than the pad on the top layer. This is typical of most boards.

So, any thermal vias we drop from the top pad to the bottom plane will be mostly ineffective because the temperature difference between them is already so small. The addition of the plane has already lowered the pad temperature as much as practical.

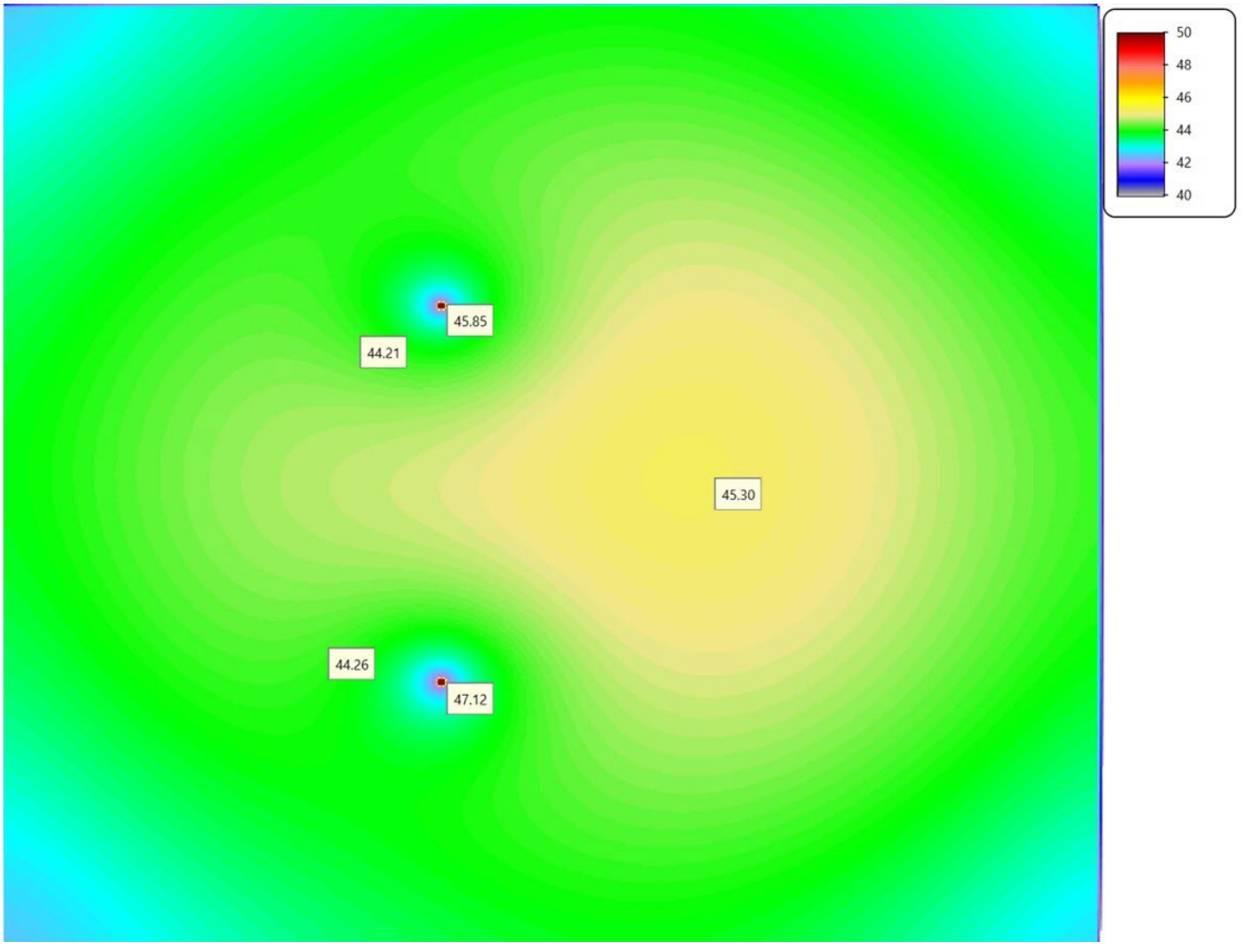


Figure 4: Thermal profile of top pad with two thermal vias.

But that's not all. Figure 4 shows a simulation where we have placed two thermal vias under the right-hand pad. The thermal vias are 20 mils in diameter and plated to almost 3 ounces. The thermal vias are relatively large so that we can see the results in the figure. Even so, we have to zoom in optically and narrow the temperature range in order to visualize those results.

As seen in Figure 4, the pad is hotter in the center than it is around the edges. This is because the edges of a pad or trace cool more efficiently than does the midpoint. Heat can conduct away from the midpoint primarily only in the vertical (Z-axis) direction. But heat around the edges can conduct away both vertically and horizontally. All normal pads, and all traces are cooler at the edges than they are at their midpoint.

But more importantly, the thermal vias only have a small impact, and they have that only at a point[7].

1. Each thermal via only changes the temperature by less than two degrees.
2. And they do so at only a very small area around the via.

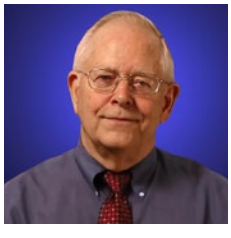
That is why almost every article that discusses thermal vias recommends using a lot of them. But even if you covered the entire pad with thermal vias, the temperature still would not change by much; the gain has already been achieved with the underlying plane. The only thing thermal vias do is use up a lot of routing channels.

Summary

By learning more about how PCB design decisions impact thermal temperatures around the board, we discover there are several areas where we can make significant impacts in design efficiencies. DESIGN007

References

1. IPC-2152, *Standard for Determining Current Carrying Capacity in Printed Circuit Board Design,* IPC, August 2009, page 26.
2. *PCB Design Guide to Via and Trace Currents and Temperatures,* by Douglas Brooks and Johannes Adam, Artech House, 2021.
3. We talk about temperature sensitivities in Chapter 7 of our book referenced in No. 2.
4. We used a simulation program called thermal risk management (TRM), which was originally conceived and designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating, as well as various components and their own contributions to heat generation.
5. See Section 8.4 of our book referenced in No. 2.
6. The maximum "pixel" resolution and density in a simulation is determined by the smallest dimension in the X-Y plane. Via simulations require about one to two orders of magnitude greater resolution than "standard" trace simulations, placing a significantly greater load on the computer CPU and memory. For this reason, modeled board areas for via simulations are typically quite a bit smaller than would be the case for regular trace simulations. This results in a slight upwards bias in model temperatures from what might be otherwise expected. *Relative* temperatures within the model, however, exhibit much smaller upward biases.
7. Temperature is a "point" concept. That is, it varies from point-to-point around a board or trace. So, too, are resistance, resistivity, thickness, and sometimes even thermal conductivity coefficients. We discuss this in numerous places in our book, and especially in Chapter 13, "Do Traces Heat Uniformly?"



Douglas Brooks, PhD, is a veteran signal integrity instructor and the founder of UltraCAD Design in Issaquah, Washington.

Dr. Johannes Adam is a thermodynamics physicist and founder of ADAM Research.

MilAero007 Highlights

CACI Successfully Completes Optical Communications Terminal Interoperability Testing for Space Development Agency's Transport Layer ▸

CACI International Inc announced that it successfully completed Optical Communication Terminal (OCT) Interoperability Testing (OIT) of its CrossBeam® OCT for the Space Development Agency's (SDA) Tranche 1 data relay and tracking network. As part of this testing, CACI was the first SDA-compliant terminal to successfully establish a consistent data communication link with the reference modem.

Amitron Becomes MIL-SPEC Certified ▸

Amitron, a leading U.S.-based manufacturer of printed circuit boards (PCB), brings an additional 80,000 square feet of manufacturing space into the overall MIL-SPEC ecosystem with high automation, and the latest equipment technology and processes for military and aerospace applications.

Historic Wind Tunnel Facility Testing NASA's Mars Ascent Vehicle Rocket ▸

The MAV (Mars Ascent Vehicle) team recently completed wind tunnel testing at NASA's Marshall Space Flight Center in a facility that has been a critical part of NASA missions going all the way back to the Apollo program.

U.S. Army Awards Comtech $48.6M for Next Generation EDIM SATCOM Solutions ▸

Comtech announced the company was recently awarded a $48.6 million contract to deliver Enterprise Digital Intermediate Frequency Multi-Carrier (EDIM) modems in support of U.S. Army satellite communications (SATCOM) digitization and modernization programs.

Lockheed Martin Conducts First Flight In U-2 Avionics Tech Refresh ▸

Lockheed Martin Skunk Works, in partnership with the U.S. Air Force, completed the first flight of the U-2 Dragon Lady's Avionics Tech Refresh (ATR) program. During this mission the aircraft successfully performed a low-altitude functional check flight to integrate new avionics, cabling and software.

Airbus Unveils PioneerLab as its New Twin-engine Flying Laboratory ▸

During the German National Aviation Conference in Hamburg, Airbus Helicopters unveiled the PioneerLab, its new twin-engine technology demonstrator based on the H145 platform. It complements Airbus' range of FlightLabs and focuses on testing technologies that reduce helicopter emissions, increase autonomy, and integrate bio-based materials.

Northrop Grumman to Develop New Guided Ammunition for U.S. Navy ▸

The U.S. Navy has awarded Northrop Grumman Corporation a development contract for the company's newly designed 57mm guided high explosive ammunition. Designated for use with the Mk110 Naval Gun Mount, the company will test and mature the munition for qualification. The 57mm guided high explosive ammunition has the unique ability to continuously maneuver in-flight as it moves toward a designated target.

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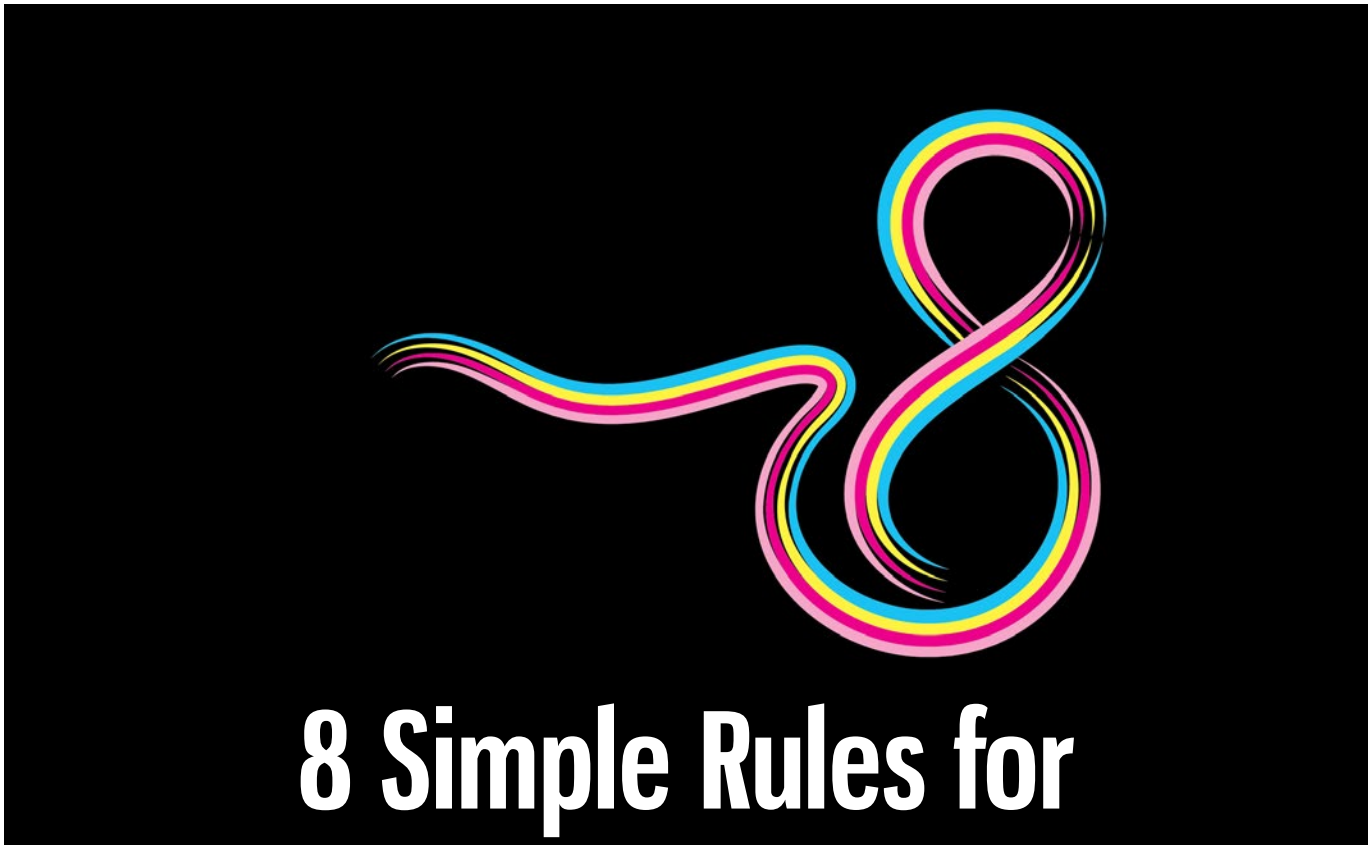

8 Simple Rules for Streamlining Your Design

Feature Article by Chris Young
YOUNG ENGINEERING SERVICES

There are many ways, dozens to be sure, and most likely many more, to streamline a PCB design. My goal here is to pick a single-digit number of rules to abide by, that can be reasonably adhered to, and provide some bang for the buck. These rules are meant to reduce design scope creep, avoid PCB respins, and improve production yields.

One

Communicate clearly

Use explicit communication when addressing ambiguous items. Test point placement can seem like an ambiguous task. Statements like, "Find room for test points," do not help to define scope or draw boundaries. Instead, try statements like, "Production test points can only be on a single side of the PCB in order to reduce test fixture complexity." Implicit communication should be reserved for well-defined objectives and processes. An example would be instructing a PCB designer to place test points per the design procedures identified by company policy X, paragraph Y.

Two

Proceed with a common goal in mind

Designing on the fly without a mutually agreed upon set of goals is a catalyst for scope creep and technical debt. A design blitz, as in football, is a defensive high-risk maneuver intended to reduce schedule (offensive) pres-

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sure. Instead, take the time needed to establish a well-defined and measurable set of design goals. Include the project stakeholders, get buy in, and then execute.

Three

Design your PCB power delivery system (PDS)

Your PCB power delivery system (power planes/structures) should be based on your power distribution requirements and not a coincidence of layout. This means that your PDS design should take place before settling on a board stackup. A typical PDS is composed of discrete capacitors, power plane capacitance, and on-chip capacitance. Determining the amount of plane capacitance needed for a specific design should involve the use of a simulator such as HyperLynx, ADS, or HFSS. Designing an appropriate PDS for your board design is easy to say, much harder to do, and very much worth your time. Improper or poorly implemented PDS designs are nearly impossible to recover from without a costly board respin.

Four

Know your drill holes

A PCB can play host to many types of drill holes for various reasons. A few examples are vias, mounting holes, tooling holes, and press fit holes. Vias come in many forms, but they tend to be some type of plated hole that is typically used for signal, ground, or power transitions from one PCB layer to another. Vias can also be used for thermal conduction between PCB layers. It is important to understand that mechanical engineers typically regard mounting and tooling holes as two very different types of holes that serve entirely different purposes. Mounting holes can be plated or non-plated and provide a clearance/loose fit for the PCB so that it may be attached to some other structure. Tooling holes are designed and manufactured to a tight tolerance so they can provide a transition fit needed for precise alignment of a PCB in an assembly or test fixture. PCBs use interference fit holes for press fit connectors. The connector/PCB mating pins interfere slightly with the holes on the PCB, requiring force to be applied to the connector during the mating process instead of soldering the pins to the PCB itself. Knowing the types of drill holes used on your PCB and their purposes allows designers to effectively communicate their purposes to other stakeholders in a project.

Five

Coordinate your design with your fabricator

The last thing you want to hear from a PCB fabricator is that they are no-bidding your design because it is not compatible with their capabilities. It is perfectly reasonable to include your PCB fabricator in your design reviews. Making sure that your design fits within the manufacturing capabilities of your fabricator is a primary objective, not an "on the side" project. Furthermore, your PCBs built for production should be well within fabricator's range of capabilities and should not be pushing their edges so that your yields (major PCB cost driver) are not driven by process variations.

Six

Consult with the group or company assembling your boards

It is best to know what practical limitations your assembly process imposes on your design instead of finding out post assembly. Not all pick-and-place machines are created equal. Accuracy of small component placement can vary greatly between different pick-and-place machines. Manually removing assembled boards from panels can damage shock-sensitive components. The risks associated with

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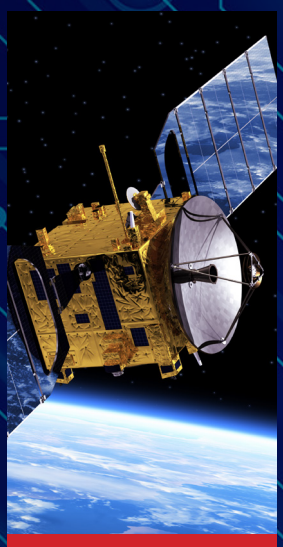
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whoever may be assembling your boards can be mitigated by simply involving them in your design review process.

Seven

Document your component library process

A well-documented CAD library process reduces the chances of errors when creating parts. Part requests should include the part number, manufacturer, part description, datasheet(s), priority level, need date, package type, part type, and any descriptive information or notes for symbol or footprint creation. The part that is created to fulfill the request should be documented and linked to the request. The part should then be reviewed and documented as either meeting the request or as needing to be reworked. The documentation could take the form of a spreadsheet, database, or even a physical paper trail. The intent is to explicitly communicate what parts need to be created and how.

Eight

Test point placement is critical

PCB test points serve to support design and production. Circuit designers will use test points to assist in integration and verify functionality. Test points are typically used in production to load software/firmware and verify proper PCB assembly. Production using test points should take precedence over design and engineering test points. Test point locations directly impact the complexity of test fixture design, so strive to place them on only one side of the PCB. Do not place components on the opposite side of a PCB underneath a test point. This provides space on the PCB to apply an opposing force to reduce stress and strain on the board assembly when test points are engaged during test. Don't find space for test points. Make space by performing test point placement alongside component placement. **DESIGN007**

Resources

1. "Power Delivery System Design," by Lee Ritchey, Altium.

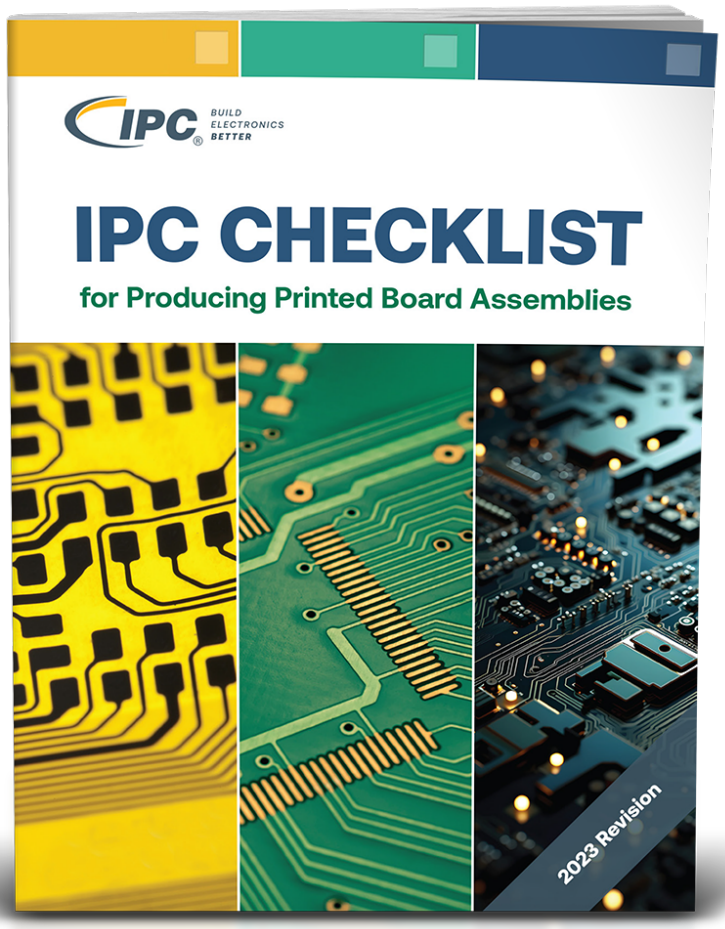
2. Simulators – Keysight ADS, Siemens EDA HyperLynx, Ansys HFSS.

Chris Young is founder and president of Young Engineering Services.

Anatomy of IPC Checklist

Typical PCB production cycle, from design through end product

Complete list of current IPC reference standards



Cross-sectional view of plated through-hole issues

Step-by-step operations for design, fabrication, and assembly

Avoid the 'Ferrari Problem' and Simplify Your PCB Design

Feature Article by Zach Peterson
NWES

When I last spoke with DirectPCB cofounder Greg Papandrew, he mentioned that many boards are designed like Ferraris when what the product really needs is a Ford Pinto. Those of us who work in PCB design education, whether on corporate training or on the conference scene, tend to teach new designers how to build Ferraris. What we sometimes don't do so well is teach new designers how to identify whether a Pinto will get you safely to your destination.

So, if you need to take your Ferrari and convert it to a simpler version, how can you do it without losing your form and function? Better yet, how can you avoid the Ferrari problem altogether?

The operative word "simpler" could mean many things, and a designer's job in this area is to identify the "things" that create the most value in a design. This could be electrical performance, mechanical reliability, requirements to support a specific component type (e.g., fine-pitch BGA), or something else entirely.

1. IDENTIFY THE COST DRIVERS

Any PCB that could be reasonably termed "more advanced" is more complex and thus tends to cost more. There are several factors

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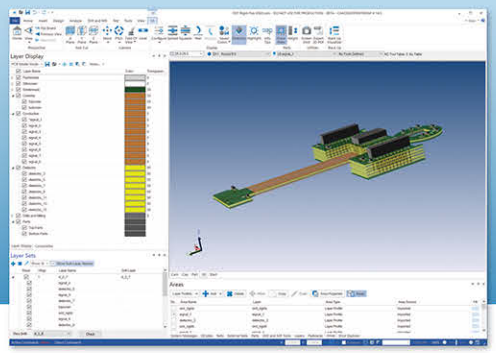

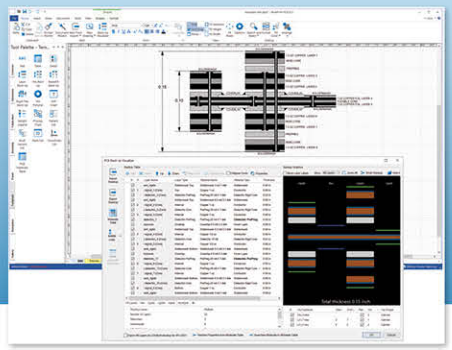

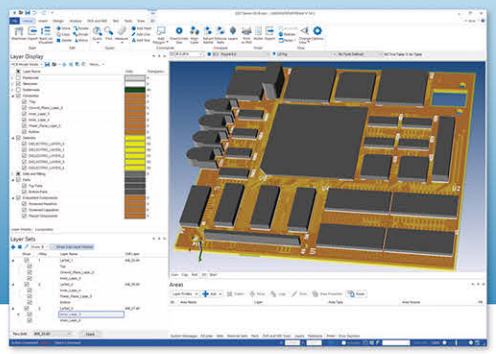

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that can drive this, which are listed in approximate order of importance:

- Type of laminate material (PTFE, advanced FR-4, etc.)
- Etch and drill feature size and processing
- Layer thickness and layer count, especially HDI build-up layer count
- High BGA/QFN count
- Expensive surface finishes
- Specialized requirements like heavy copper

Here, the key is to identify the absolute necessities that are required for your device to function to its basic specifications. There are design choices I make out of force of habit, and I have to go back and check myself based on realistic operating requirements. Keep in mind a few simple questions here:

- Do you really need a PTFE laminate in your design, or did you use it because you read somewhere that all RF boards need PTFE?
- Do you really need blind and buried vias everywhere, or can your placement and routing handle larger mechanically drilled vias?
- Is there an SI or density reason I need sub-5 mil trace widths with controlled impedance?
- Does every stub need back-drilling?

Not everyone needs heavy copper PTFE with blind/buried stacked vias and 3-mil line/spacing. Focus on what's important and save yourself and your wallet a lot of headache. Simple steps like changes to your stackup, process limits, and material selection can create big cost savings, both in prototyping and volume production.

2. A LITTLE BOARD COMPLEXITY IS OKAY

This might seem like it contradicts No. 1, but I don't think this is the case. Complexity is about give and take: You add in a bit of complexity in one area, but it makes your life much easier in another area. Think blind and buried vias on a fine-pitch component: your design might work fine with neck-down routing and mechanical drilling at 6 mils, even if the conventional wisdom demands fine-line routing with stacked microvias just because your design looks like it might be HDI.

As an instructor, I've noticed that some new designers tend to think that anything over two layers is a bad design, or that the sudden addition of two internal ground planes will drop a nuclear bomb on board fabrication budgets. They end up spending a ton of time on perfect placement to minimize ghost wire crossings, and then much more time trying to route things with minimal coupling or overlap.

The reality is that four-layer boards are not advanced anymore. A board with two interior stitched ground planes is really an entry-level board, and I certainly would not call these stackups "complex." They also make routing on the top and bottom surfaces much easier, as you no longer have to worry about interlayer coupling. Then there are the EMI and SI benefits; many of the most basic SI and EMI problems can be suppressed or prevented just by using the right stackup. So, if you're new to design, give yourself permission to add a couple ground planes; your EMC testing results will thank you later.

3. OVER-SPECIFYING AND OVER-CONSTRAINING

Over-constraining a design can back designers into a corner, to the point where they over-specify every net in their design rules. The corollary to this is in routing, where some EMI-worthy design features are implemented regardless of need, and they must be handled manually.

Something I've seen that is related to No. 2 is in mixed-signal design. One of the big instances where I see designers create more

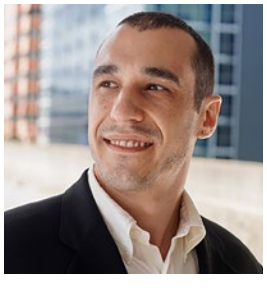
work for themselves is in this realm, where the most common design mistake is to create split grounds or split planes, then try to link them back together with a ferrite, capacitor, or some other EMI-inducing craziness. Even if you applied isolation correctly, it creates new routing and placement constraints that can't always be clearly defined in some CAD systems.

Another common instance here is a stitching via near a signal via. It is true that stitching vias are needed when changing layers or references, but do you really need to painstakingly add this manually to every signal via? Find the main single-ended signals that really need it, such as your SPI bus. Noise margins on your configuration lines are very often large enough that you don't need to throw a stitching via on these. Think about the context of the rule; don't just follow it blindly.

Keep it Simple, Save the Headache

The trick to stepping up your design game is not about knowing advanced design techniques but knowing when to implement them. I've met some designers who are decades my senior but still fall victim to this mistake. Those of us who educate designers have to take a bit of responsibility for this. It's our job to provide context for these rules so our peers can avoid the Ferrari problem.

When you do find that you need your design techniques, learn to leverage your tools for these engineering problems. Higher-end CAD programs have the automation tools needed to create more advanced design constraints. Take time to learn these techniques and you will set yourself up for success. **DESIGN007**



Zach Peterson is the founder of Northwest Engineering Solutions as well as a PCB design instructor and podcast host.

Brandy Tharp: A Passion for Helping Others

Eleven-year-old girls hold many interests, from sports and playing games, to learning how to make more complex decisions and finding commonalties with friends and loved ones.

While Brandy Tharp may have been doing all those things at that age, she was also learning a new skill that most of her friends probably weren't—how to solder. It lit a fire in this young girl who enjoyed math, helping others, and finding ways to harness her energy.

"My mom taught me how to solder on rechargeable battery units that she built," says Brandy, director of education at IPC. "It was something I grew up with. Everybody kind of fell into some facet of the field."

When she started college, Brandy also worked for a telecommunications equipment manufacturer doing hand insertion manual assembly, then learning how to run a wave solder machine because she could work a weekend shift.

"But I'm not the kind of person who can sit still," she says. "I like to know a little bit about everything." Because the company was short on operators, Brandy learned how to program and run more lines and equipment, working her way through each department. That led to a position in the training department and launched a career in training and certification.

Continue reading in *IPC Community*.

Best Practices for Ensuring PCB Design Manufacturability

Connect the Dots

by **Matt Stevenson,** SUNSTONE CIRCUITS

It makes sense to optimize your board using design for manufacturability (DFM) techniques, but applying DFM best practices can be confusing without formal training. The results are designs that are often incomplete, poorly designed, or too complex.

When these issues arise, your PCB manufacturing partner rejecting the design can be considered a best-case scenario because it means they have your back. If your design is simply dropped into an automated queue without concern for manufacturability, the output can be a batch of unusable boards.

Expensive mistakes can be avoided by adopting practices that encourage design for manufacturability. In addition, carefully choosing a manufacturing partner and service level that align with your needs will help you achieve a quality result.

Let us examine some design best practices that will help reduce costs, increase yield, and improve manufacturability.

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Study the Rulebook

It is up to you to be familiar with the design rules. Not every manufacturer prioritizes making DFM rule sets for popular design tools available, cost-effective, and current. Working with a manufacturer who does make rules available will save time and money.

Of course, using design rule checks (DRC) alone will not guarantee manufacturability, but performing them is a great way to ensure that you have created as close to an error-free design as possible.

Remember that error-free is an unattainable point on the horizon you can almost see, but never quite catch. The goal should be a design that lowers the risk of defects and can then be manufactured and assembled. The DRC will help you identify conflicts, such as issues with insufficient clearances between electrical conductors, that will affect electrical functions and create potential manufacturability issues.

Always Review Your Design

We strongly encourage you to always review your design. Take a second look for issues such as insufficient power trace widths, blind vias, and components that are laid out too close together. When a design pushes the manufacturer's tolerances, it is easy to accidentally cut holes or route slots too close to pads or traces.

Copper thickness is another important design consideration. Higher current may require thicker copper and narrow traces probably should be thinner. Be specific about what you need to ensure your design will not fail. Check land patterns against the part supplier's manufacturer datasheets (MDS) as well. Often, that is all it takes to avoid common design issues.

Consider How Your End Product Will Be Used

Your manufacturing partner does not know what type of device the board will be part of, or the conditions in which it will have to perform. It's common for harsh environments or exposure to interfere with a board's performance. To avoid catastrophic failure down the road, you must call out materials that will tolerate the final product's operating environment. Be sure your board and components can tolerate thermal stress or solder joints risk breaking and damaging components.

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Adhere to the Principles of DFM

We recommend integrating all these best practices into a design process that looks forward to the manufacturing process. Finding issues earlier makes them cheaper and easier to fix. From the outset, perform all design tasks while considering yield and other manufacturing issues that affect cost and quality.

Communicate with your manufacturing partner regularly throughout the design process. They can do more than just find problems. A good manufacturing partner has valuable insight into how design decisions impact manufacturability, yield, and quality of the boards.

Each manufacturer has unique capabilities and process requirements that can have a large impact on the manufacturability of your design, making an open line of communication critical. For example, your suppliers can confirm that you are using up-to-date footprint files throughout the design process.

Highly manufacturable designs exist within a range of specifications. Manufacturers can often help you tweak your design to make the best use of these ranges. Designer/manufacturer communication about DFM can help save time, reduce costs, and even improve the functionality of your board.

Help When You Need It

Choosing a manufacturing partner with readily available support staff can help you solve manufacturability puzzles during the design process, rather than after submission. It's useful to ask a few questions of any potential manufacturing partner before deciding.

- Is competent technical support available when you need it?
- How quickly will they respond to your needs?
- Email is slow, so how can you get support for time-sensitive issues?
- What is their escalation policy for difficult support requests?
- What support packages are available and how much do they cost?

The real key to optimizing the manufacturability of your PCB designs is choosing the right tools, process, and manufacturer that meet the needs of your design. Treat your parts suppliers, PCB manufacturer, and PCB fabricator as members of your design team. Prioritize open and persistent collaboration with each of them.

Good communication and adherence to a DFM-focused process will ensure board quality, manufacturability, and cost-effectiveness.

DESIGN007

Matt Stevenson is vice president at Sunstone Circuits, a division of American Standard Circuits. To read past columns, click here. Matt is also the author of *The Printed Circuit Designer's Guide to... Designing for Reality.*

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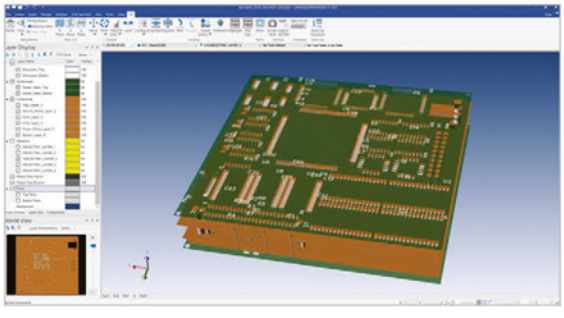

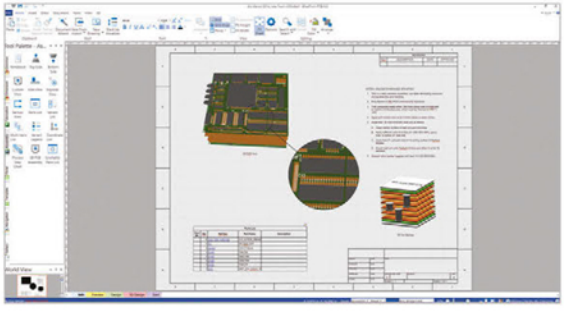

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Take It From Scotty: Simple Really Is Better

Tim's Takeaways

Feature Column by Tim Haag, FIRST PAGE SAGE

I am, at heart, a die-hard "Star Trek" fan. When I was a kid, I was all about phasers, warp drive, and cool stuff like that. However, these days, I tend to put a higher value on production and storytelling. But like any fan (I'm avoiding "Trekkie" because, frankly, it's kind of embarrassing), certain moments from the hundreds (if not thousands) of hours filmed for the various TV shows and movies are among my favorites. One of those moments is in "Star Trek III, The Search for Spock," when our heroes steal the Starship Enterprise from space dock.

The space dock scene is a pivotal moment in the movie. It is highlighted by excellent character interaction, humor, amazing music by the late great James Horner, and marvelous (for its time) special effects and cinematography. After some careful maneuvering to get the Enterprise out of space dock, Kirk and the crew fly away at warp speed, leaving their pursuers in the dust thanks to a little sabotage on the part of Scotty, the chief engineer. As it turns out, Scotty had previously removed some crucial components from the pursuing ship, causing their new and fancy computer to fail, and allowing the Enter-

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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prise to make a clean getaway. The scene ends with Scotty's sarcastic comment about the overly complicated computer on the other ship, "The more they overthink the plumbing, the easier it is to stop up the drain."

I've always liked Scotty more than anyone else on that show because, let's face it, he was an engineer. But with this movie, I really came to appreciate his common sense and, if I'm being honest, the sarcasm he used to describe it. Even in a universe where transporter beams and deflector shields are as common as the Keurig on my kitchen counter, Scotty still knew when something was too complex to be practical. Wise words, and a lesson here for everyone.

In our industry, we design and manufacture amazingly complex electronics. I've laid out circuit boards for everything from large computer systems to small wearable devices, and even though they have had different degrees of design difficulty, they all had the same common objective: They all had to work correctly once they were built. To accomplish this, circuit boards are designed according to several standards to ensure they can be manufactured and work as intended. If you are in the design and layout part of this business, you are no doubt already familiar with many of these different standards. But once you go beyond the industry standards and into the realm of rules, processes, and procedures, the water can get murky.

Take, for instance, the rules and constraints we use in the CAD system to design the board. These are wonderful tools and an essential lifeline for both design and manufacturing, but they can work against you if you aren't careful. Let's look at a couple of ways this can happen:

- **Too many rules:** Our design databases can become afflicted with the same problem that Scotty alluded to, where overthinking the plumbing can stop up the drain. For example, instead of defining a unique rule for each net and thereby managing thousands of rules, group your nets together according to their needs and assign them all to a single net class. This will save you time and system resources.
- **Lack of understanding:** It is important to be very familiar with what your PCB design CAD system will do with the rules you feed it. I've seen some databases where rules have clashed with each other, like keep-out areas that block a copper pour that is supposed to connect to a specific net in that area. If you don't rethink and redefine the rule, you have to either break it or turn checking off.
- **Old data:** Sometimes CAD databases get inundated with rules they simply don't need. This can happen when people read in stock rules from their corporate library, fail to clean out older rules already in their databases, or both. I've opened up some designs that have rules not even intended for that design but reside in the database, taking up additional resources.

Mismanaged design rules can overload your system as well as generate unexpected results.

Mismanaged design rules can overload your system as well as generate unexpected results. I'll summarize here by saying it is imperative that PCB designers know what rules are loaded into their systems and optimize those rules for the best performance of their design tools. But design rules are just part of the murky waters I described earlier. Now, let's look at processes and procedures for a moment.

Processes and procedures are an essential part of any design department. They organize the workflow, ensure that the proper steps, checks, and balances are in place, and serve as a guide to the users in the department. How-

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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ever, processes and procedures are not ever-fresh on their own. They can get stale quickly and must be reviewed regularly to look for areas needing optimization and enhancement.

For example, do you remember many years ago when PCB designers had to create an aperture list with every set of Gerber files that was sent out? I remember how I used to manually optimize my traces and pad sizes to match the limited amount of aperture positions on the mechanical aperture wheel in the photoplotter. Thankfully, apertures began to be included in the Gerber file when the file format was updated to RS-274X, which certainly made life much more convenient for me as a designer. And yet, many design department processes and procedures continued to insist that a separate aperture file still had to be created along with the set of Gerbers. Why?

Look at the processes and procedures you have in place to determine whether you can increase your and your staff's overall efficiency. Here are some areas to keep an eye out for:

- **Design reviews:** These meetings are essential, but do you need the same reviews you've always done? Many design reviews are driven by the needs and technologies of the time, so something may have changed and made some of these reviews redundant. On the other hand, some of your newer processes may reveal the need for an additional review at a spot you didn't expect.
- **Workflow:** Just as with the aperture list, areas of your documented workflow may have changed. Over time, you and your staff probably have adjusted to these changes without realizing it, and you could be in for some surprises when you hire and train someone new.
- **SOPs:** Like the workflow documentation, CAD departments often have a bunch of SOPs to help with everything from how to create a padstack to filling out a timecard. While SOPs like this should be documented, more often than not they exist as hidden text files and sticky notes.

Here is where open communication is essential to ensure that everyone in the department is aware of process changes and where to find official documentation on how to stay current with these changes.

To keep our department processes from getting "stopped up," we must work diligently to prevent our workflows from being unnecessarily complex.

To keep our department processes from getting "stopped up," we must work diligently to prevent our workflows from being unnecessarily complex. As we have seen, this includes not only the processes and procedures that guide our groups in their daily work, but also the design rules and constraints used to lay out a circuit board. Until next time, keep on designing everyone—and yes, "live long and prosper." DESIGN007

Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns, click here.

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Just a Matter of Time

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Electromagnetic energy propagates at about half the speed of light within the dielectric of a multilayer PCB. This speed is inversely proportional to the square root of the dielectric constant (Dk) of the material. The lower the Dk, the faster the propagation of the wave. In the past, we ignored the board-level delay as it was relatively instantaneous compared to the slow rise time of the signal waveform. But now that we have entered the realm of Gigabit/s design, an unaccounted 10 ps of delay can mean the difference between success and absolute failure of a high-speed design. Also, the trend is toward lower core voltages, which conserves power. However, reducing the core voltage also reduces the noise margin and impacts the system timing budget.


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Table 1: Overall DDR3-1066 timing budget allowances and resulting margin

Parameter	Setup (ps)	Hold (ps)
Open window from simulations	456	631
SDRAM setup and hold times from datasheets	25	100
Slew rate derating if >1V/ns	2.3	2.8
Timing offset with respect to VREF	13	11
SDRAM derating	88	50
Crosstalk	47	42
Controller error – skew	200	200
Clock error – jitter	30	30
PCB routing tolerance	10	10
Margin	**41**	**185**

Designing a memory interface is all about timing closure. Each signal's timing needs to be compared to the related clock or strobe signal in such a way that the data can be captured on both the rising and falling edge of the strobe—hence the term double data rate (DDR). The increase of data rates to 7800 MT/s for DDR5 has made the timing margin associated with each rising and falling edge even tighter.

Table 1 lists the various timing delays of a DDR3 memory interface running at 533 MHz. After allowing for the chip-level delay, setup and hold times, slew rate derating, clock skew, and jitter we are left with a total margin of just 41 ps on the setup time. Even at this relatively low clock frequency of 533 MHz, 10 ps is all the margin we have left for the board-level delay. Increase the crosstalk or jitter and we are looking at imminent system failure. So, the velocity of propagation of the electromagnetic wave of energy through the PCB is now very significant.

Most systems, whether at the chip or board level, operate synchronously; as such, voltage levels must rise or fall within a specified time or else the circuit will be out of sync and failures will occur. The timing budget tells us how much margin we have, or to put it another way, how much headroom we have before a failure occurs.

So, how do we go from a timing spec (Figure 1) to the actual flight time of the entire memory interface?

The signal and timing, relative to other signals, ride on an electromagnetic carrier wave at various speeds, depending on the surrounding dielectric materials. This energy transports the signal from the driver along the transmission line to the load and does not disrupt the original timing but rather adds the same delay to all the signals that travel the same path. So, one must keep all the relative signals on the same path (layer) or there will be discrepancies when the signals arrive at the load. Alter-

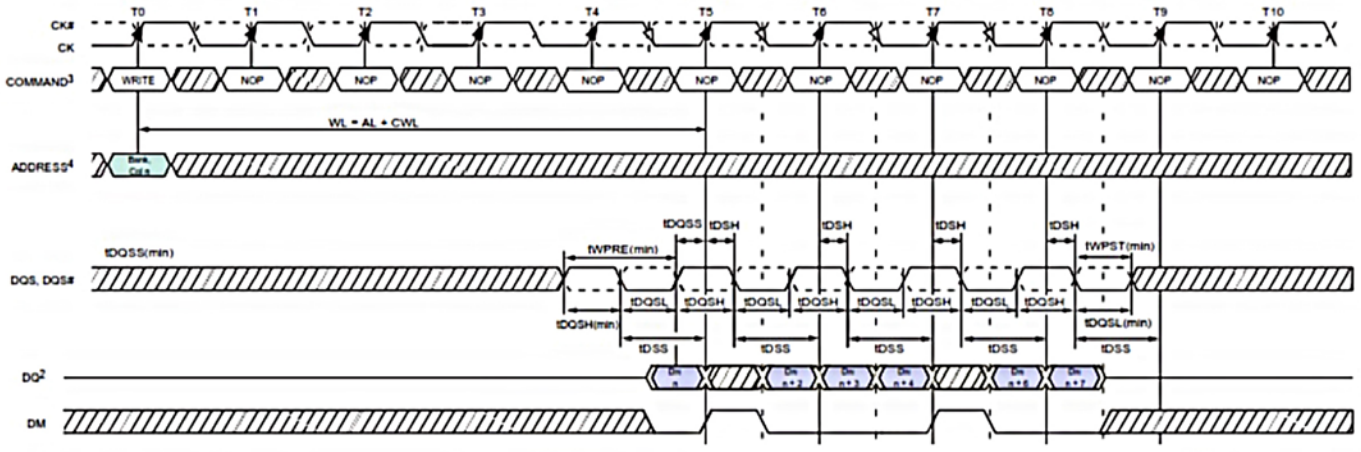

Figure 1: DDR3 synchronous timing. (Source: JEDEC Std 79-F3)

natively, one can compensate for a delayed layer by adding delay intentionally using serpentines to the signal trace in question.

Clocks are essential gatekeepers of the digital domain. Setting the pace for all that follows the clock can be a single trace or differential pairs that carry complementary signals. Because each bit of the data bus must arrive and become stable before the clock cycle, the clock signals establish setup time for accepting or extracting the data. The hold time ensures that the entire bus remains steady during the read-in or read-out of data after the clock.

Fortunately, synchronous buses, as typically used for parallel data signal transfer, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an impact within a small window around the moment of the clocking. The crosstalk must be specified during the setup (t_S) and hold (t_H) window at the receiver. During this interval, the crosstalk must never drive any valid signal across the receive threshold to the opposite logic state.

So, providing the receiver waits sufficiently long enough for the crosstalk to settle before sampling the data bus, the crosstalk has no impact on the signal quality at the receiver. If the crosstalk arrives during the signal transitions, then its only impact is jitter on the eye. However, this only applies to signals within the same group. Asynchronous and unrelated

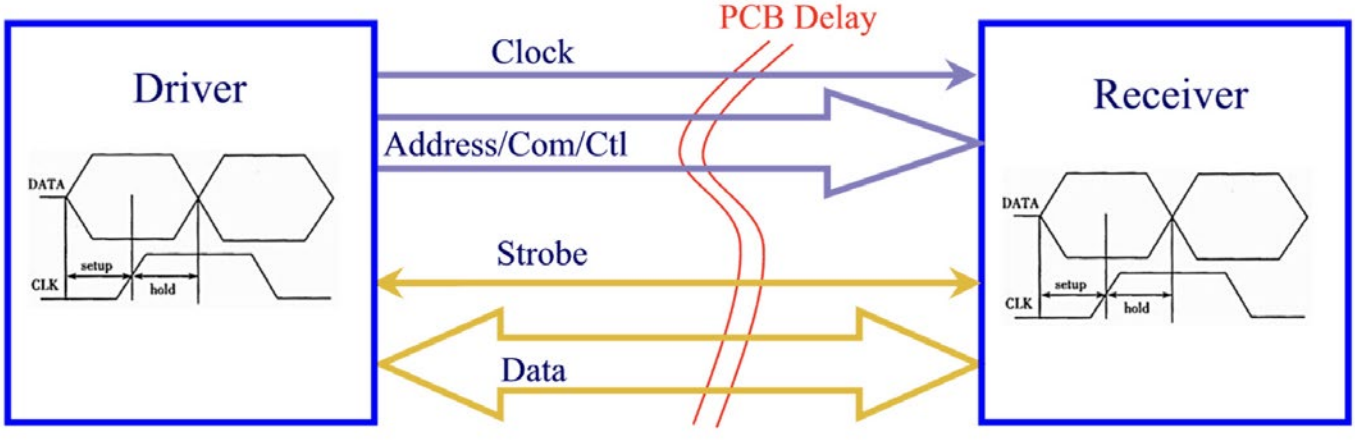

Figure 2: Source synchronous timing relationship across substrate.

signals, on the other hand, always remain sensitive to crosstalk.

From a PCB designer's perspective, we can only optimize what we can control and that is just the placement and routing. Ensuring the route tolerance is less than 10 ps is all we can do to stabilize the design. This may sound tight and difficult to manage but I do this routinely whether called for or not. Put in a little extra effort during layout and one can achieve perfect timing with every design.

A stripline is any trace sandwiched between reference planes on both sides. The electric fields of a stripline are totally contained between the two solid planes, so the speed of propagation for signals guided by the trace is entirely determined by the dielectric constant of the surrounding materials.

On the other hand, a microstrip is any trace fabricated on the surface layers of a PCB. A microstrip has dielectric material and a plane on one side and air on the other. An embedded microstrip is similar but is covered in a conformal coating such as solder mask or another dielectric material. In this case, the effective dielectric constant should be calculated by a field solver and represents a combination of the surrounding materials. There are also other variants of microstrip and stripline, such as build-up microstrip and dual asymmetric stripline.

The electric fields surrounding the microstrip exist partially within the dielectric material(s) and partially within the surrounding air. Since air has a dielectric constant of 1, which is always lower than that of FR-4 (typically 4.3), mixing a little air into the equation will speed up the signal propagation. Even if the trace widths are adjusted on each layer so that the impedance is identical, the propagation speed of the microstrip is always faster than the stripline, typically by 13–17%. The speed of propagation of digital signals is independent of trace geometry and impedance.

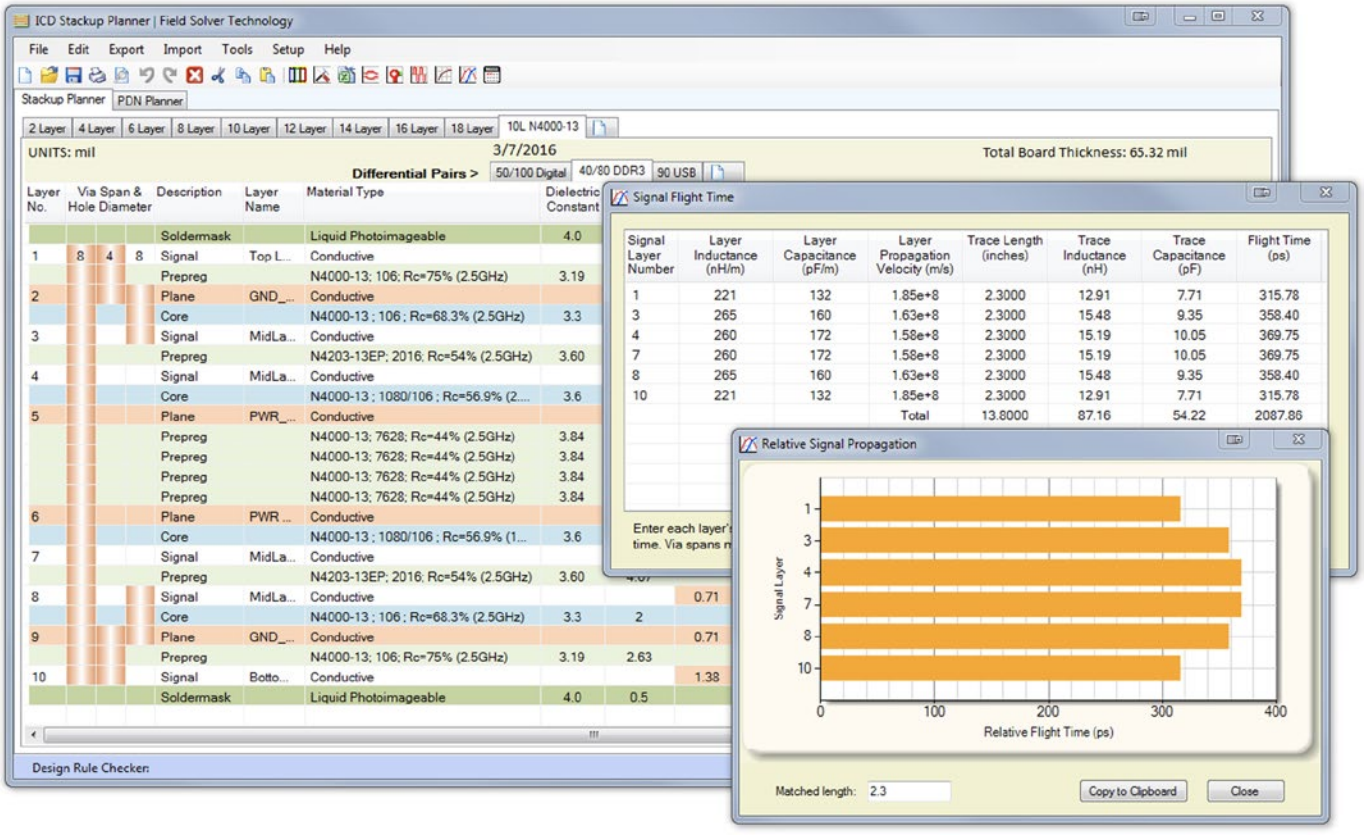

Figure 3: Relative signal propagation for each signal layer on a 10-layer DDR3 stackup. (Source: iCD Stackup Planner)

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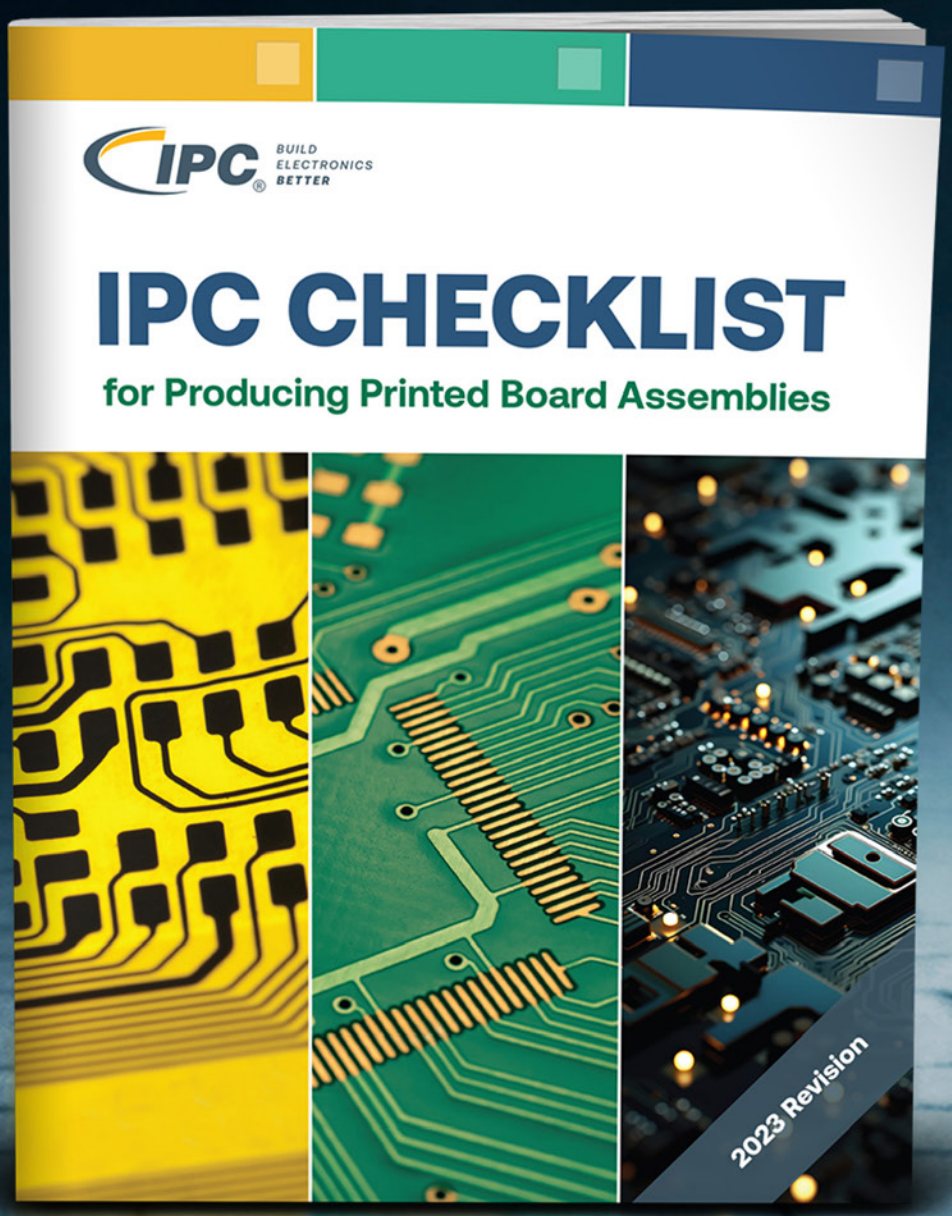

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If you are aware of this issue, then the trace delays (Figure 3) can be matched to compensate for the flight time variance, so that at the nominal temperature all signals running on either microstrip or stripline will arrive at the receiver simultaneously. It is good design practice to route each memory bus on the same layers. That is, avoid routing on the surface layers other than fanout, and drop immediately to the internal stripline layers routing all data, address, associated clocks/strobes, and control signals on the same layer pair to avoid propagation delay variance.

Key Points

- Electromagnetic energy propagates at about half the speed of light within the dielectric of a multilayer PCB.
- The lower the Dk, the faster the propagation of the wave.
- Designing a memory interface is all about timing closure.
- The signal and the timing, relative to other signals, ride on an electromagnetic carrier wave at various speeds, depending on the surrounding dielectric materials.
- This energy transports the signal from the driver, along the transmission line to the load, and does not disrupt the original timing but rather adds the same delay to all the signals that travel the same path.
- Clocks are essential gatekeepers of the digital domain.
- Synchronous buses benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an impact within a small window around the moment of the clocking.
- Asynchronous and unrelated signals always remain sensitive to crosstalk.
- From a PCB designer's perspective, we can only optimize what we can control and that is just the placement and routing.
- Even if the trace widths are adjusted on each layer, so that the impedance is identical, the propagation speed of the microstrip is always faster than the stripline, typically by 13–17%.
- The speed of propagation of digital signals is independent of trace geometry and impedance. **DESIGN007**

Resources

• Beyond Design: "Crosstalk Margins," "DDR3/4 Fly-by vs T-Topology Routing," "Signal Flight Time Variance in Multilayer PCBs," by Barry Olney

• "Board-level timing analysis," Tech Design Forum Techniques.

• "High-speed PCB design timing analysis and simulation strategy," Engineering Technical, PCBway.

• "Understanding Simulation Analysis Parameters for DDR4 Bus Systems in SystemSI," Cadence.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.

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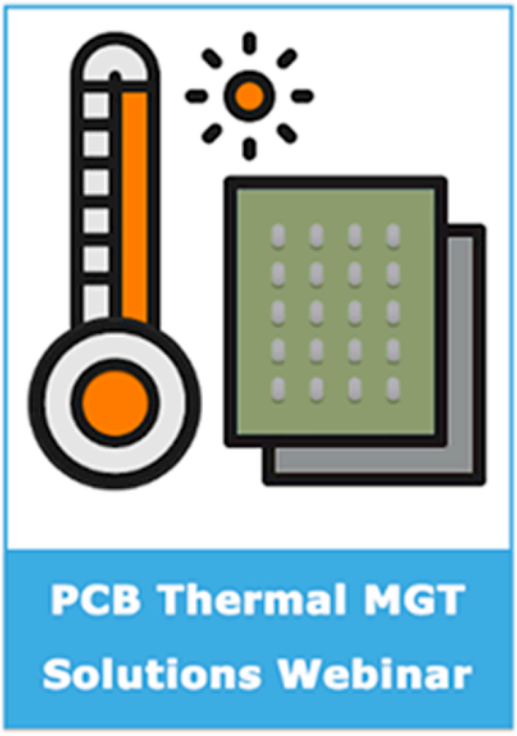


UHDI FUNDAMENTALS:

Talking UHDI With John Johnson, Part 1

Interview by Steve Williams
FOR ASC

American Standard Circuits is an early adopter of Averatek's A-SAP™ process for its ultra high definition interconnect (UHDI) products. I sat down with industry veteran John Johnson to discuss this. John, vice president of business development, oversees quality at American Standard Circuits, and previously worked at Averatek. In the spirit of full disclosure, we will be discussing and sharing photos, slides, and materials with permission from both ASC and Averatek. This is the first of a three-part interview.

Steve Williams: Welcome John, good to see you again.

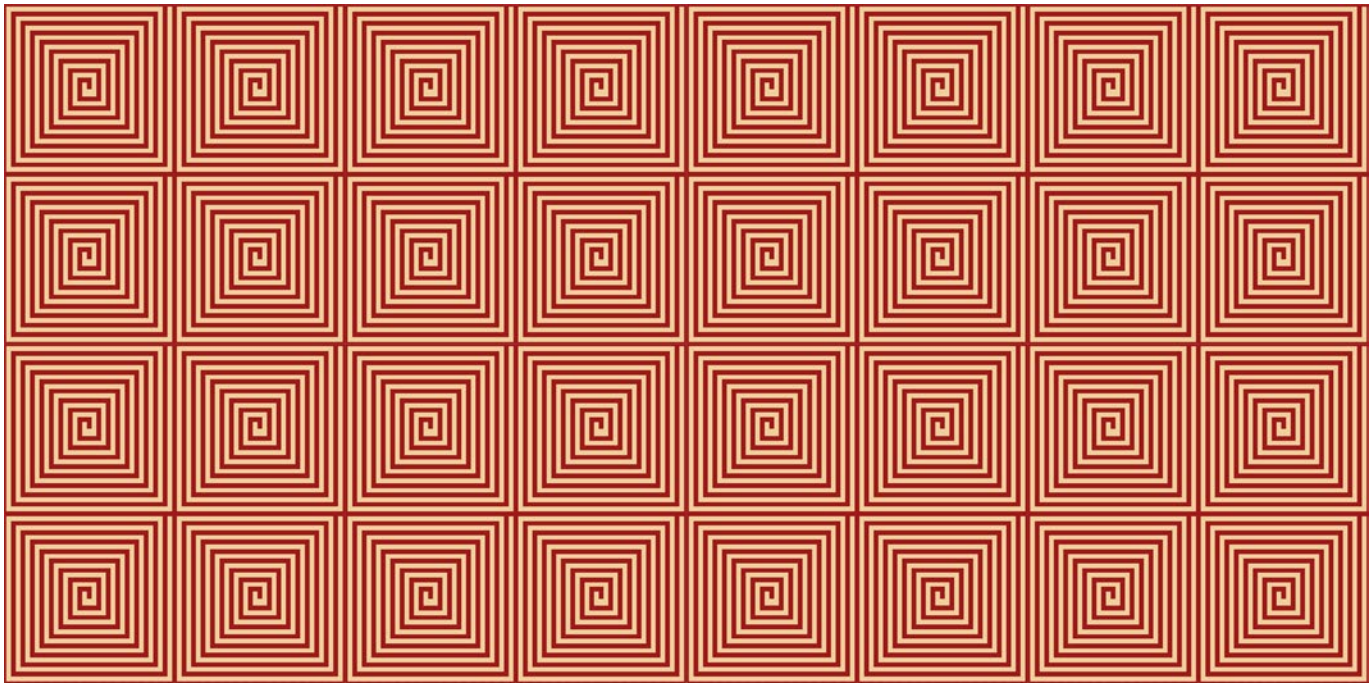
John Johnson: Thank you, Steve. It's my pleasure. I'm always looking for opportunities to talk about UHDI and the A-SAP process.

What does A-SAP stand for? What does it mean?

The A in A-SAP stands for Averatek, and of course, SAP is a semi-additive process. So, it's an Averatek semi-additive process they've developed for the electronics industry, predominantly circuit boards.

Very good. You've had a lot of leadership positions in the industry, but before American Standard, you worked at Averatek. Tell me about that.

I was the vice president of sales and customer support and, predominantly, my role was working with the licensees to get them up and running, to bring product realization to the forefront with them.



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The fully additive process is a pretty old process, and I remember back when they were making print and etch boards with 15-mil line width and space. What's the difference between additive and semi-additive?

Semi-additive is similar, but it's not. With that old additive process, those processes would run in plating for 24 hours or more to get the right plating thickness, but in this process, we are putting down a very thin layer of electrolytic copper as a base metal, rather than using an ultra-thin foil or something like that.

Once that's defined, then we go down with a photoresist and image trace patterns, which are actually trenches in the resist. Then we plate those up and strip away the resist, and there we go. We'll just flash-etch the base electrolytic copper so it's not touching the circuit walls at all. It really looks like an additive-type trace, but it's plated up inside that trench. You then get perfectly straight sidewalls and a lot of benefits toward signal integrity.

Talk a little bit about chemistries and what kind of applications this process typically is made for?

This process works well for anyone trying to define a very thin-lined trace, and it works for ultra-high density circuit boards. In fact, that's what we call our program: ultra-high density interconnection. If you look at any high-performance HDI circuit boards, they can benefit from this technology where you have something sub-75-micron trace and space—the old 3-mil lines and spaces. If you have a 2-mil and, let's say, via-in-pad plated over with multiple plating steps, this technology can help; it's a pretty broad range for packaged substrates and interposers. There are many buzzwords floating around in the U.S. because they're bringing this technology back here to support the supply to critical industries like defense and aerospace. This allows us to not be so dependent on the Far East. But it requires traces that are sub-25 microns (sub-1 mil), so this chemistry works well for that as well as passives like inductors and capacitors inside the boards. The technology for embedded capacitors and resistors is not new, but certainly, this can be done in a different way where you're building traces that are very tall and narrow, meaning that your aspect and spacing ratios are tight. For antennas and wave-

John Johnson

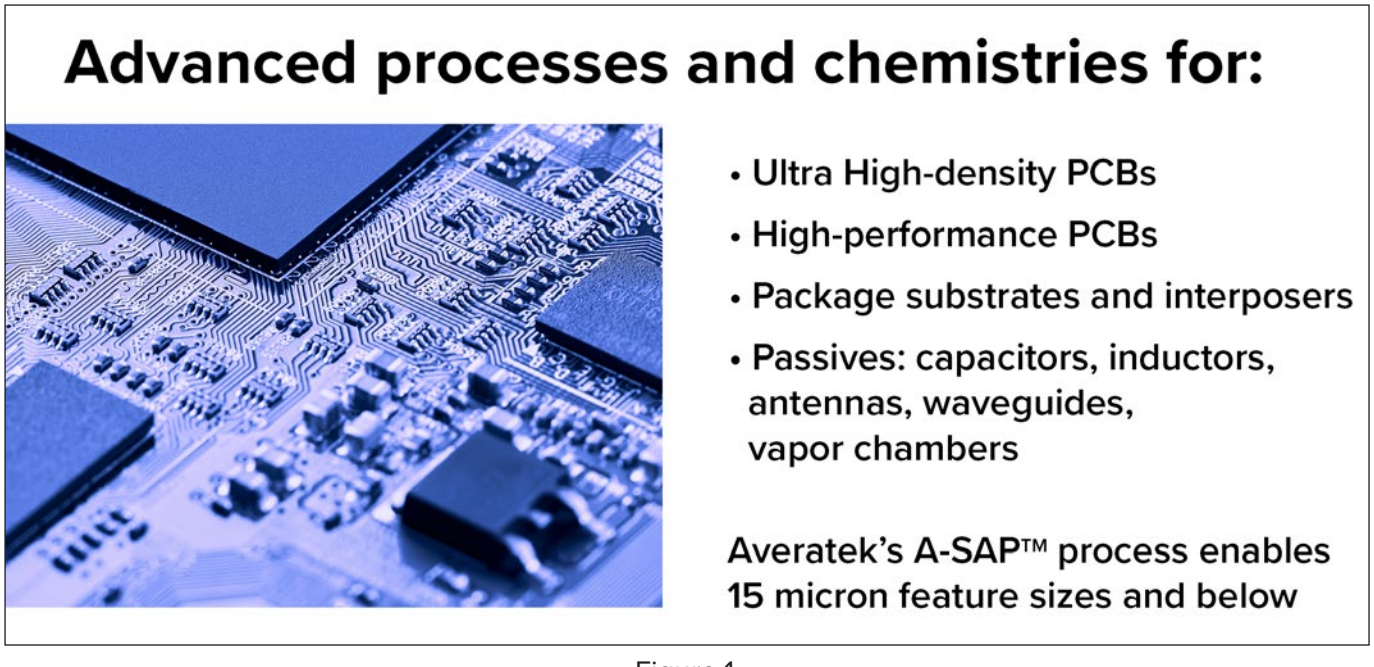

Figure 1.

guides, there are many aspects that Averatek has worked on to grow this into different passives. For the future, they're looking at ways to embed chips, so it's pretty exciting.

That is exciting stuff. I remember when 3-mil line and space was the state-of-the-art, or even the bleeding edge if you go back far enough.

It's nice to see this type of technology come around because it certainly gives us a chance to leapfrog over where Asia is today.

Tell me about some of the advantages of this technology.

When you look at the circuit board today, we're locked in at 3-and-3; some folks can do 2-and-2 in lines and spaces, but that might be by accident. If you can get down to 25-micron (1-mil) lines and spaces, you can reduce the size of the circuit board. Already the chips have gone smaller and smaller in terms of pitch. Half-millimeter BGAs are fairly common and we keep hearing it will go down to 0.35 mil, 0.3 mil, and who knows from there. Well, you can't route that out of a pattern very easily with even a 2-mil line and space. You have to get down to the 1-mil line and space. That helps, but when you're doing that, you're reducing layer counts and the number of microvias in a structure, which can improve reliability. You don't need as many stacked microvias. When I was at Averatek, we looked at situations of reconfiguring 12-layer boards with many subassemblies down as far as a two-layer board. It's quite amazing when getting to the ultrafine lines and spaces.

Oh, absolutely John.

Look for Part 2 of this interview in the December 2023 issue of *Design007 Magazine.*

DESIGN007

Steve Williams is president of The Right Approach Consulting. He is also an independent certified coach, trainer, and speaker with the John Maxwell team.

Accelerating Battery Research With Robots

Empa researchers want to accelerate the development of urgently needed new energy storage systems with the help of the Aurora battery robot. The Aurora project is part of the European research initiative Battery2030+, which was recently awarded over 150 million euros in funding by the EU. In addition, the project is part of the ETH Board's "Open Research Data" initiative, which promotes digitization and free access to research data.

The world urgently needs new types of energy storage. Developing completely new concepts for batteries and exploring their potential is currently a lengthy process, as Corsin Battaglia, head of Empa's Materials for Energy Conversion laboratory in Dübendorf and professor at ETH Zurich, emphasizes: "Our goal is to accelerate this process."

The robotic platform is currently being further developed in the Empa laboratories together with the company Chemspeed Technologies AG. Empa researcher Enea Svaluto-Ferro is implementing the work steps and "training" Aurora.

"While the robot weighs, doses and assembles the individual cell components with constant precision, initiates and completes charging cycles precisely and performs other repetitive steps, researchers can use the generated data to drive the innovation process forward," says Svaluto-Ferro.

(Source: Empa)

Flex007 Highlights

With Flex and Rigid-flex, Ask the Right Questions ▸

I recently met with Tony Plemel, senior applications engineer with Flexible Circuit Technologies. In this interview, Tony discusses when flex designers need to break the rules, when they can't break the rules, and why it's so important for fabricators to ask designers the right questions to ensure a successful build.

Insulectro Flex Materials Showcase Offers Tips for Technologists ▸

Insulectro continues its drive to educate PCB designers about the ins and outs of advanced flex materials. On Sept. 19, the company hosted an all-day seminar on flexible and printed electronic materials at its San Jose, California, facility. The event kicked off with a presentation by Dave Rosenfeld, a technical fellow at Celanese, which acquired DuPont's mobility and materials business last year.

Got Questions? Standards Have the Answers ▸

The I-Connect007 Editorial Team recently spoke with Gerry Partida, vice president of technology at Summit Interconnect, and co-chair of the IPC-6012 committee. Gerry has been involved with standards development for years, and he believes that adhering to IPC's standards and specifications has been a big part of Summit's success.

Selecting a Rigid-flex Manufacturer ▸

If you're coming from the rigid PCB world, you're probably wondering how to get started and how to select a rigid-flex vendor. Mike Morando explains that if you're designing PCBs for an OEM that is betting everything on a next-generation rigid-flex design, you would want to use the absolute best vendor for your rigid-flex design. Your new rigid-flex design needs to be put into the right shop to leverage the best manufacturing solution.

Standard of Excellence: Keep Learning or Start Dying ▸

"Keep learning or start dying" is an old but morbid (to say the least) phrase that's perfectly suited to our own PCB industry. I would tweak it just a bit and say that if you're not increasing your technology level and expanding your technology roadmap, your company will start to die. I think one of the reasons for the demise of PCB manufacturing in our country over the past 20 years is that many companies stopped investing in their future. Anaya Vardya explains.

Wearables Bounce Back with 8.5% Growth in Q2 2023 and a Positive Forecast ▸

Global shipments for wearable devices returned to growth in the second quarter of 2023 (2Q23) reversing two quarters of decline, according to new data from the International Data Corporation (IDC) Worldwide Quarterly Wearable Device Tracker. The market grew 8.5% year over year with shipments totaling 116.3 million devices.

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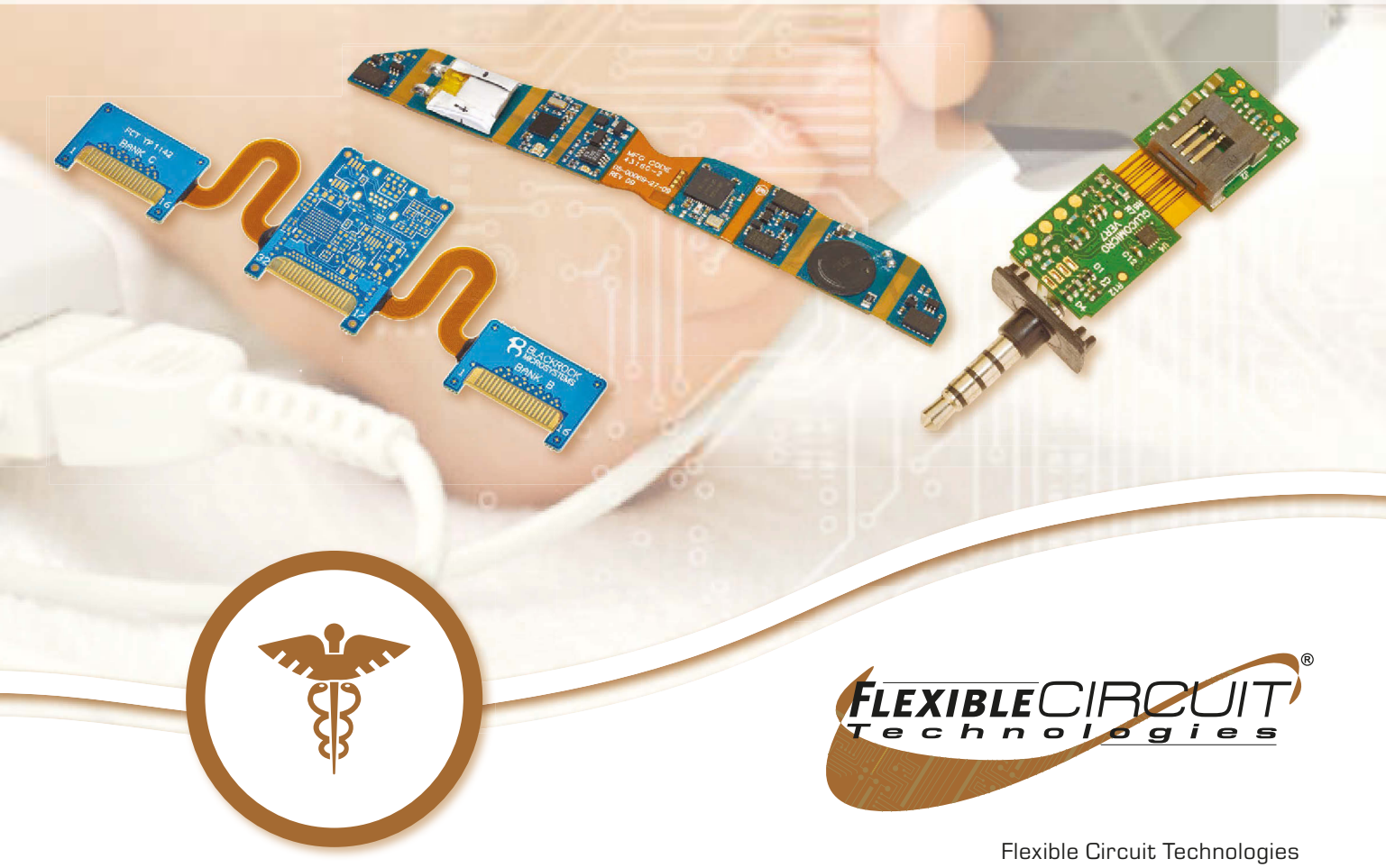

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The Simplest Way Is the Best Way

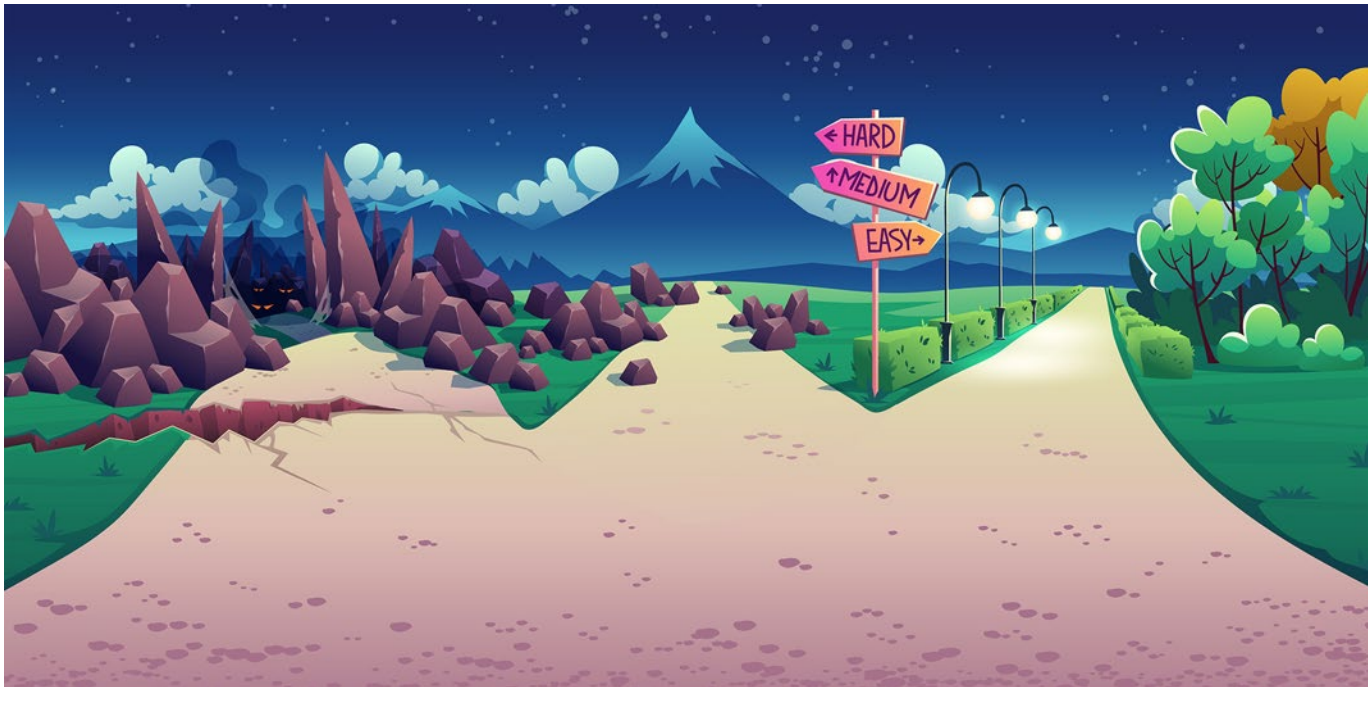
Flexible Thinking

Feature Column by Joe Fjelstad, VERDANT ELECTRONICS

Interconnection substrate technologies (PCBs, flex and rigid-flex circuits, and IC packaging substrates) have made possible the steady advance of electronic products for more than seven decades. They are foundational structures for electronics and arguably the backbone of modern electronics. However, their design and manufacture has become increasingly challenging over the years.

Much has been written about these challenges and numerous solutions have been offered (including my own), but with so many ideas and prospective solutions in play these days, we should understand some basics before jumping in to make sure we don't get in over our heads.

In a presentation I made at a conference about a dozen years ago, I concluded, "First do the right things and then do those things right." I don't doubt that others have come to that conclusion, but it was an epiphany in the moment. So, with so many solutions being floated out there, the challenge is in determining what is right, and therein lies the rub (as the great English bard so eloquently stated). In this brief commentary, I will discuss various strategies and tools to simplify PCB design, making it accessible to a wider range of industry participants even as constant change remains upon us all.



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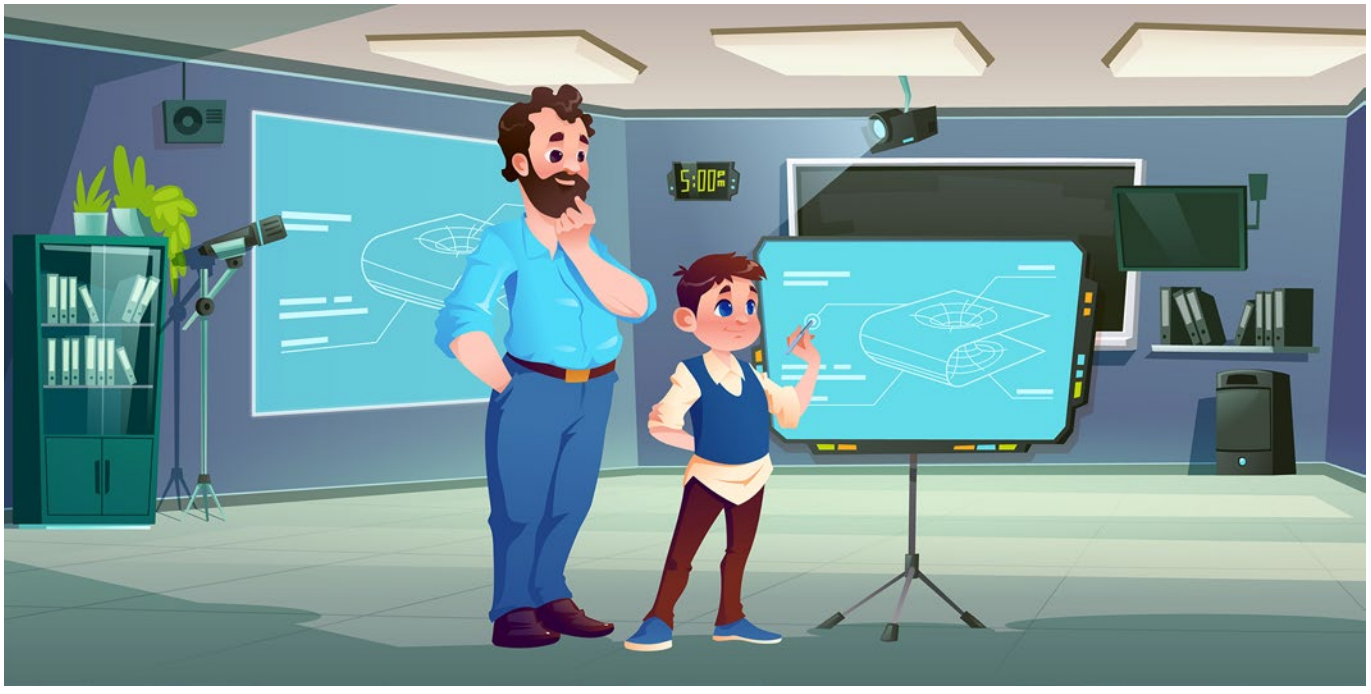


Start With a Plan

The first step in simplifying PCB design is to start with a clear and well-thought-out plan. Define the objectives of your project and the functions the assembly will desirably perform. This will, of course, include a list of the key components needed. Having a comprehensive design plan in place before you dive into the technical details will save you time and reduce errors down the line. To prevent getting blindsided, it is important to consider extraneous factors, like size constraints, power requirements, and signal integrity concerns.

Choose Your Software

Choosing one's design software is essential for a streamlined design process. There are various software suites available that provide schematic capture, PCB layout, and library management functionalities crucial for an efficient design workflow. The advertisements of many of these providers can invariably be found in industry literature (including the content of this magazine), offered for consideration by design tool ad sponsors. They vary in terms of their broader capabilities and price, and the demands of your designs will influence the choice. To allow for seamless handoff, ensure that they have compatibility with other manufacturing software. Gerber-based document packages are frequently called out in this regard, though IPC-2581 and ODB++ are slowly increasing in use.

Break Down the Process

It is generally advisable to break your PCB design into smaller, manageable modules. Such a modular approach simplifies the design process by allowing the designer to focus on individual sections of the overall interconnection structure. This allows one to design and test individual modules separately before integrating them into the final board design. Such an approach also serves the cause of reusability, which can save time and effort on future projects. It is a practice learned and used commonly by semiconductor chip designers as well.

Most PCB design software tools include libraries of pre-designed components, such as resistors, capacitors, microcontrollers, and the like. These libraries should be tapped to streamline your design process. Library components have predefined footprints and schematics, reducing the need for extra work and ensuring compatibility.

Keep It Simple

"Less is more" is a timeless adage and it holds no less true in interconnection design. (It has been a key objective of the Occam Process which I have been advocating for many years.) Certainly, there are many interconnection designs that require circuit substrates having multiple layers but they can significantly increase design complexity and signal integrity management. Strive to keep layer count down. Fewer layers, with thoughtful, simplified routing will reduce manufacturing costs and make it easier to debug and troubleshoot your PCB (if, but hopefully not, needed).

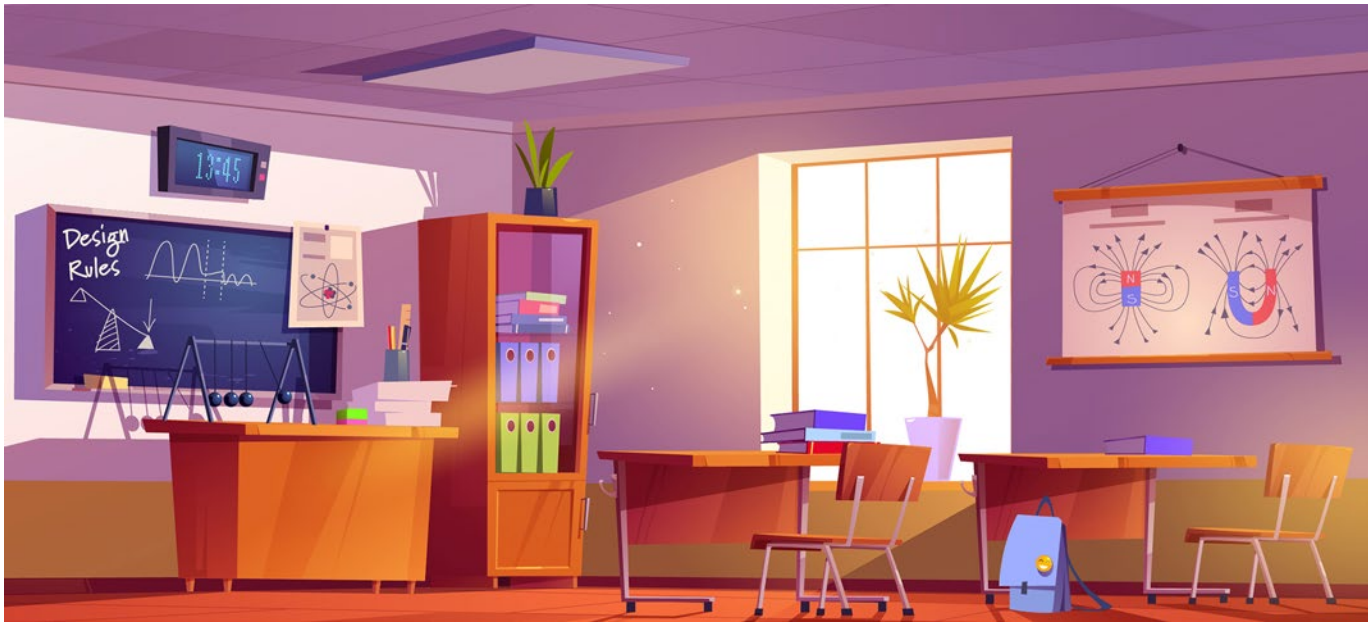
DRC and DFM

Use design rule check (DRC) and design for manufacturing (DFM) tools that are commonly provided in PCB design software. These tools automatically check your design against manufacturing constraints and provide feedback on potential issues. Leveraging these tools can save you from costly design errors and revisions, as well as simplify the communication with your board manufacturer. In this regard, I refer one of my previous columns about designing with manufacturing (DWM). While I can't say for certain that I was first to use the term (perhaps not) but I've noticed that it's used more frequently these days. This is a good thing as the need to work closely with manufacturing is becoming ever more apparent, especially with more challenging interconnections, like flexible circuits. The manufacturer knows where the limits are, then taps into and uses that knowledge.

That said, every PCB manufacturer has their own specific design rules and guidelines that must be understood and abided by to assure a successful fabrication process. Familiarize yourself with those rules and incorporate them into your design process early on. This will help circumvent issues related to minimum line and space widths, as well as minimum capture pad and via or drilled hole sizes that can negatively impact the manufacturing process and lead to delays and/or costly mistakes.

Present-generation PCB design software typically comes with built-in DRC and DFM tools that automatically check your design against general manufacturing constraints and provide feedback on potential issues when identified. Leveraging these tools can save you from costly design errors and revisions, as well as simplify communication with your vendor.

Auto-routing tools are also common and are a godsend for today's increasingly complex designs. Auto-route tools can significantly simplify the routing process by automatically connecting components while adhering to



established design rules. While manual routing is often necessary for critical or sensitive signals, auto-routing can handle simpler connections and save you time in the design phase.

Testing

I decided some years ago that testing is somewhat of a necessary evil. It really doesn't provide any value ("first do the right things and then do those things right"), however, until we can collectively believe in and execute on that precept there will likely be a need to make some allowance for test points and their access to troubleshoot when things go sideways.

Some Like It Hot

Electronics get hot in operation. It is a fact of life (and physics), has always been an issue, and it is becoming increasingly critical as design densities, operating frequencies, and speeds increase. It is therefore necessary for the designer to be familiar with thermal management structures and their uses. These include properly-sized heatsinks, and the design, construction, and use of thermal vias, thermal pads, and the like to maintain a stable operating temperature for temperature-sensitive components and to enhance product longevity.

Maintaining a good and traceable paper trail for your design and providing comprehensive documentation of the design are both important to assure that learning is captured for future efforts. Thus, maintaining detailed schematics, layout files, and version control is vital for capturing the effort as a learning tool for reference and use with future revisions.

Seek Feedback

Finally, one should not shy away from getting feedback from colleagues, design gurus, and mentors on your efforts. We are all, to one extent or another, teachers and students of each other, so getting feedback can serve to provide fresh perspectives and solutions to simplify and improve your future designs. Keep learning.

In summary, interconnection design, be it rigid or flexible, is often a daunting task but the task can be simplified by using good strategies and the right tools. The simple steps described here are more of an overview than a complete prescription, but it is believed sufficient to set the attentive designer on the road to success.

Embrace change and the future because they will always be there.

Lastly, don't ever stop advancing your education. Try to keep current with the technology. There are new approaches to IC design and manufacture entering the playing field on a regular basis, because technology never sleeps and new problems cannot always be solved with old methods. Embrace change and the future because they will always be there. **DESIGN007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition*, and watch his in-depth workshop series "Flexible Circuit Technology."

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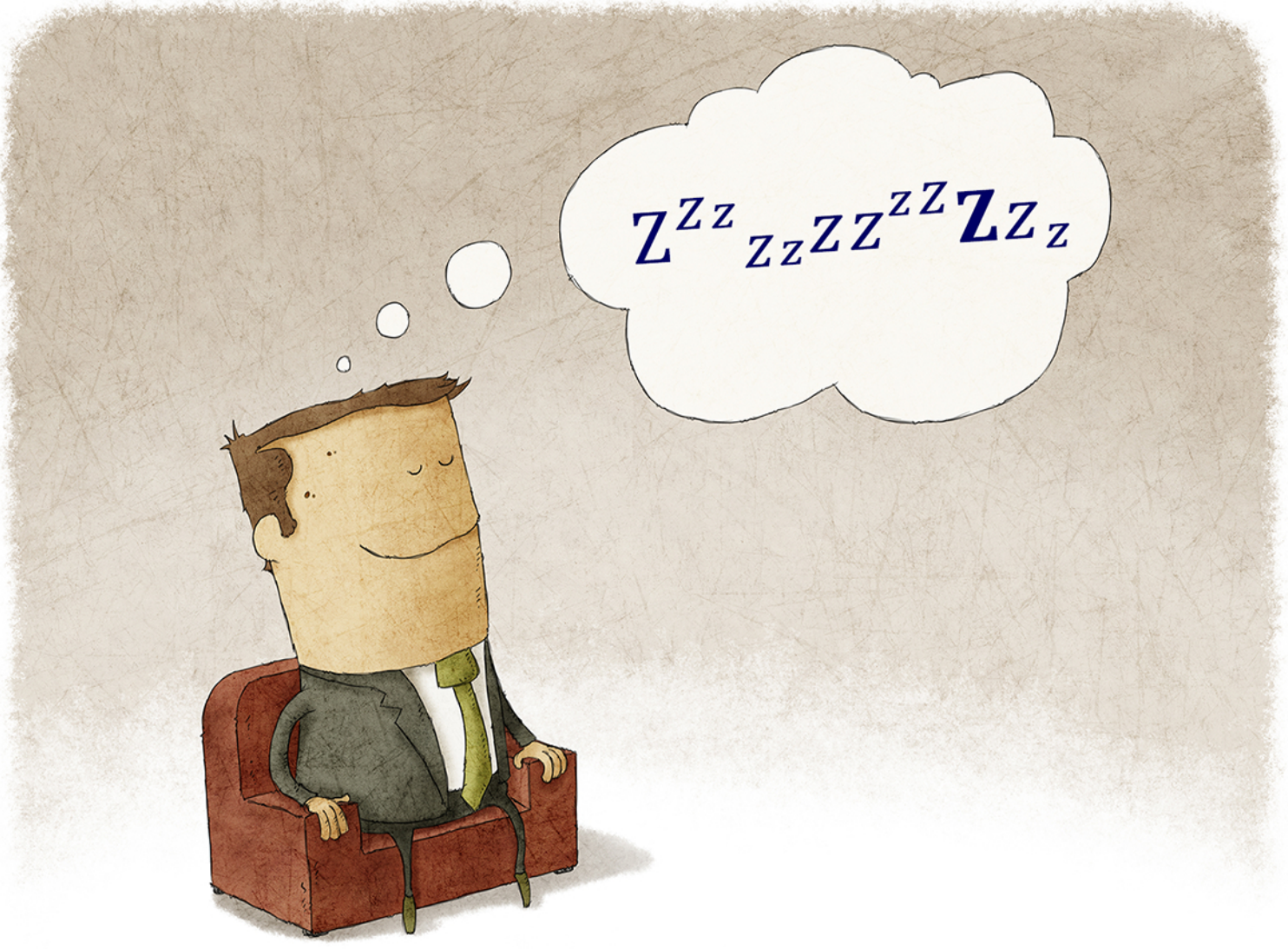

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TOP TEN

EDITOR'S PICKS

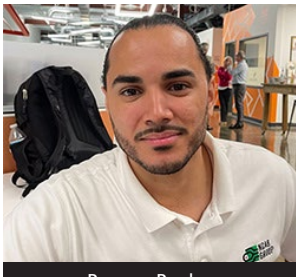
Cadence Reports Third Quarter 2023 Financial Results

Cadence reported third quarter 2023 revenue of $1.023 billion, compared to revenue of $903 million for the same period in 2022. On a GAAP basis, Cadence achieved operating margin of 29 percent and recognized net income of $254 million, or $0.93 per share on a diluted basis, in the third quarter of 2023, compared to operating margin of 29 percent and net income of $186 million, or $0.68 per share on a diluted basis, for the same period in 2022.

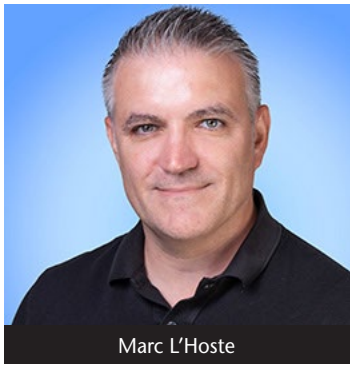
IPC Standards: Ticket to a Safe Passage

When we met with John Watson, we asked him to discuss the importance of understanding IPC standards, the price you'll pay if you decide not to follow them, and his plans for getting new designers on board with standards as early as possible in their careers.

Fresh PCB Concepts: Sustainable PCBs— Raw Materials and Compliance Methods


Ramon Roche

The shift toward sustainability in the printed circuit board industry has required PCB producers to rethink their manufacturing processes and who they do business with. NCAB's Ramon Roche reports that a PCB producer's sustainability efforts are for naught if their raw materials providers are not in regulatory compliance.


Marc L'Hoste

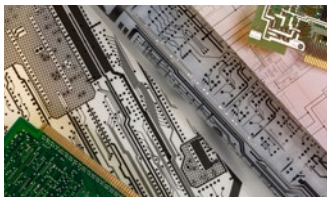
Planning, DFM, and Inspection: Key to High-reliability Fab

We asked ICAPE's Marc L'Hoste to share some advice regarding high-reliability fab. In this conversation, Marc is clear that planning, pre-work, and inspection are the key ingredients to high-reliability success.

Advanced Materials Update with John Andresakis

I recently sat down for an interview with John Andresakis, the director of business development for Quantic Ohmega. I asked John to update us on the company's newest materials, trends in advanced materials, and the integration of Ticer Technologies, which Quantic acquired in 2021.

Connect the Dots: Choosing the Right CAD Tool



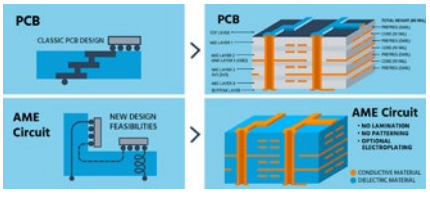
Sunstone's Matt Stevenson says each designer has different needs from a CAD tool. Some only produce a few designs per year, which means there is limited opportunity to learn the ins and outs of complex CAD software. Others constantly work on PCB design, moving from one design to the next with barely enough time to catch their breath. How can designers find the right CAD tools to fit their design needs?

Dana on Data: IPC AME Standards Development Launched

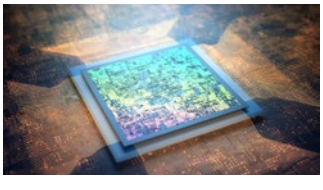
An important element of design requirement determination and manufacturing requirements, says Dana Korf, involves qualification, performance, and inspection standards. These are critical to ensure that the product's electrical, mechanical, and reliability requirements are met without expensive over/under specification.

Downstream Technologies Releases CAM35 Version 15 and BluePrint-PCB Version 7

"We constantly query our customer base and they are always providing feedback on how to improve our products," said Rick Almeida, one of DownStream's founders. "Based on that input, we have responded with new releases which include significant additions and enhancements."



UHDI Fundamentals: Ultra HDI Pushes PCB Manufacturing Capabilities



Ultra high-density interconnect (UHDI) is a term used in the electronics industry to describe a cutting-edge technology that pushes the limits of fabrication capabilities for printed circuit boards (PCBs) and semiconductor devices. Anaya Vardya explains that UHDI represents an advancement in miniaturization and integration, allowing for the creation of electronic components and systems with extremely high levels of functionality in a smaller footprint.

PCB Design Software Market Size to Reach $2.53 Billion in 2032

The global printed circuit board (PCB) design software market size reached $1.15 billion in 2020 and is expected to register a significantly steady revenue CAGR during the forecast period, according to latest analysis by Emergen Research.

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Regional Manager

Southwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the Southwest Region. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deploy-ment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
  - Reviews progress of sales performance
  - Provides quarterly results assessments of sales reps' performance
  - Works with sales reps to identify and contact decision-makers
  - Setting growth targets for sales reps
  - Educates sales reps by conducting programs/seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

apply now

Career Opportunities

EMA Design Automation

Technical Marketing Engineer

EMA Design Automation, a leader in product development solutions, is in search of a detail-oriented individual who can apply their knowledge of electrical design and CAD software to assist marketing in the creation of videos, training materials, blog posts, and more. This Technical Marketing Engineer role is ideal for analytical problem-solvers who enjoy educating and teaching others.

Requirements:

- Bachelor's degree in electrical engineering or related field with a basic understanding of engineering theories and terminology required
- Basic knowledge of schematic design, PCB design, and simulation with experience in OrCAD or Allegro preferred
- Candidates must possess excellent writing skills with an understanding of sentence structure and grammar
- Basic knowledge of video editing and experience using Camtasia or Adobe Premiere Pro is preferred but not required
- Must be able to collaborate well with others and have excellent written and verbal communication skills for this remote position

EMA Design Automation is a small, family-owned company that fosters a flexible, collaborative environment and promotes professional growth.

Send Resumes to: resumes@ema-eda.com

apply now

pluritec®

MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and x-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport for travel.

Must be able to travel extensively.

apply now

Career Opportunities

Technical Service & Applications Engineer

Full-Time — Flexible Location

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement-based inspection technology for electronics manufacturing. Located in Duluth, GA, Koh Young America has been serving its partners since 2010 and is expanding the team with an Applications Engineer to provide helpdesk support by delivering guidance on operation, maintenance, and programming remotely or on-site.

Responsibilities

- Provide support, preventive and corrective maintenance, process audits, and related services
- Train users on proper operation, maintenance, programming, and best practices
- Recommend and oversee operational, process, or other performance improvements
- Effectively troubleshoot and resolve machine, system, and process issues

Skills and Qualifications

- Bachelor's in a technical discipline, relevant Associate's, or equivalent vocational or military training
- Knowledge of electronics manufacturing, robotics, PCB assembly, and/or AI; 2-4 years of experience
- SPI/AOI programming, operation, and maintenance experience preferred
- 75% domestic and international travel (valid U.S. or Canadian passport, required)
- Able to work effectively and independently with minimal supervision
- Able to readily understand and interpret detailed documents, drawings, and specifications

Benefits

- Health/Dental/Vision/Life Insurance with no employee premium (including dependent coverage)
- 401K retirement plan
- Generous PTO and paid holidays

apply now

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- **Engineering**
- **Quality**
- **Various Manufacturing**

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

apply now

Career Opportunities

INSULECTRO

Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers to build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

apply now

MivaTek Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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Career Opportunities

eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

apply now

American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

apply now

Career Opportunities

APCT
Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

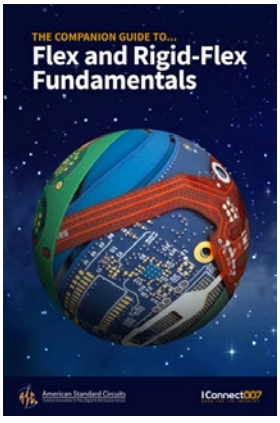
apply now

YOUR JOB AD HERE

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (PACIFIC)

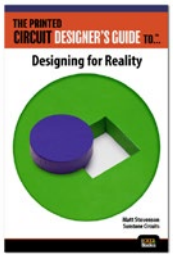
I·Connect007
GOOD FOR THE INDUSTRY

THE COMPANION GUIDE TO... FLEX AND RIGID-FLEX FUNDAMENTALS



I-Connect007 and American Standard Circuits are proud to announce the launch of the companion guide to the immensely popular *The Printed Circuit Designer's Guide to... Flex and Rigid-flex Fundamentals.* This short guide, written by topic experts at American Standard Circuits, is designed to provide additional insights and best practices for those who design or utilize flexible and/or rigid-flex circuit boards. Topics covered include trace routing options, guidelines for process optimization, dynamic flexing applications, rigid-to-flex transition and more. Visit I-007ebooks.com to download your copy.

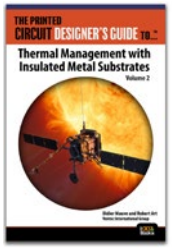
I-007eBooks The Printed Circuit Designer's Guide to...



Designing for Reality

by Matt Stevenson, Sunstone Circuits

Based on the wisdom of 50 years of PCB manufacturing at Sunstone Circuits, this book is a must-have reference for designers seeking to understand the PCB manufacturing process as it relates to their design. Designing for manufacturability requires understanding the production process fundamentals and factors within the process. **Read it now!**



Thermal Management with Insulated Metal Substrates, Vol. 2

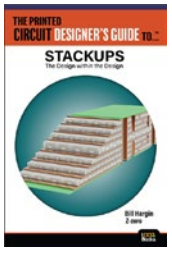
by Didier Mauve and Robert Art, Ventec International Group

This book covers the latest developments in the field of thermal management, particularly in insulated metal substrates, using state-of-the-art products as examples and focusing on specific solutions and enhanced properties of IMS. **Add this essential book to your library.**

High Performance Materials

by Michael Gay, Isola

This book provides the reader with a clearer picture of what to know when selecting which material is most desirable for their upcoming products and a solid base for making material selection decisions. **Get your copy now!**



Stackups: The Design within the Design

by Bill Hargin, Z-zero

Finally, a book about stackups! From material selection and understanding laminate datasheets, to impedance planning, glass weave skew and rigid-flex materials, topic expert Bill Hargin has written a unique book on PCB stackups. **Get yours now!**

Our library is open 24/7/365. Visit us at: I-007eBooks.com

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