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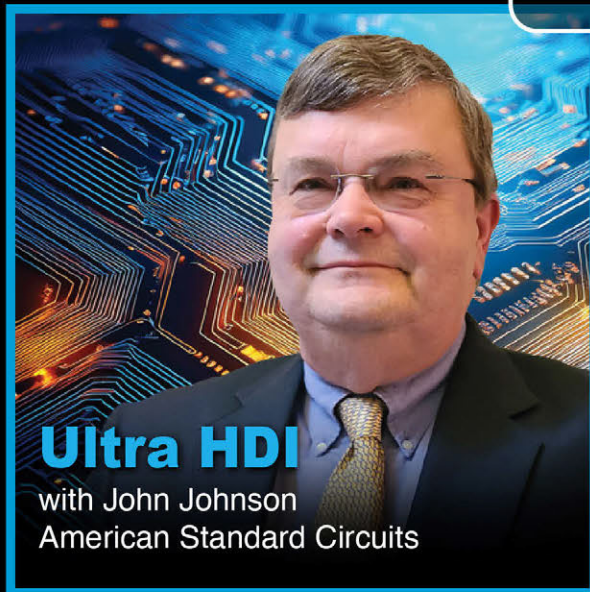
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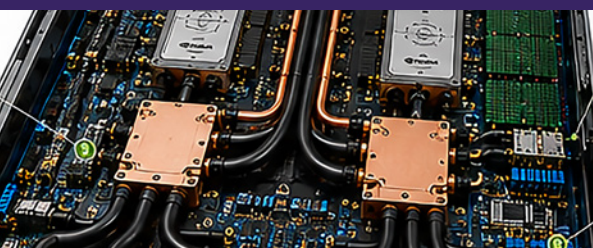
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From Ecosystems to Innovation

The industry's toughest challenges can't be solved in isolation. This issue explores how co-design, advanced PCB fabrication, AI infrastructure, materials selection, and flexible circuits create stronger products and better outcomes. From intelligent data transfer and HDI advancements to AI data centers and robotics, experts help us understand that better products begin with broader collaboration.

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The Power of the Electronics Ecosystem

BY MARCY LARONT, I-CONNECT007

Electronics hardware product design and manufacturing is a completely interconnected (pun intended) and interdependent system. Success depends on every part of the ecosystem functioning together, a reality that once seemed easy to ignore but today, few have the time or resources to work independently.

From co-design to innovation in HDI manufacturing and flexible circuits, these systems function best when we get out of our silos and more fully understand what it takes to get an idea or product to market.

AI data centers are perfect examples of connected systems in motion. These behemoths are engineering and technical marvels, but political hot potatoes in many states as governments and citizens wrestle with their environmental impacts and the rising cost of energy. This spring, I was hosted by Schneider Electric for a tour of TeraWulf, one of the nation's largest AI data center campuses. I also interviewed an executive from Motivair, which provides advanced liquid cooling and end-to-end thermal management systems specifically for AI



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data centers. You'll find my special section on that visit in this issue, which I believe demonstrates how relevant AI data centers are to our professional and personal lives. I'd love to get your feedback via [email](#) or [LinkedIn](#).

Our PCB design expert contributors embraced this month's assignment, offering a range of insightful and often creative metaphors to describe the PCB design ecosystem. From critters in the forest to a failed baton handoff in the 2020 Olympics, and even a drum major in a parade, we gain a clearer picture of the importance of an ecosystem, and find ourselves asking, "Why haven't we been doing this all along?"

Stephen Chavez of Siemens declares that his greatest successes came when "every stakeholder became part of the design process instead of becoming a reviewer of completed work." However, Kristin Moyer raises some concerns about data security in fully cloud-based systems, especially when working in classified settings. Being fully integrated will require some essential protocols yet to be determined.

In PCB fabrication, we revisit the idea of vertical conductive structures (VeCS), an alternate way to process HDI boards with very high layer counts and large form factors, using standard PCB processes and equipment. Joan Tourné of NextGin Technology developed VeCS in partnership with Wus, and writes about its continued development with R-VeCS and X-VeCS. Given where we find ourselves with HDI and packaging challenges, this is worth another look.

With a view toward advanced electronic packaging, Mike Carano explores pre-electroless causes of voids, which become far more likely with large motherboards and very high layer counts, as are

popular in 2.5D and 3D heterogeneous integration. GreenSource Engineering shares preliminary results from a study on agitation and copper balancing to achieve more uniform copper plating across large panels. PCBAA is discussing the National Defense Authorization Act (NDAA) and the mandate from the U.S. government to soon disallow PCBs from China, Russia, Iran, and North Korea. There's a deadline coming up quickly for commentary that you don't want to miss.

Finally, we focus on flex. I'm thrilled to have a new column from Flexible Circuit Technologies, kicked off by Dan Skweres, taking us through the familiar journey of "just because you can doesn't mean you should." Anaya Vardya of American Standard Circuits writes about the "cockroach" robot and how its "exoskeleton" is the flexible circuit itself. "The rigid-flex PCB that is simultaneously a skeleton, nervous system, and muscle interface may prove to be one of the most consequential engineering innovations in small-scale robotics," he writes. Really fascinating stuff!

I always enjoy putting together these issues at the confluence of legacy and innovation. Cherish these fleeting end-days of summer and take some time to enjoy reading through this month's magazine. **I-CONNECT007**



Marcy LaRont is the managing editor of *I-Connect007 Magazine* and executive director of IPC Publishing Group. Marcy started her career in PCBs in 1993 and brings a wide array of business experience and perspective to *I-Connect007*. To contact Marcy, [click here](#).

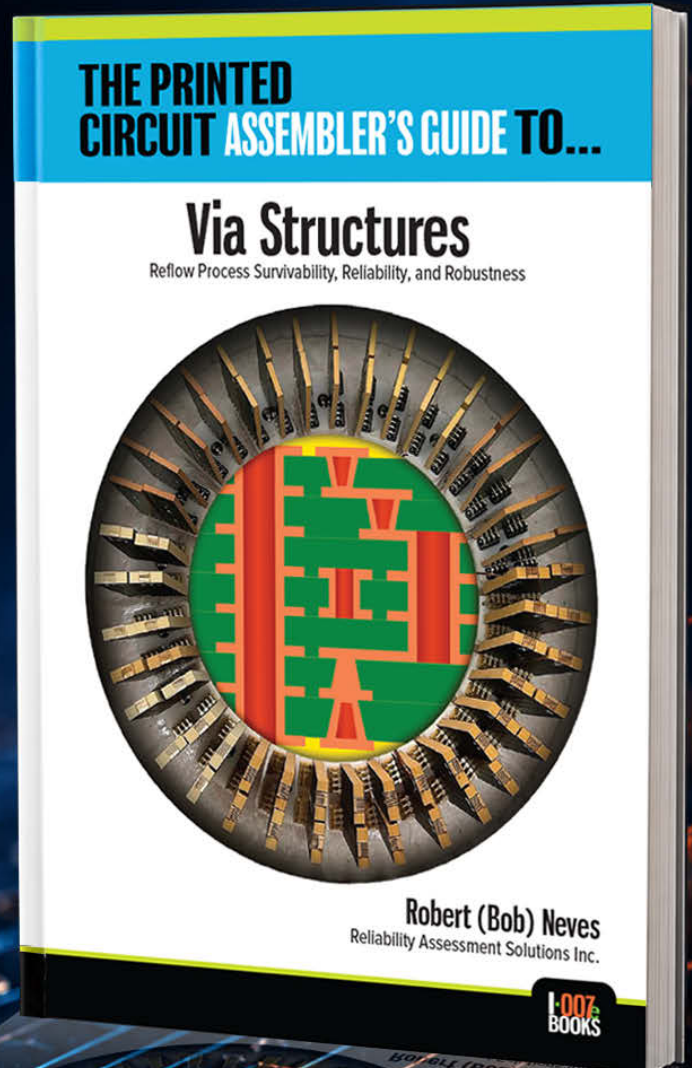
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Life in the Engineering Ecosystem



BY KELLY DACK, CIT CID+

A while back, I started thinking about the word ecosystem, a term that's become almost mandatory in discussions about electronics: the PCB ecosystem, the electronics ecosystem, and the design ecosystem. Is it more than an overused metaphor? What if it really is an ecosystem?

That question sent me down the kind of rabbit hole I enjoy. I started imagining electrical engineers, product managers, PCB designers, manufacturing and test engineers, supplier management, quality, and everyone else we work with fitting into the same kind of biological classification system we learned in high school.

It sounds a little odd (perhaps evidence I've spent too many years writing DFM analysis reports), but the analogy holds up surprisingly well. None of these disciplines survives in isolation. Like organisms in nature, each depends on the others, each contributes something essential, and when one

struggles, the whole system feels it.

As PCB designers, we can fall into the trap of thinking we're the center of the project. After all, without us, there's nothing to build or test. But really, we're just one specialized organism sharing a habitat with many others.

One purpose of this column is to remind us that our responsibility doesn't end when the CAM files leave our desktop. In many ways, that's where it begins. Every trace we route, footprint we approve, fabrication note we write, and dimension we place becomes the starting point for someone else's work. Manufacturing, assembly, inspection, test, procurement, and ultimately the customer all depend on the quality of that information.

A design succeeds not simply because it meets electrical requirements, but because every downstream stakeholder can build on it without breaking the chain.

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Nature Works the Same Way

A healthy forest isn't sustained by its tallest tree. It thrives because every organism, from towering pines to fungi beneath a fallen log, plays a role. Remove one critical link and the ecosystem suffers. PCB product development is no different.

The CAM package we release is more than Gerber and drill files, netlists, and fabrication notes. It's the information every downstream discipline needs to do its job well. When it's complete, accurate, and aligned with manufacturing, assembly, inspection, test, and supply chain requirements, each stakeholder adds value before passing the work along. The customer creates demand for the next generation of products, and the cycle begins again.

That's what makes an engineering ecosystem healthy, not the brilliance of any one discipline, but the strength of the connections between them.

Now here's where biology becomes more interesting than taxonomy. Classification tells us what something is. Ecology explains why it survives.

What do you see when you walk through a healthy

forest? You might see towering trees, birds singing, and squirrels chasing one another. Underneath your feet, you likely don't see the army of insects, fungi, and bacteria doing their work. Nobody puts termites on the cover of *National Geographic*, yet without them, the entire forest eventually collapses.

A fallen tree doesn't die. It becomes lunch. Fungi move in like the world's least desirable tenants. Ants and termites begin demolition. Birds arrive because there's now an all-you-can-eat insect buffet. Seeds are spread. New trees grow. Life continues because every organism contributes to something the next organism needs.

Now let's substitute "forest" with "PCB project." This time, a customer specification isn't the end goal; it's nourishment for the estimating team. Estimating feeds the quote, which "feeds" the planners and program managers. They feed the engineering team, which feeds the PCB designer, who then publishes the digital DNA—schematics, BOMs, fabrication drawings, Gerber and drill files, IPC-2581 or ODB++ data—that nourishes the fabricator's CAM

engineers. Then the ecosystem follows this order: CAM to procurement and material planning to manufacturing to assembly, then to inspection, test, and shipping. Finally, it arrives at the customer's dock, which feeds the marketplace, which in turn feeds the next specification.

Just like that, the entire ecosystem is ready to repeat the cycle.

Every successful handoff depends on the quality of the one before it. If Engineering hands Manufacturing a design that's incomplete, ambiguous, or impossible to build, the chain stumbles. Manufacturing has to improvise, and Inspection will struggle to verify. Test chases the symptoms instead of functionality. Ultimately, delivery slips, costs climb, and customers notice.

Nature has a term for organisms that can't adapt: extinction. Engineers have a different term: "Rev B."

Every deliverable we create becomes nutrients for someone else's

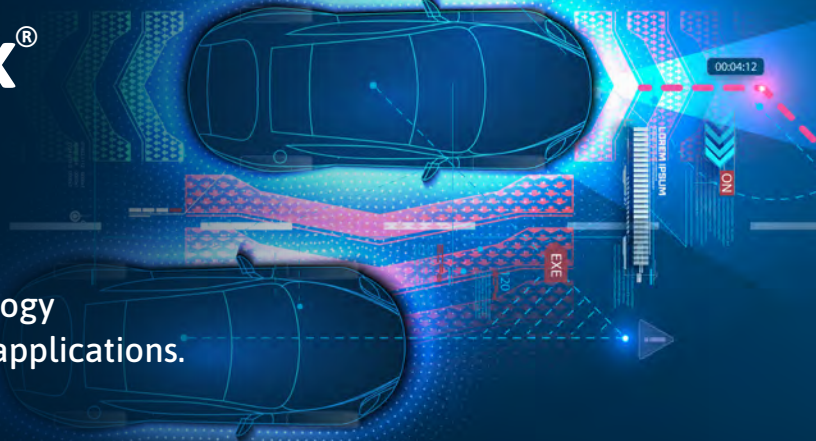
Table 1: How the PCB engineering food chain stacks up

BIOLOGICAL HIERARCHY	PCB INDUSTRY ECOSYSTEM
Domain	Technology and manufacturing ecosystem
Kingdom	Aerospace, defense, medical, automotive, telecom, industrial, consumer electronics
Phylum	Program management, systems engineering, electrical engineering, mechanical engineering, PCB design, manufacturing, quality, procurement
Class	RF, flex, HDI, signal integrity, assembly engineering, CAM, inspection, reliability
Order	Design teams, manufacturing teams, quality teams, supply chain
Family	PCB designers, electrical engineers, CAM engineers, fabricators, assemblers, inspectors, test engineers
Genus	Cross-functional product teams trying to get along before the next design review
Species	PCB designer

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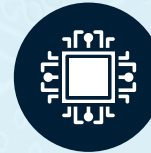
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job. A poorly organized schematic starves the layout designer. A careless footprint sends Assembly hunting for torches and pitchforks. Confusing fabrication notes leave CAM engineers performing something akin to an archaeological dig, trying to determine what the designer really meant. Missing tolerances become Quality's version of a murder mystery, and somewhere in Purchasing, a buyer discovers you've specified a laminate that hasn't been manufactured since disco was popular.



Nature has a term for organisms that can't adapt: extinction. Engineers have a different term: 'Rev B.'

The best PCB designers eventually discover that their real job isn't routing traces. It's understanding every organism downstream that's forced to consume whatever they produce.

Good designers learn enough electrical engineering to understand intent, and enough:

- Mechanical engineering to appreciate packaging
- Fabrication to know what can actually be built
- Assembly to avoid creating soldering nightmares
- Inspection to know what can actually be measured
- Procurement to avoid specifying parts obtainable only during a leap year under a full moon

But doesn't this concept apply to every member of the PCB project ecosystem? I think it does. As a PCB project "environmentalist," I am sensitive to the great void in communication I see between our industry species. We still do not seem to understand one another's roles, language, diet, function, and habitat.

For this reason, I've been compelled to put together some course content to help all of us in this PCB ecosystem understand each other's roles, communication, expectations, and deliverables. Keep an eye out for this upcoming offering by the Global Electronics Association: [From Blueprint to Build: A Survey of the PCB Design & Manufacturing Ecosystem](#).

Throughout this class, we'll leave our natural habitat from time to time. We'll wander into Manufacturing's territory. We'll visit CAM and observe Quality in its native environment. We'll peek into Assembly. We'll even attempt to communicate with Procurement, a fascinating species known to survive almost entirely on spreadsheets, supplier lead times, and coffee.

The class will venture into the PCB designer's lair, an unnecessarily dark and mysterious place where multiple monitors glow into the early hours and caffeinated beverages mysteriously disappear, to get an overview of how much of the digital DNA that nourishes the entire engineering ecosystem is created.

Along the way, we'll discover that every discipline has predators, natural enemies, survival instincts, and a unique role in keeping the project alive.

Because once you understand how every organism survives, you begin performing your own role with a new awareness. You stop seeing your deliverables as the finish line and recognize them as the nourishment the next organism needs to survive. You understand how your work influences every heartbeat throughout the ecosystem.

I hope you'll join me for this Association-sponsored class as we follow a PCB project from blueprint to build, and discover why every PCB project organism matters. **I-CONNECT007**



Kelly Dack, CIT CID+, specializes in DfX-driven PCB design and applications engineering at Pioneer Circuits, Inc. To read past columns, [click here](#).

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PCB Design Is a Team Sport (Revisited)

BY JOHN WATSON, PALOMAR COLLEGE

At the Tokyo 2020 Olympics, the U.S. men's 4x100-meter relay team of Trayvon Bromell, Fred Kerley, Ronnie Baker, and Cravon Gillespie was expected to contend for gold. With some of the fastest sprinters in the world, reaching the final seemed almost certain. Instead, the heavily favored team finished sixth in its qualifying heat and failed to advance, missing the final by just two-hundredths of a second. This massive disappointment was not due to a lack of individual speed but to a poorly executed baton exchange between Kerley and Baker, which forced both runners to slow down at the most critical moment.

Four exceptional athletes entered the race, but they did not perform as one connected unit. Their failure demonstrated an important lesson: Bringing talented individuals together and calling them a team does not automatically make them one. Individual ability cannot overcome poor coordination or a failed exchange.

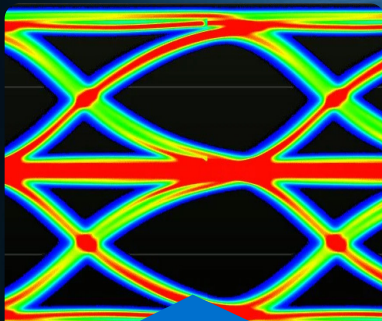
PCB development works much the same way. A company may assemble outstanding specialists, but if information and responsibilities are not exchanged effectively, even the most talented group can fail to reach the finish line.

During the COVID-19 pandemic, I wrote an article

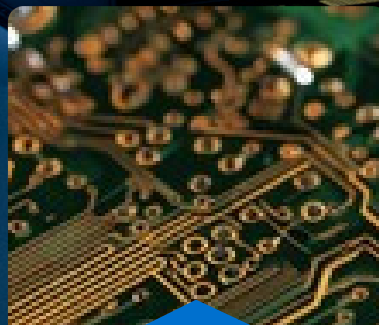
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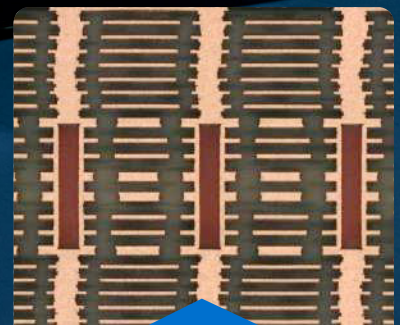
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for I-Connect007 titled “PCB Design... It’s a Team Sport.” The central insight was that successful PCB design cannot be achieved by one person working in isolation. Like a relay team, PCB development depends on electrical engineers, PCB designers, librarians, mechanical engineers, component specialists, manufacturers, assemblers, test engineers, and quality personnel combining their individual expertise. Each person performs a specialized role, but the product’s success depends on how effectively those roles work together. My insight was correct then and remains just as important today: PCB design is and always will be a team sport.

Today, as I look back, I realize that I did not take my idea far enough. I focused primarily on assembling the right people and encouraging them to cooperate as a team, failing to recognize that team members could still operate within separate departments, use disconnected tools, and move the design from one discipline to another through a series of handoffs. They might belong to the same team while still working in silos.

Even then, the PCB industry was moving beyond that traditional structure. The next step was not simply to improve cooperation among individual specialists, but to create an entire interconnected product development ecosystem. We even came up with a catchy little name for it: co-design. It just rolls off the tongue, doesn’t it?

Co-design describes a connected development process in which every discipline contributes its expertise early enough to influence the product. Instead of electrical engineering, PCB layout, mechanical design, sourcing, manufacturing, assembly, and testing working independently and passing the design from one silo to the next, they operate within a shared environment where information, decisions, and feedback flow in both directions. That is how it works—in theory.

Of course, I can already hear murmuring from my Altium friends in the back of the room: “Isn’t CoDesigner already a feature?” Yes, Altium CoDesigner supports collaboration between ECAD and MCAD. However, the co-design ecosystem I am describing is much broader. It connects not only PCB and mechanical designers but everyone involved in designing, sourcing, manufacturing, testing,

supporting, and improving the final product.

What I observed several years ago is still true, but our industry is now moving at the speed of a 2.4 GHz signal. PCB development has become too complex and fast-moving for traditional silos. Higher design densities, shorter schedules, tighter mechanical and thermal constraints, supply-chain instability, and increasing pressure for first-pass success have made late-stage handoffs too costly. At the same time, cloud platforms, shared data, and real-time collaboration tools have enabled earlier connections across disciplines. The industry did not suddenly discover collaboration; product complexity made the ecosystem necessary, and technology made it practical. That is the new reality of our industry.

Like our Olympic sprinters, PCB designers are among the best in the world at what they do. We possess tremendous individual skill, experience, and technical knowledge. But just as speed alone could not carry the U.S. relay team into the final, individual expertise alone cannot guarantee a successful product. Our next challenge is learning to apply that expertise within that cute little connected ecosystem: coordinating with other disciplines, sharing information earlier, and mastering the handoffs that turn outstanding individuals into a successful team.

So, how do we encourage the adoption and implementation of such a co-design ecosystem within our work environments? It begins by recognizing that co-design is not simply another software feature, management initiative, or project management system. It represents a fundamental change in how people communicate, make decisions, and measure success.

Build the Team Before the Design Begins

A co-design team begins by bringing together everyone whose decisions can influence the product: electrical engineering, PCB design, mechanical engineering, sourcing, fabrication, assembly, testing, and quality. Identify them before the design begins, define what each person contributes, and determine when their expertise must be incorporated into the process.

Give the team a shared objective, clear respon-

sibilities, and regular opportunities to identify concerns early. Invite fabricators and assemblers to critical design reviews rather than waiting until the files are released. Create an environment where team members feel comfortable challenging assumptions, identifying risks, and asking how a decision will affect the rest of the product.

The goal is to build better connections. Great co-design teams know who is carrying the baton, who will receive it next, and what must happen to complete every exchange successfully.

Connect Everyone Through a Single Source of Truth

That may sound like common sense, but fractures within a team often begin with the flow of information. The project starts with one baton. Then someone creates a second spreadsheet, another person saves a separate copy of the design, and an important decision becomes buried in an email. Before long, the team is carrying several batons and, like our ill-fated Olympic team, heading home without qualifying.

Just creating a single source of truth is not enough; the team must commit to using it. Assign ownership of the information, make it easily accessible, and establish clear rules for where files, requirements, decisions, comments, and revisions are maintained. Conduct reviews using the live source, record decisions there, and retire outdated files so they cannot quietly re-enter the project.

The principle is simple: If information affects the product, it belongs in the shared system, not in someone's inbox, personal folder, or memory. A co-design team succeeds when everyone knows where the baton is, whether it is current, and who is responsible for carrying it forward.

Turn Individual Expertise Into Shared Product Success

Some believe that such a co-design ecosystem diminishes individual expertise, but the opposite is true: It gives that expertise a greater purpose. The electrical engineer, PCB designer, mechanical engineer, sourcing specialist, fabricator, assembler, and test engineer each bring knowledge that the others may not possess. The goal is to connect that knowledge so every decision strengthens the complete product.



Some believe that such a co-design ecosystem diminishes individual expertise, but the opposite is true: It gives that expertise a greater purpose.”

That will require change (no matter how dreaded) and a change in how success is measured. Completing the schematic, layout, enclosure, or fabrication package should not be considered a victory if the product later experiences sourcing problems, manufacturing delays, test failures, or an expensive redesign. Success belongs to the entire team and should be measured by the final result: product performance, manufacturability, cost, schedule, reliability, and first-pass success.

Make this practical by establishing shared product goals at the beginning, reviewing risks as a team, and recognizing people who prevent problems even when those problems fall outside their immediate responsibilities. Encourage every team member to ask, “How will my decision affect the next person and the final product?”

The fastest individual runner does not win the relay. That's for the team that successfully carries the baton across the finish line. **I-CONNECT007**



John Watson is a professor at Palomar College, San Marcos, California and has recently added instruction at U.C. San Diego and U.C. Santa Cruz. To read past columns, [click here](#).

Four Lessons in *Engineering Judgment* for PCB Designers



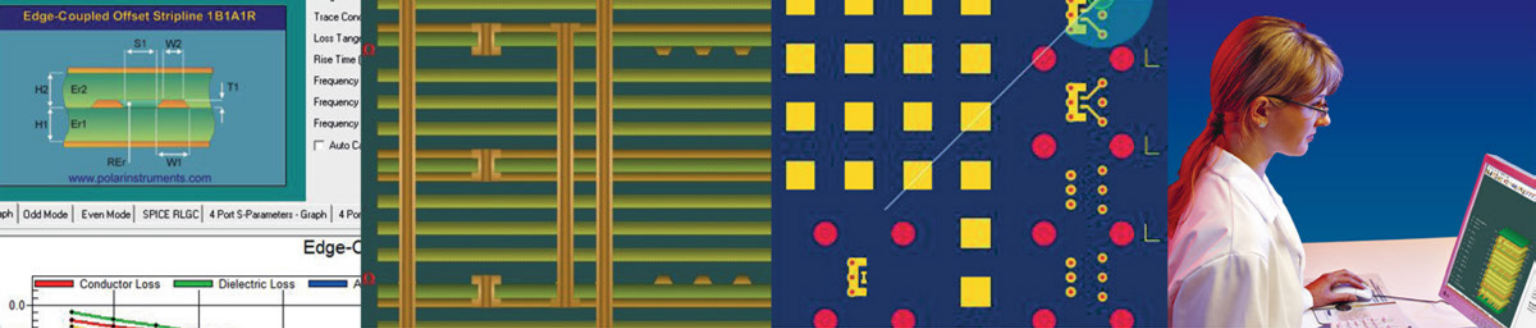
BY DAN SKWERES, FLEXIBLE CIRCUIT TECHNOLOGIES

Editor's note: This begins a new column series by Flexible Circuit Technologies, which will appear monthly in I-Connect007 Magazine. The column will feature five rotating authors who share expertise from their many years of working with flexible circuits.

In my more than four decades in the industry, I've watched design tools and manufacturing capabilities evolve in ways we could hardly have imagined when I started, touching everything from conventional rigid boards to today's highly sophisticated flexible and rigid-flex circuits. But anyone with meaningful experience in the PCB industry can relate to the phrase, "Just because you can doesn't mean you should."

Some of the advances I've seen have made us better engineers. Others have made it easier to create unnecessary complexity. Our CAD systems let us specify incredibly tight tolerances, route astonishingly dense designs, and call out requirements that were once impossible to manufacture. It's impressive, but using it wisely requires engineering judgment, something software can't provide.

Looking back over my career, where I have



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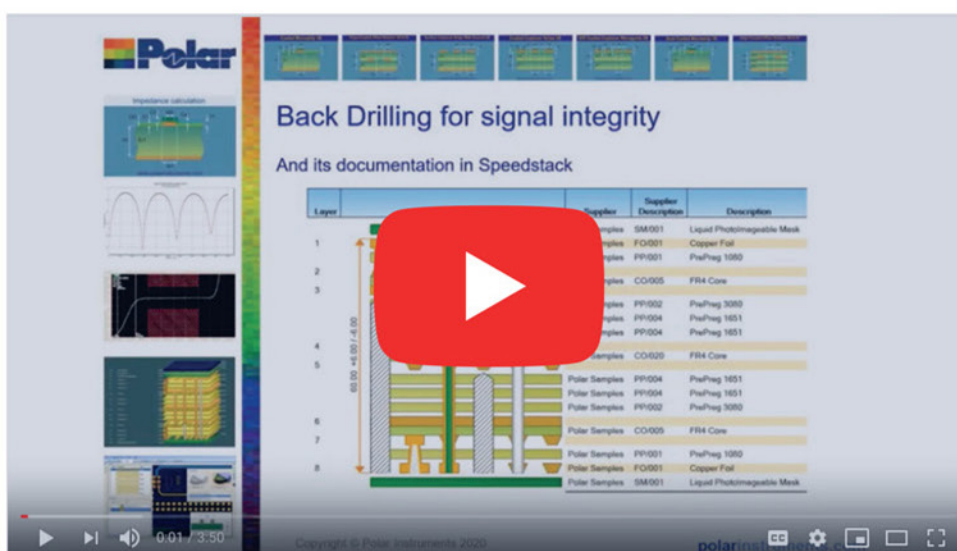
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worked in various PCB manufacturing environments, including production, prototype, and R&D, each setting provided distinct technical and process-related insights, and reinforcing the importance of anticipating downstream challenges and planning several steps ahead to ensure successful execution.

Thousands of PCB designs have crossed my desk over the years. Most have been practical manufacturing designs with requirements aligned to available process capability. Others, however, included specifications and layout decisions that were difficult to justify from a manufacturing standpoint.

Here are a few examples that illustrate the “just because you can doesn’t mean you should” idea.

From Tape to CAD

When I started, PCB artwork was created with tape on enlarged layouts. Every change took time and effort, so designers naturally thought carefully before making one. You didn’t make a design more complicated unless there was a good reason.

Today’s software allows us to make changes almost instantly, which is an incredible advantage. But that same convenience also makes it easy to add complexity without stopping to ask whether it’s necessary.

But just because your software lets you route one more trace through a congested area doesn’t mean that’s the best engineering solution. Sometimes moving a component or changing the stackup creates a board that’s easier to manufacture, easier to inspect, and ultimately more reliable.

Tolerances

One example I’ve seen many times is dimensional tolerances. Designers can specify incredibly tight positional tolerances for connector holes, pads, and other critical features. I’ve seen flex designs where every bend area carried unnecessarily tight fabrication requirements. Sometimes that’s exactly what’s needed.

But just because you can specify a tighter tolerance doesn’t mean the product requires it. Every tighter tolerance limits your manufacturing options. It may increase cost, extend lead times, and reduce the number of suppliers capable of building the board, all without improving how the product actu-

ally performs.

That same principle applies to highly dense routing combined with fabrication requirements that only a limited number of suppliers can meet. While modern layout software makes extremely challenging designs possible, those decisions must still be evaluated against program cost targets, schedule constraints, and practical manufacturability.

IPC Class 3

I see the same thinking when IPC Class 3 gets specified. It’s easy to assume that asking for the highest level of workmanship automatically produces the best board.

But just because you can specify Class 3 doesn’t mean your application benefits from it. Class 1 applies to products for which the primary requirement is the basic function of the completed assembly. Class 2 applies to products that require continued performance and extended service life, where uninterrupted operation is desired but not mission-critical.

If the product truly requires a Class 3 high performance/harsh environment, then it’s absolutely the right decision. But if the product is really a Class 2 application, you’ve added inspection, documentation, testing, and cost without adding value to the customer. Class 3 generally carries the highest fabrication and verification cost, and it can extend lead time depending on the qualification and inspection requirements imposed.

This becomes especially important in flex and rigid-flex designs, where manufacturing complexity is already higher than in conventional rigid boards.

Each IPC class establishes distinct acceptance criteria, including annular ring dimensions, copper plating thickness, and allowable feature-level anomalies such as nicks, pits, and other discontinuities.

Working With Flex

Flexible circuits allow us to do some remarkable things today. We can create incredibly dense rigid-flex designs with multiple bend areas, exotic materials, and complex constructions.

But just because a design can be built doesn’t necessarily mean it should be built that way. Sometimes a slightly larger bend radius, a simpler layer

count, or a different material selection creates a product that's easier to manufacture and more reliable in the field.

Final Thoughts

Looking back over 40 years, I've learned that good engineering isn't about pushing every design to the limit of today's technology. I want to understand the product's requirements and make decisions that support them. The best designs achieve the right balance of performance, reliability, manufacturability, and cost. Input from a capable fabricator can reduce total program cost by aligning material selection and fabrication methods with the actual functional requirements of the design.

Every time I review a design, I find myself coming back to this simple reminder: Just because you can doesn't mean you should. It's a lesson that has served me well throughout my career, and one that's just as relevant today as it was when I first entered this industry. **I-CONNECT007**



Dan Skweres is a senior applications engineer for Flexible Circuit Technologies.

BELOW THE SURFACE

Why Thermal Failure Is Still the No. 1 Killer in Power Electronics

BY CHANDRA GUPTA, REMTEC

Why do power electronics fail? There's a range of answers, from overvoltage and mechanical stress to poor assembly and environmental exposure. If you ask your favorite AI search engine for an answer, you'll get a pretty simple response: excessive temperature leads to component degradation, material breakdown, and eventual failure. In a sense, that's true, but it's oversimplified and incomplete. The real issue is thermal management failure at the system level. Heat is still the number one killer, and most of the time, you don't even realize it's there.

The Hidden Thermal Bottlenecks

I don't think engineers are ignoring heat. They're actually misjudging where the heat is. We tend to focus on obvious hotspots: power devices, MOSFETs, and IGBTs. We add heatsinks, fans, maybe even liquid cooling. But here are some hidden bottlenecks:

- Interfaces between materials
- Solder joints with poor thermal conductivity
- Die attach layers that trap heat
- PCB dielectric materials that resist heat flow
- Copper thickness that spreads current—but not heat—effectively

These bottlenecks are subtle resistances in the thermal path, and those small resistances compound. Heat just needs a place where it can't escape fast enough, and that's where degradation begins.

Why PCB-based Designs Hit a Ceiling

Traditional PCB materials, especially FR-4, were never designed for high-power thermal performance. They were designed for manufacturability, cost efficiency, and electrical insulation. Secondary to that was thermal conductivity.

In low- to moderate-power systems, this works fine. But as power densities increase, especially in EV, aerospace, and RF applications, we start to see a hard limit. You can only push so much heat through a material that fundamentally resists heat flow. At that point, no amount of heatsinking can compensate for what's happening inside the structure.

Engineers hit a ceiling, so they work to optimize the cooling system, but the real bottleneck is embedded in the substrate itself.

[Continue reading here.](#)



Designing for a More *‘Intelligent’* and *Connected* Future

With more collaborative and computationally demanding PCB designs, cloud-based workflows are rapidly moving from possibility to reality. But greater connectivity also raises new questions about data security, intellectual property, and the sharing of design information in an increasingly complex electronics ecosystem.

In this interview, Kristin Moyer of the Global Electronics Association explores the benefits and challenges of cloud-based design environments, the growing importance of standardized data transfer

protocols such as IPC-1751 and IPC-2581, and why a secure, intelligent data ecosystem will be essential for the future of co-design, automation, and advanced electronics manufacturing.

Marcy LaRont: Kristin, cloud-based design environments are becoming a much bigger part of the PCB design ecosystem. What is driving that shift?

Kristin Moyer: Cloud-based environments offer greater processing power, storage, and the ability for teams to work together across locations. One

A person in a yellow shirt is sitting on a suspension bridge that spans a deep valley with a lake. The background features snow-capped mountains under a sunset sky. An orange speech bubble is overlaid on the image.

Hmm... If I have a **conductor width and isolation distance of 40 μm (1.5 mils)**, does that mean my **PCB is considered Ultra HDI?**

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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example of this is Altium, which has indicated it intends to make cloud-based workflows its primary operating model over time, though it will maintain some desktop presence. The ECAD/MCAD design ecosystem must necessarily become more collaborative, and so the cloud-based/web application interface is more desirable.

Though this is increasingly where we are going, there are security concerns. What are the downsides of a cloud-based environment for design?

Before we talk about the drawbacks, it's important to distinguish between cloud storage and a true cloud-based design environment. Today, many companies store their design files in the cloud while the CAD software runs on a local workstation. In a cloud-based design environment, both the software and the design data reside in the cloud, so you're accessing the design tools over a network.

So, the most obvious downside of a cloud-based system is that you are now network-dependent, which raises significant concerns about data security. Being cloud-based means you are vulnerable to penetration from an outside source.

Another problem involves access, particularly in secure test facilities. If you're at a government site that sits in the middle of nowhere, or you're at a rocket launch site and there are network connectivity issues, how will you access your design?

How is that situation handled right now?

The product data management system we use now allows you to check out a design, make edits, and check it back in, which provides revision control. With cloud-based storage, you bring the data down onto your own computer, and even if you're off the network, you can still access the design tools, or at least the ones that are not network-dependent.

So, despite legitimate reasons for more cloud-based systemization, it sounds like we are less secure inside the cloud.

Yes, the more accessible the design, the less security it has, even with encryption. Anything connected to the network is more vulnerable to external intrusion. If the application requires a physical license key to run a machine and you can disconnect it from the network, the application can only be accessed

on that machine. Historically, it has been shown that the less access to a file, the more secure the data.

Both IP and ITAR, as well as other classified and highly sensitive information, require strict access, and more restrictions can be added to a physical machine that is not connected to a network.

Can you give an example? What is your personal experience with this?

I previously worked for a U.S. military and aerospace company with dedicated laptops and computers. Some machines were allowed to connect to the internet, and others were in secure areas that were not allowed to access the internet. Everything was transferred on specifically encrypted USB drives, and certain security protocols still had to be followed.

ECAD and MCAD vendors are addressing this issue in various ways. Do you see a tool vendor adopting a solely cloud-based system in the near future?

Without speaking for Altium directly, I believe they will approach it the way they have with their other server applications. Nexus will be part of Altium 365, but on a closed intranet.

As we add more capabilities to the tools and increase the complexity of the designs themselves, we're exceeding the processing capacity of single-processor computers. Therefore, it makes sense that some CAD tool providers may aspire to an open, internet-based, cloud-based operating environment as their primary market.

For secure facilities, such as military, aerospace, medical, and other sectors with very sensitive IP and data security requirements, a custom solution will be created. But it stands to reason that tool providers will want as many internet users as possible to harness its processing power to achieve these larger, more complex designs.

In the case of Altium, it is owned by Renesas, a silicon design company. Integrating silicon design with board design requires significantly more processing capability—Apple's M1 Ultra chip has 114 billion transistors, for example, and you need a lot of processing power to do that kind of layout. Therefore, it stands to reason we are seeing a big push from them on this front.



Hmm, what is recommended
**minimum distance for
copper to board edge?**

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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Protocols for Data Transfer

We've been hearing more about IPC-1751 and IPC-2581. What problems are these standards designed to solve, and do they help with what we have been discussing?

Making sure everyone in the design and manufacturing ecosystem is working from the same information has always been a significant challenge. These newer data transfer methods, such as IPC-1751 and IPC-2581, provide a more secure way to transfer electronic design data because the files can be fully encrypted and all of the information is contained in a single data package.

They also provide the benefit of clarity of information and intent between the PCB designer and the rest of the manufacturing ecosystem. Having people read a set of notes and interpret them is asking for trouble. With these standards, the design requirements are built directly into the electronic data so that machines have everything they need.

That becomes even more important in connected factories and Factory 4.0 or 5.0 environments. Instead of requiring an operator to do a great deal of programming up front, you feed the data directly into the machines, which are automated enough to run from that standardized information.

Is this reflected in the whole product ecosystem?

Yes, again, it gives that clarity of intention without the need for interpretation. Gerber and ODB+ are the two industry-standard formats for packaging and sending PCB design data to fabricators and EMS vendors, and both contain a lot of useful data. But I once had a bug in the ODB+ data exporter that the software could not detect. The data came out with a short across a point, and if the boards had been built to that data, they would have been scrap, wasting a lot of time and money. The new, standardized data transfer protocol eliminates this possibility.

It contains all the materials information for the fabricator and the temperature profiles for the assembler, including solder fluxes and test information. All the ecosystem data is in a single file, which you can encrypt and transfer.

How does it remove the opportunity for human error?

It provides consistency, accuracy, and data security. Your entire recipe is stored securely in a single file. To get human interpretation out of the ecosystem, you have pure data and clear intent.

This feels very timely, so why hasn't the IPC-1751 data transfer protocol been more widely adopted?

There are a few reasons. Some engineers will say, "This is just the way we do things." To change that mindset, there needs to be training and knowledge transfer to the design side of the ecosystem. The message needs to be that it is desirable and necessary. You have to overcome that cultural mindset.

The other issue is with the CAD tools themselves, with multiple tools and methods needed to read, interpret, and manipulate the data from all sides of the ecosystem. Even with a standard, it takes time for the ECAD and MCAD tool communities to implement the changes, but it's a critical variable for wide adoption and use.

Regardless of some of the challenges, is IPC-1751 an inevitability where data transfer and security are concerned?

Yes, having secure data transfer such as what is stipulated in IPC-1751 is inevitable, much as I believe going to cloud-based design systems is inevitable. That will be one of the big drivers toward standardized data transfer implementation.

How does co-design factor in here?

Having a universal data format will be necessary for successfully implementing co-design and cloud-based storage and design methodologies. For co-design to be a functional reality, the CAD ecosystem—ECAD, MCAD, and physics modeling—with different file formats, must be overhauled. The only way we successfully implement a harmonized environment for development design is with a new intelligent data format structure that can actually move between all these parts of the ecosystem without the need for human intervention or interpretation.

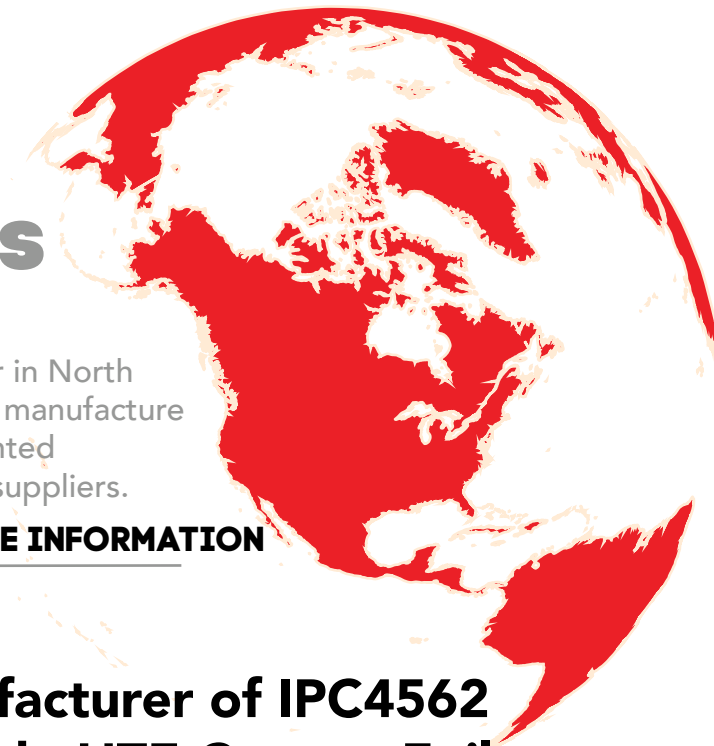
Well said, Kristin. Thank you.

Thank you, Marcy. I look forward to being part of the future. **I-CONNECT007**

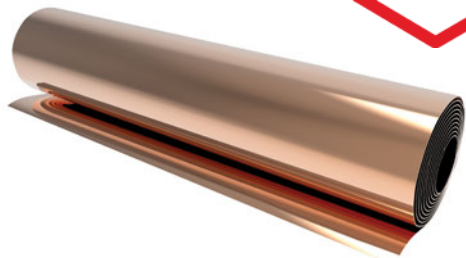
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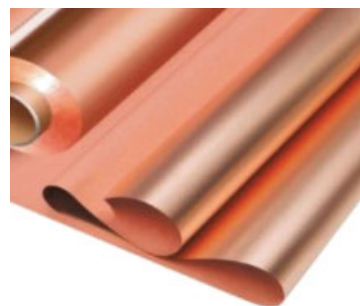


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Beyond DFM

PCB Design and Manufacturing as a Cooperative Effort

BY JOE FJELSTAD

The concept of co-designing PCBs by incorporating input from all areas of manufacturing has grown significantly over the past several years, bringing a sharper focus on the early contributors to a collaborative electronic system.

From those pioneers, we have learned that the PCB is no longer simply the platform on which a design is manifested; it is now an active part of the electrical, thermal, mechanical, and economic architecture of the product. As operating frequencies rise, component pitches shrink, power densities increase, and product schedules tighten, decisions made by one discipline can no longer be isolated from the consequences they create for others.

In my past PCB workshops, I have referred to PCB designers as the “drum majors” of the industry.

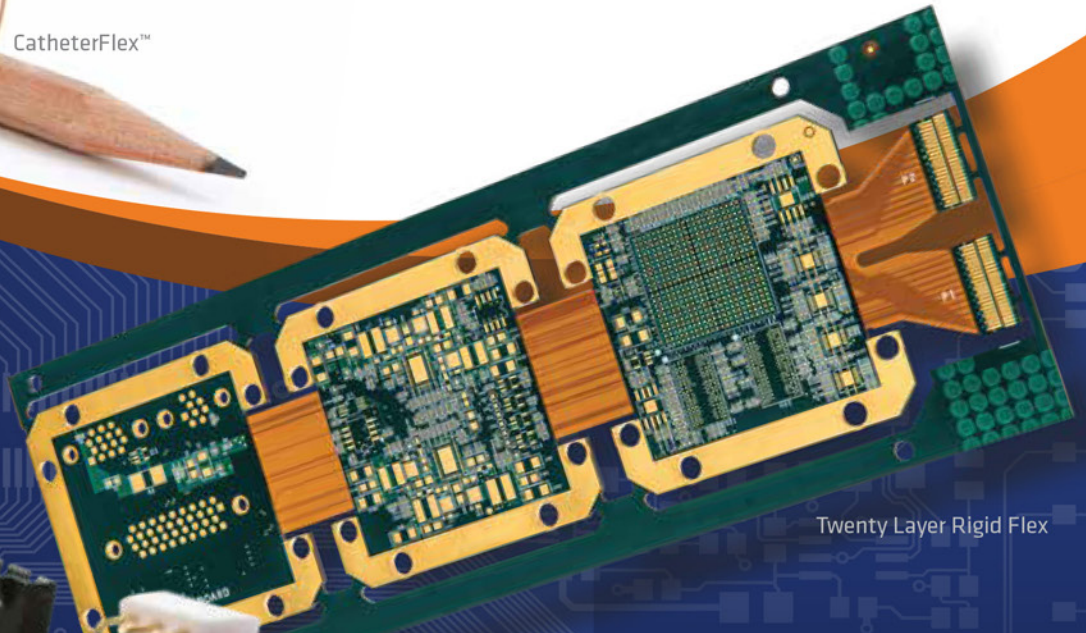
They lead the electronic manufacturing “parade” and the decisions by designers can make the difference between stirring marching music and chaotic cacophony. Yes, the designer must still translate logical component connectivity into a manufacturable physical structure, but that task requires earlier access to system requirements, greater awareness of manufacturing capabilities, and continuous interaction with specialists who once entered the process much later.

A central question, in my opinion, is whether this evolution will simply lead us back to another discussion of DFM or whether the industry is ready to recognize that successful PCB development depends on something broader that integrates the process and its executors to create perfect or

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near-perfect printed circuit assemblies every time. Don't misunderstand me. DFM remains essential and won't go away, but as I've written about in past columns, DFM alone is not designing with manufacturing (DWM); it is not cooperative design.

PCB Project Steps

Every PCB project has a natural process hierarchy, whether the organization formally recognizes it or not. There are myriad elements to the process, starting with program management, which defines the product objectives, including the usual suspects: size, weight, cost, schedule, performance, reliability, regulatory obligations, expected production volume, acceptable risk, and others. These requirements inevitably flow down to the team of individuals responsible for turning the concept into a working product.

In the PCB design environment, the work branches into several distinct but interdependent families of activity, including design-rule development, logical design and schematic capture, component selection, box design, material selection and stackup, component placement and routing, signal and power integrity analysis, HDI planning, documentation and configuration control, thermal consideration, and many others, often product-specific considerations. You probably have your own concerns to add to the list here.

Each of these activities often has its own terminology, analytical tools, constraints, and measures of success. Yet, importantly, none of these activities can or should operate independently. A decision that optimizes one activity may well create serious difficulties elsewhere.

Here are some examples that might help. A smaller component may reduce total PCB area but may require finer fabrication features, which can limit the number of potential vendors. A lower-loss laminate may improve RF performance but create procurement or processing challenges. A buried-via structure may simplify routing while increasing fabrication complexity, inspection difficulty, and cost. A mechanically convenient connector location may force longer high-speed routes or disrupt the power-distribution network.

It must be conceded that, at times, overall require-

ments make such decisions unavoidable. Ultimately, the project's success or failure often hinges on whether these decisions are considered together.

The PCB Designer as Drum Major

The PCB designer, like the drum major, is uniquely positioned within the hierarchy, as nearly every project requirement eventually becomes a physical constraint on the board.

Electrical intent becomes placement, routing, impedance, spacing, and return-path requirements. Mechanical intent becomes board outlines, keep-out regions, mounting features, connector positions, and component-height restrictions. Thermal requirements become copper distribution, thermal vias, heat spreaders, airflow considerations, and component separation. Manufacturing requirements become feature sizes, annular rings, aspect ratios, material selections, panel-utilization choices, and process tolerances.

The PCB database is like a musical score, where these otherwise separate engineering intentions meet.

This does not mean that the PCB designer should be expected to independently solve every electrical, mechanical, manufacturing, and reliability problem. Like the drum major, it is not his role to play every instrument; the PCB designer ensures that all band members know the music and follow instructions to create a satisfying musical experience. The designer must have timely access to the people who own those problems.

I was discussing this with a well-known and respected friend in the industry, who observed that one should not ask a piccolo player to sound like a tuba. He was spot on!

Too often, real collaboration begins only after the layout is substantially complete. At that point, the manufacturing engineer reviews the design for fabrication concerns, the assembler checks component clearances and solderability, the SI specialist identifies problematic interconnects, and the mechanical team discovers enclosure conflicts. Unfortunately, you get a predictable result: redesign, schedule pressure, strained relationships among team members, and too often, costly compromises that don't always deliver on their promises. The

argument here is that earlier collaboration changes the process from error correction to much more cost-effective error prevention.

Some Thoughts on RF and HDI

RF and HDI designs are often treated as specialized classes within the larger PCB discipline. That classification is useful, but it can also create artificial boundaries.

We have learned through hard lessons that RF performance depends not simply on trace geometry, but also on laminate properties, base copper roughness (top and bottom), plating thickness and uniformity, connector selection, fabrication tolerances, and assembly consistency, along with other more arcane concerns. The RF designer, PCB designer, material supplier, fabricator, and test engineer must therefore participate in a shared and interactive design process.

HDI (and now more frequently UHDI) presents a similar challenge. Microvias, sequential laminations, few-micron lines, few-micron-thick dielectrics, microvia-in-pad structures, and stacked and/or staggered interconnects collectively expand routing capability, but they also affect cost, yield, reliability, and perhaps most importantly, supplier availability. There are simply not that many suppliers for such a product, especially in North America.

An HDI architecture cannot be responsibly selected solely because it makes routing easier. Nor should it be rejected solely because it appears more expensive on a per-panel basis. The architecture must be evaluated, again in terms mentioned earlier, in the context of total product size, layer count, assembly methods, yield, electrical performance, testing, reliability expectations, and production volume.

This same principle applies to almost every advanced PCB technology. Its value cannot be understood from the perspective of a single discipline; thus, manufacturing must become a true design participant, not an observer.

Conclusion

Manufacturing is frequently positioned at the end of the design chain, where its role is to determine whether the completed design can be built. This is the traditional home of DFM. Sadly, the fabrica-

tor is only asked to approve or reject a finished design and is being used as an inspector rather than as an engineering resource. They can offer so much more.

Experienced, top-tier fabricators are invaluable resources, possessing detailed knowledge of material behavior(s), registration capabilities, drilling and plating limits, imaging processes and their limitations, material movement during lamination, copper distribution concerns and recommendations, impedance control, and myriad other potential defect mechanisms. In addition, and not yet covered but very important, assembly specialists understand stencil design, solderability, package behavior, component warpage, thermal profiles, cleaning constraints, rework risks, and inspection limitations. That combined knowledge (manufacturing and assembly) provides its greatest value before the design architecture is fixed, which nicely sums up the purpose of this (hopefully) brief commentary.

At the end of the day, unless we collectively understand the limitations of DFM and the potential of DWM, we will continue to miss the target. DFM asks whether a design can be manufactured. DWM teaches how a product can be jointly optimized for performance, manufacturing, assembly, reliability, inspection, cost, supply resilience, and lifecycle support. In short, DFM rules are applied to the design, and DWM, or co-design, shapes the design to get it right the first time. The distinction is fundamental. **I-CONNECT007**



Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185

patents issued or pending. To read past columns or contact Fjelstad, [click here](#). Download *Flexible Circuit Technology, 4th Edition*, and watch Fjelstad's in-depth workshop series "[Flexible Circuit Technology](#)."



WHO REALLY DESIGNS THE PCB?

“Who designs the PCB?” sounds like a simple question, but it assumes there’s a simple answer. In reality, every discipline involved in product development, from electrical and mechanical engineering to manufacturing and procurement, has a hand in designing the PCB. Today’s products are created through constant collaboration among multiple engineering disciplines, each influencing decisions that affect performance, manufacturability, cost, and reliability.

A Significant Evolution

The PCB designer has not simply gained access to better tools, more automation, and/or sophisticated design methodologies. The role itself has changed. A discipline primarily focused on translating electrical connectivity into physical layout has become a critical integration point where electrical performance, mechanical constraints, manufacturing capability, supply chain realities, and product reliability must all converge.

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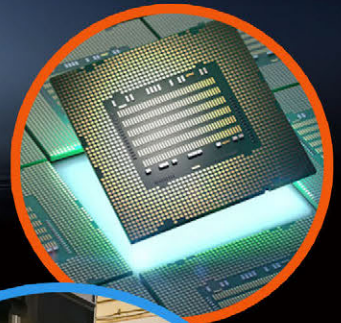
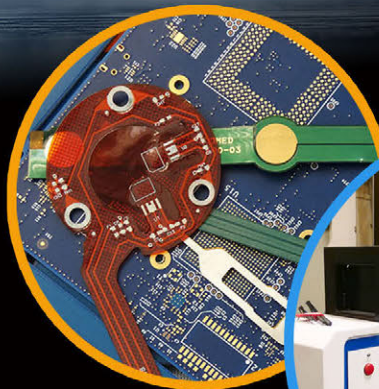


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Design for assembly, design for test, design for reliability, design for cost, and design for supply chain are not separate activities competing for attention. They are interconnected perspectives that contribute to the overall health of the engineering ecosystem.”

The reason is that electronic systems have become too complex for any single discipline to optimize independently. Modern designs are a combination of high-speed digital interfaces, RF functionality, advanced packaging, power delivery challenges, thermal constraints, HDI structures, and global supply chains, all of which can change throughout the product lifecycle.

For example, I've seen that a decision made by one engineering group rarely remains isolated. A component choice might influence placement, via technology, routing, thermal performance, manufacturing complexity, and long-term availability. In other situations, a stackup decision could affect SI, power integrity, cost, and fabrication yield. A mechanical change can create electrical consequences that were never considered during the original architecture. The PCB has become the physical point where these competing requirements meet.

In the past, product development often followed a sequential path where each discipline contributed its expertise, but often only after the previous discipline had completed its work. But what I've found is that the earlier the conversations happen, the fewer problems have to be fixed later.

My most successful projects weren't because a final design review discovered every possible issue before manufacturing. They succeeded because the right conversations happened earlier in the process. Manufacturing engineers influenced fabrication decisions before the routing was

complete. Mechanical engineers would collaborate during placement, rather than after the board was constrained. SI analysts shaped routing strategies before critical nets became too difficult to modify. Procurement teams identified component risks while alternatives were still available.

The difference was that every stakeholder became part of the design process rather than a reviewer of completed work. This is where the concept of an engineering ecosystem becomes so important.

Everyone Contributes in a Healthy Ecosystem

No single organism operates independently, and the stability of the system depends on the relationships between all participants. Engineering organizations function in the same way.

- Program managers establish business objectives, schedule, and priorities
- System architects define the technical vision
- Electrical engineers establish functionality
- Mechanical engineers define physical realities
- Manufacturing engineers ensure producibility
- Quality teams establish reliability expectations
- Procurement teams manage supply chain considerations

PCB designers integrate these requirements into a physical implementation. The success of the product depends on how effectively these disciplines interact.

Within this ecosystem, the PCB designer does not replace the expertise of other disciplines, nor should they be expected to become an expert in every engineering specialty. Instead, their unique value comes from understanding how decisions create interaction and recognizing when collaboration is required.

Every placement decision affects thermal behavior, manufacturability, SI, test accessibility, and mechanical integration. Every routing strategy involves tradeoffs between performance, cost, complexity, and reliability. The designer becomes the person who helps translate system-level intent into a physical product that can actually succeed in the real world.

This broader responsibility is especially evident as we see more diversity in PCB design. HDI technologies require closer collaboration with fabricators and process engineers. RF designs require deeper interaction with electromagnetic specialists. High-speed digital systems demand careful consideration of return paths, impedance control, timing, and power delivery. Flexible and rigid-flex designs introduce mechanical reliability concerns that extend far beyond traditional layout practices. The days when a designer could work independently within the boundaries of a CAD environment are disappearing because the product itself no longer allows it.

This does not mean DFM has become less important. Quite the opposite. It remains one of the most essential disciplines in successful PCB development. However, its role has expanded. Manufacturing is now a partner that helps shape better designs from the beginning.

The same principle applies across the entire product lifecycle. Design for assembly, design for test, design for reliability, design for cost, and design for supply chain are not separate activities competing for attention. They are interconnected perspectives that contribute to the overall health of the engineering ecosystem.

Change Your Mindset

Today's organizations are moving away from isolated engineering processes and toward connected workflows where information flows continuously between disciplines. Digital engineering environments, simulation, automation, and emerging AI capabilities will continue improving this collaboration by making design intent and engineering data more accessible throughout the lifecycle. However, technology alone will not create better products.

The greatest advantage will come from engineering judgment, experience, and collaboration. Tools can help identify possibilities, analyze performance, and automate repetitive tasks, but they cannot replace the conversations that occur when experienced engineers challenge assumptions, share knowledge, and solve problems together.

Ultimately, that may be the most important lesson from the evolution of PCB design. The future of our profession will not be defined by how quickly we can create layouts or how many design rules we can automate. It will be defined by how effectively we connect engineering disciplines and preserve the intent behind every decision.

So, who really designs the PCB? The answer is that the PCB is designed by an ecosystem of engineers, specialists, manufacturers, suppliers, and stakeholders who contribute their expertise throughout the development process. The PCB designer remains central to that ecosystem, not because they own every decision, but because they help bring those decisions together into a successful product.

The best products emerge when every participant understands that they are not designing an individual piece of the system; they are helping create the system itself. **I-CONNECT007**

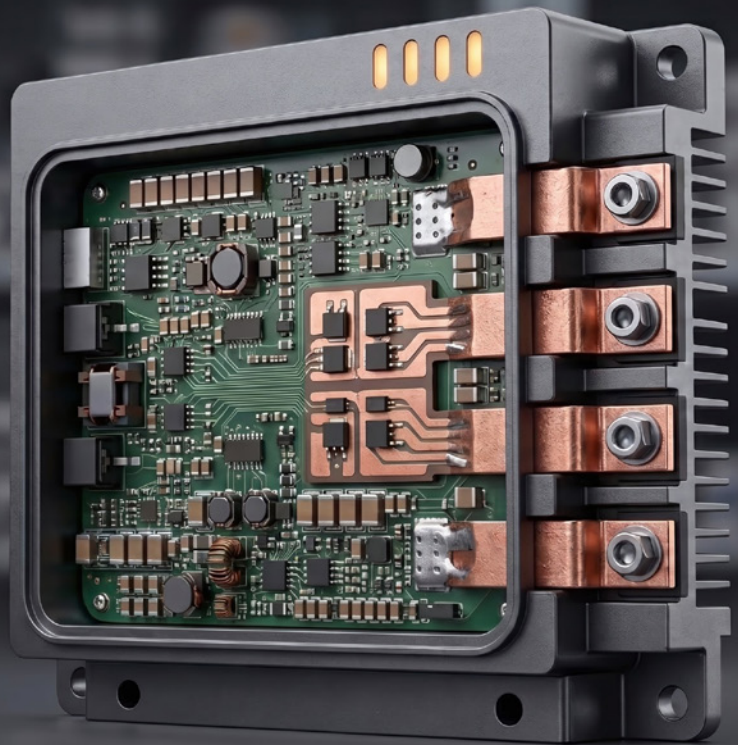


Stephen V. Chavez is principal technical product marketing manager at Siemens EDA and chair of PCEA.

From Substrate to System

The Power Module Assembly

SPOTLIGHT ON
Assembly



BY BRIAN BUYEA, REMTEC

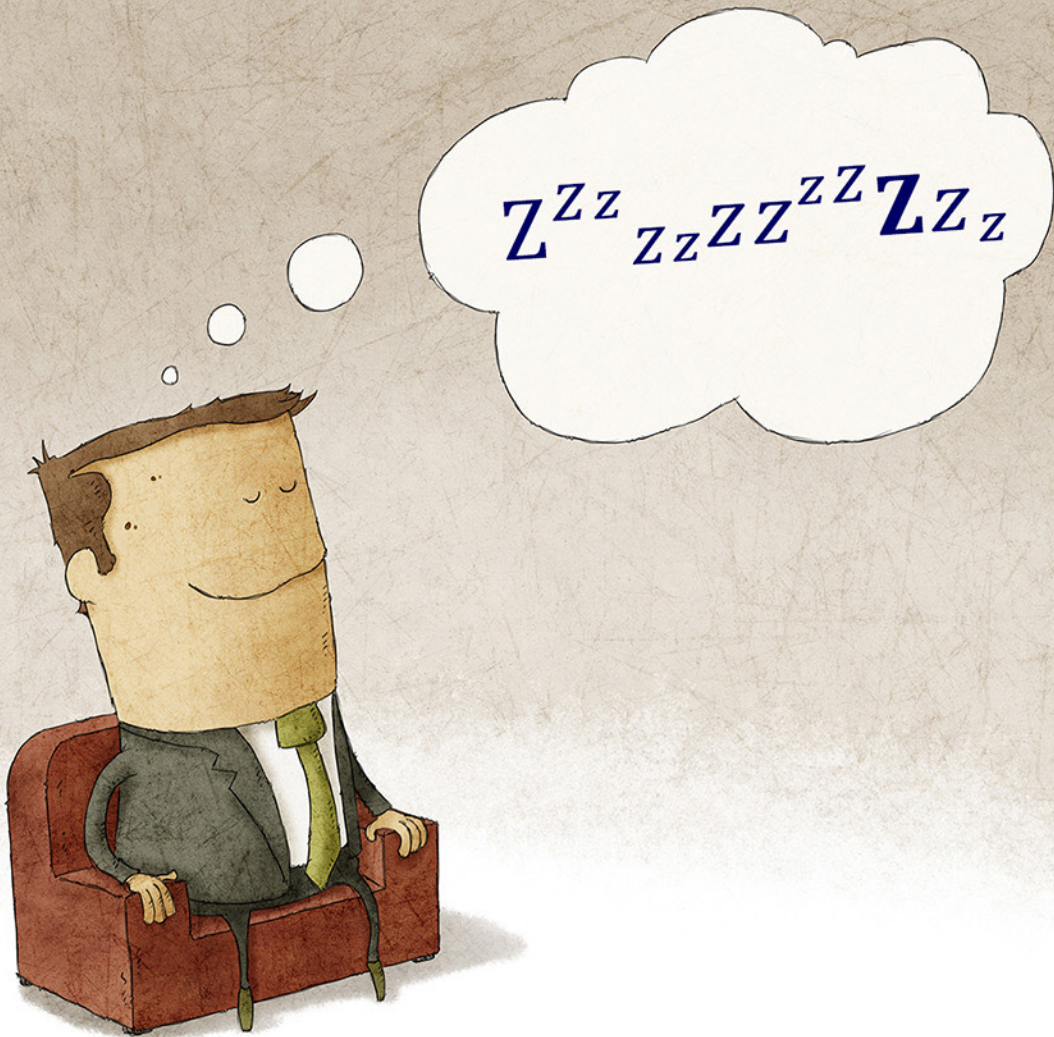
If you ask 10 engineers what “assembly” means in electronics, you’ll likely get 10 variations of the same answer: placing components on a board and soldering them down. That definition might work for traditional PCB-based electronics, but in high-power, high-reliability systems, it falls short by a mile.

Power module assembly is actually about building a system from the ground up, one that must handle heat, current, mechanical stress, and

time without failure. When you’re working with ceramic substrates and high-performance materials, assembly becomes less of a step and more of a discipline.

So, a power module assembly includes everything required to transform a bare substrate into a fully functioning, field-ready system—electrically, thermally, and mechanically integrated—and every step matters.

We **DREAM** Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."

– Barry Olney



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Assembly Is More Than Placement

In ceramic-based electronics, assembly starts long before anything is physically attached. It begins with understanding how the substrate, the devices, and the final application all interact.

This is not a “drop it on and solder it” environment. You’re dealing with materials like alumina or aluminum nitride, chosen for their thermal conductivity and stability. You’re often integrating bare die instead of packaged components, and you’re designing for environments where failure is not an option: electric vehicles, aerospace systems, defense platforms, industrial drives.

Assembly, in this context, is the process of integrating electrical performance, thermal management, and mechanical integrity into one unified structure. That’s a very different mindset.

Die Attach: The Foundation of Performance

Everything starts with die attach, the process of securing the semiconductor die directly onto the substrate. It sounds simple, but it’s one of the most critical steps in the entire assembly process because the die attach layer is responsible for both electrical conduction and thermal transfer. If it’s done poorly, you create electrical and thermal resistance, which, in power electronics, is the enemy.

There are several methods used depending on the application—solder attach, sintering, conductive adhesives—but the goal is always to create a strong, uniform bond that efficiently transfers heat away from the die while maintaining electrical integrity. Think of die attach as the foundation of a building. If it’s weak or inconsistent, everything built on top of it is at risk.

Wire Bonding: Connecting Performance to Reality

Once the die is attached, it needs to be connected, and that’s where wire bonding comes in. It creates

the electrical connections between the die and the rest of the circuit. Typically using gold, aluminum, or copper wire, this process forms the pathways through which current flows.

But wire bonding isn’t just about making a connection. It’s about making the right connection. Bond geometry, loop height, wire diameter, and placement all impact performance. In high-power applications, these factors influence current handling, resistance, and even inductance. Poorly designed or executed wire bonds can become points of failure under thermal cycling or vibration.

In other words, wire bonding is where electrical design meets physical reality and gets tested.

Encapsulation: Protecting What Matters

Now that the die is attached and connected, it needs to be protected. Encapsulation is the process of sealing the assembly to protect it from environmental factors, including moisture, contaminants, mechanical damage, and thermal stress.

This step is essential in high-reliability applications because power modules do not operate in clean, controlled lab environments. They operate in vehicles, on factory floors, in the sky, and sometimes in space.



The road to American manufacturing is paved with PCBs.

PCBs make modern life possible. Every semiconductor needs a printed circuit board and IC substrate to function.

Over the past 20 years, PCB production has moved away from the United States at an alarming rate. PCBAA is the industry's voice in Washington, DC, leading a bipartisan coalition to advocate for investments in this critical industry.

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Encapsulation materials must be carefully selected to match the thermal expansion properties of the substrate and components. If they don't, you introduce stress, and that leads to cracks, delamination, and eventual failure. Done correctly, encapsulation extends the life of the module and ensures consistent performance over time.

Housing Integration: Where Mechanics Meets Electronics

At some point, the assembly needs to become a product, and that's where housing integration comes in. This involves incorporating the assembled substrate and components into a mechanical structure that supports the module, protects it, and often contributes to thermal management. It's part of the system that must account for mounting requirements, vibration, thermal expansion, and heat dissipation. In many cases, it includes features like heat sinks, baseplates, or direct cooling interfaces.

Problems arise when housing is designed in isolation from the electronics. Misalignment, stress points, and thermal inefficiencies become common. But when housing is integrated into the assembly process from the beginning, everything fits, mechanically and functionally.

Why Integration Reduces Failure Points

Now, let's shift from process to strategy. When power module assembly is handled by multiple vendors—one for substrates, another for die attach, another for packaging—you introduce interfaces, and every interface is a potential failure point. You get miscommunication, material mismatches, and process inconsistencies.

Integrated sourcing, where one partner manages the entire assembly process, eliminates those gaps. It ensures that every step is aligned, every material is compatible, and every process is optimized for the final application.

Thermal Performance: The Real Battleground

Heat drives the evolution of power module assembly. As power densities increase, and devices get smaller, the demand for efficiency is relentless. In this environment, thermal performance is everything.

A unified assembly approach allows for optimized heat flow from the die, through the attach material, into the substrate, and out through the housing. Every layer is designed to work together. Ceramic substrates already offer a significant advantage due to their high thermal conductivity, but that advantage can be lost if the assembly process isn't properly aligned. When it is aligned, you get systems that run cooler, last longer, and perform more reliably.

Lifecycle Support: From Design to Production

Power module assembly doesn't end when the product is built. In many ways, that's just the beginning. True assembly capability includes lifecycle support, from design collaboration through prototyping to production.

Early design involvement allows engineers to optimize layouts, select the right materials, and anticipate challenges before they become problems. Prototyping validates those decisions, which ensures consistency at scale.

This continuity is critical because in high-performance electronics, small changes can have big consequences. Having a single partner involved from start to finish ensures that knowledge is retained, lessons are applied, and performance is maintained.

The Bottom Line

So, what is included in power module assembly? It's die attach, wire bonding, encapsulation, and housing integration, but more importantly, it's the integration of all those elements into a single, cohesive system and the understanding that performance is determined by how well every step works together.

As power electronics push the limits of what's possible, you need that level of integration. Powering the future is about building systems that work no matter what. **I-CONNECT007**



Brian Buyea is president of Remtec Inc. To read past columns, [click here](#).

A Closer Look at AI Data Centers



In November 2022, OpenAI, a company with fewer than 400 employees, released ChatGPT as a public research preview. Within five days, more than one million people signed up. Two months later, that number grew to 100 million, making ChatGPT one of the fastest-growing consumer applications in history. By early 2023, following a major investment from Microsoft, OpenAI's valuation climbed to an estimated \$20–29 billion. More importantly, the launch ignited an AI arms race that is reshaping the global technology landscape.

AI has since sparked one of the largest infrastructure buildouts in decades. Around the world, companies are racing to construct a new generation of data centers capable of supporting AI workloads that dwarf the computing demands of traditional cloud applications. These facilities are redefining expectations for processing power, memory bandwidth, net-

work speed, and power delivery, while driving unprecedented demand throughout the electronics manufacturing supply chain.

For the PCB industry, the AI data center represents far more than another high-growth market. It is reshaping design priorities and accelerating innovation in high layer count backplanes, advanced materials, signal integrity, thermal management, and manufacturing processes. At the same time, the pace of deployment is exposing new challenges, from supply chain constraints and escalating power requirements to the need for greater reliability in increasingly dense, high-performance systems.

In this Special Section, I-Connect007 examines the market forces driving the AI data center, the technologies, like liquid cooling, that enable it, and the opportunities and challenges it presents.



The journalists visited Niagara Falls at the end of the day.

POWERING AI Inside TeraWulf's Lake Mariner Campus

On a windy Thursday morning in Barker, New York, this spring, I joined 30 tech journalists as we disembarked from a bus onto the shores of Lake Ontario to tour TeraWulf's 157-acre Lake Mariner Campus. Roughly the size of 119 American football fields, it is the largest U.S. AI data center under construction.

Before the tour even began, we passed several buildings and a vacant coal power plant. In the 15-minute bus ride from the security gate to our touring destination, adjectives such as enormous

and vast came immediately to mind. Once off our bus, we were shuttled into one of the campus's smaller buildings to obtain our safety gear and attend a lecture on what we were about to see. No photos or recordings were allowed during the actual tour. As we listened to several executives from both TeraWulf and Schneider Electric, it became clear that even for them, the scale of this project and the incredible speed at which it is being completed are impressive.



Nazar Khan, co-founder and CTO of TeraWulf

TeraWulf is an AI infrastructure and power provider. A tagline on its website declares, “AI and high-performance computing scale only as fast as power allows. ... TeraWulf delivers the power and the infrastructure that make sustained growth possible.” The company creates “mega” data centers by first finding available land with ready power and fiber connectivity, working with local and state governments for permission and to complete strategies, and partnering with a company like Schneider Electric to bring it all together. TeraWulf, and the very few compatriots they have in this space, are building the data centers the world requires for the AI that we not only want, but expect in the coming decades.

The Barker location of Lake Mariner was once the site of a coal power plant. Unlike many of the hyperscalers that will eventually become users of the data center sites that TeraWulf is building, TeraWulf is not deterred by the environmental implications of site cleanups, which opens up location options that others might not see or find attractive.

HOW MUCH POWER IS 750 MW?

750 MW is a tremendous amount of power, roughly equivalent to the electricity demand of a mid-sized U.S. city, like Buffalo, New York. A 750 MW campus would rank among the largest AI-focused data center developments in North America. By comparison, a traditional enterprise data center operates at less than 20 MW, while large hyperscale campuses often range from 100–300 MW. A 750 MW site can support multiple AI training clusters containing tens of thousands of GPUs, making it attractive to hyperscalers and AI platform providers that require massive amounts of compute capacity.

The Lake Mariner Data Center is one of five such projects TeraWulf currently has underway in the United States, in early stages of development. The others are in Lansing, New York; Hawesville, Kentucky; Charles County, Maryland; and an as-yet-unidentified location in Texas. The portfolio will amount to over 2 GW of power, roughly the output of 7% of New York State during a recent summer heat wave. The Lake Mariner campus will be the largest of the five sites at 750 MW once completed, and is the only one currently operational (with newer buildings still under construction). It is a stunning example of what a modern AI data center must be to adequately support AI high compute power and heat.

The campus started with what is affectionately named the “WULF DEN,” a more modest 2 MW proof-of-concept build that has provided the basis for the huge scale-up at Lake Mariner. The next scale jump was 10x for the completion a 20 MW capacity building, CB1. CB3 and CB4 are the largest of the buildings and are still under construction, the latter clocking in at 330,000 square feet and built to

achieve 215 MW of power.

Nazar Khan, co-founder and CTO of TeraWulf, gave the clearest preview of what we would see during our tour. There were massive mechanical rooms where the building's heat exchange takes place, using coolers and chillers in a closed loop system that uses surprisingly little water (compared to their air cooling predecessors), then seemingly endless rows of server racks, each rack with its own cooling system, and finally, the connectivity for water and power at the rack level and in the floors and ceiling. Of course, the description doesn't do justice to the actual tour experience. We walked quickly, asking lots of questions, with our eyes wide and our minds spinning with amazement at the breadth and depth of the center.

Marc Garner, Schneider's global president of cloud and servers, had asked us to make note of all the renewable energies being used as we toured, and called it "a phenomenal example of how we should be producing data centers with clean energy." With abundant power availability and a predominantly zero-carbon regional grid, TeraWulf is building the foundation for the AI economy while helping redefine the future of data center development. Indeed, it was impressive and offered me some hope amid the tense societal discussion taking place (including in my own state) around the placement of AI data centers and whether the burden they will potentially or inevitably place on surrounding areas will be unfair.

The CB4 building was a feat of civil engineering in and of itself, supported by tons of concrete and steel, the two greatest material inputs in any data center build. The concrete walls of CB3 and CB4 were built approximately three stories high, all supported by heavy steel beams. The expansive concrete floors were also supported by steel, and both the floors and the ceilings of the building were designed for an immense amount of wiring and pipe work to support both power and cooling connectivity required for an AI data center. The weight of just the building infrastructure itself is massive before a single heavy server rack is moved into the space, of which there will be hundreds.

TeraWulf is one of just five power and infrastructure companies identified as capable of building



Marc Garner of Schneider presented data on projected AI compute workload to the journalists on the tour.

data centers at this scale. Like them, Schneider Electric is one of just a handful of companies capable of partnering with companies like TeraWulf to provide power and cooling infrastructure at this scale. For Lake Mariner alone, Schneider has provided more than \$290 million in power, cooling, and digital infrastructure solutions to the project.

Earlier in the day, Mark Garner stated, "At this point here, we are looking at AI workloads being around about 35% of all the compute deployed in 2030." When it comes to creating enough infrastructure to support that, he said it "is very much an arms race."

As mentioned, Lake Mariner is the only TeraWulf operational data center campus, with anchor neocloud tenants, Core42 and Fluidstack. In this race, neoclouds are vitally important. Unlike their cloud cousins, these companies rent cloud access to high-end AI servers, such as for the NVIDIA GB200 and GB300 Blackwell chips. Like TeraWulf and Schneider in their own categories, the number of viable neocloud companies capable of this scale is alarmingly small. Consequently, a signifi-



TeraWulf COO Sean Farrell spoke about the setup of the Lake Mariner campus.

cant portion of the tremendous amount of AI investment we see is dedicated to infrastructure and to creating more neoclouds. Schneider executives reported approximately 150 new neocloud companies founded over the last three years, with companies like NVIDIA helping to bring some of them to market.

To say that my visit to Buffalo and tours of Schneider Electric's Motivair facility and TeraWulf's Lake Mariner AI data center expanded my understanding of the extraordinary infrastructure required to power the AI revolution is a gross understatement.

Yet, while I have much more to learn, seeing the scale of a 750 MW AI data center firsthand gave me a new appreciation for the engineering, energy, and vision driving this transformation and the immense task in front of us to support AI as we expect it to develop and serve our needs. I am deeply grateful for the opportunity, remain humbled by the magnitude of what lies ahead, and look forward to watching this part of the AI story continue unfolding.

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WHAT'S THE DIFFERENCE?

Today, we all know “the cloud,” but how is a neocloud company different, and what makes one a hyperscaler in data centers? Here are some simple definitions and a table of the current top hyperscalers.

Hyperscaler: A company that owns and operates computing infrastructure at global scale, including massive data centers and networks.

Cloud provider: A company that delivers computing services over the internet.

Neocloud: A specialized cloud provider focused primarily on delivering high-performance AI computing, usually powered by NVIDIA GPU clusters.

Hyperscaler	2026 Total Projected CapEx Q2	2026 & Full-Year Guidance Highlights
Amazon (AWS)	~\$200 B	Remained the highest absolute spender, allocating funds heavily into expanding Amazon Web Services (AWS) data center clusters and e-commerce logistics.
Alphabet (Google)	\$175–\$185 B	Accelerated infrastructure buildouts for Google Cloud, Core Search, and internal generative AI models, with CapEx approaching 46% of sales.
Meta	\$115–\$135 B	Significantly raised full-year guidance to fund massive GPU clusters; Meta's CapEx represents an unprecedented 54% of its total revenue.
Microsoft	~\$120+ B	Consistently outpaced prior expectations, leveraging a mix of direct CapEx and aggressive finance lease structures to deploy hardware for Azure.
Oracle	\$45–\$50 B	Punching well above its weight class with a high-intensity funding plan that consumes a staggering 86% of its sales revenue.

ANATOMY OF AN AI DATA SERVER

From Hyperscale Data Center to GPU Compute Tray

AI workloads demand extreme compute density, massive bandwidth, and efficient thermal management. Here's a look inside the modern AI data server infrastructure.



EXTREME COMPUTE
AI training & inference at massive scale



EXTREME POWER
100kW+ per rack power density



EXTREME COOLING
Direct-to-chip liquid cooling for peak performance



EXTREME BANDWIDTH
Terabits per second of GPU and network connectivity

1 AI DATA CENTER RACK (42U)

High-Density AI Infrastructure

1 TOP-OF-RACK (TOR) SWITCHES

High-speed spine/leaf networking for low-latency, high-bandwidth connectivity.

2 MANAGEMENT & SECURITY APPLIANCE

Remote management, telemetry, and security monitoring.

3 POWER DISTRIBUTION UNITS (PDUs)

High-density power distribution, metering and monitoring.

4 LIQUID COOLING MANIFOLD

Distributes coolant to each compute tray.

5 GPU COMPUTE TRAYS (UP TO 10 PER RACK)

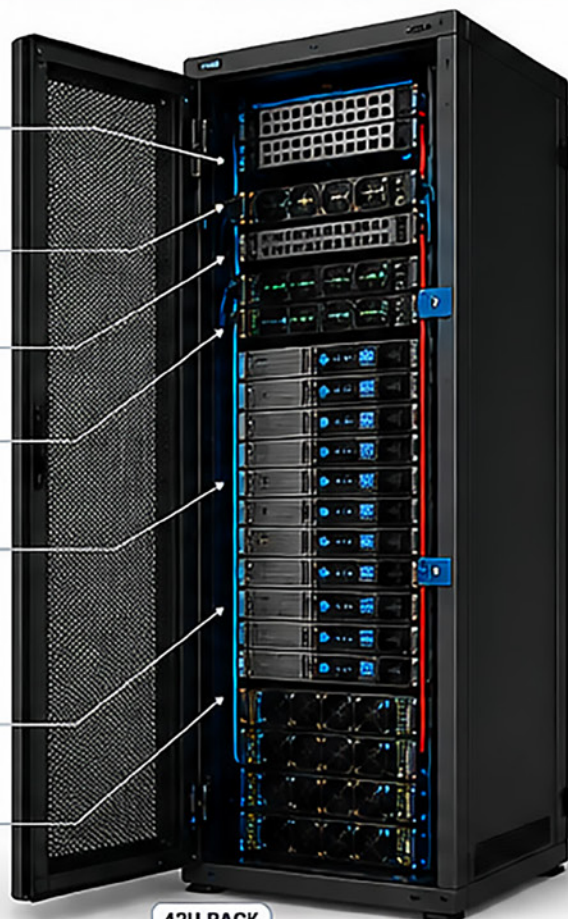
Each tray delivers massive parallel compute with GPUs, CPUs, memory, storage and networking.

6 REAR DOOR HEAT EXCHANGER

Removes heat from the rack via liquid loop.

7 POWER SUPPLY UNITS (PSUs)

Redundant, hot-swappable high-efficiency power.

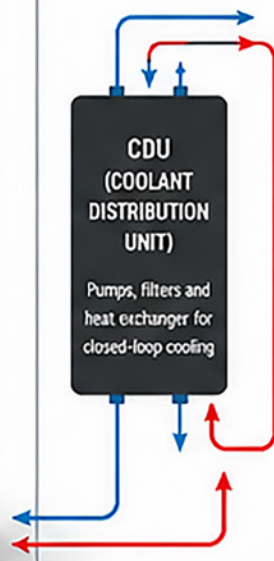


42U RACK

LIQUID COOLING LOOP

→ COLD LIQUID SUPPLY (IN)

→ WARM LIQUID RETURN (OUT)



4 HYPERSCALE AI DATA CENTER

Built for the Demands of AI



Extreme Compute Density
Rack densities of 70kW–130kW+ for AI workloads



High-Speed Fabric
Terabit-scale networking for massive AI clusters



Advanced Liquid Cooling
Direct-to-chip and rear door heat exchange for maximum efficiency



Resilient Power Architecture
Redundant power and cooling for 24/7 uptime

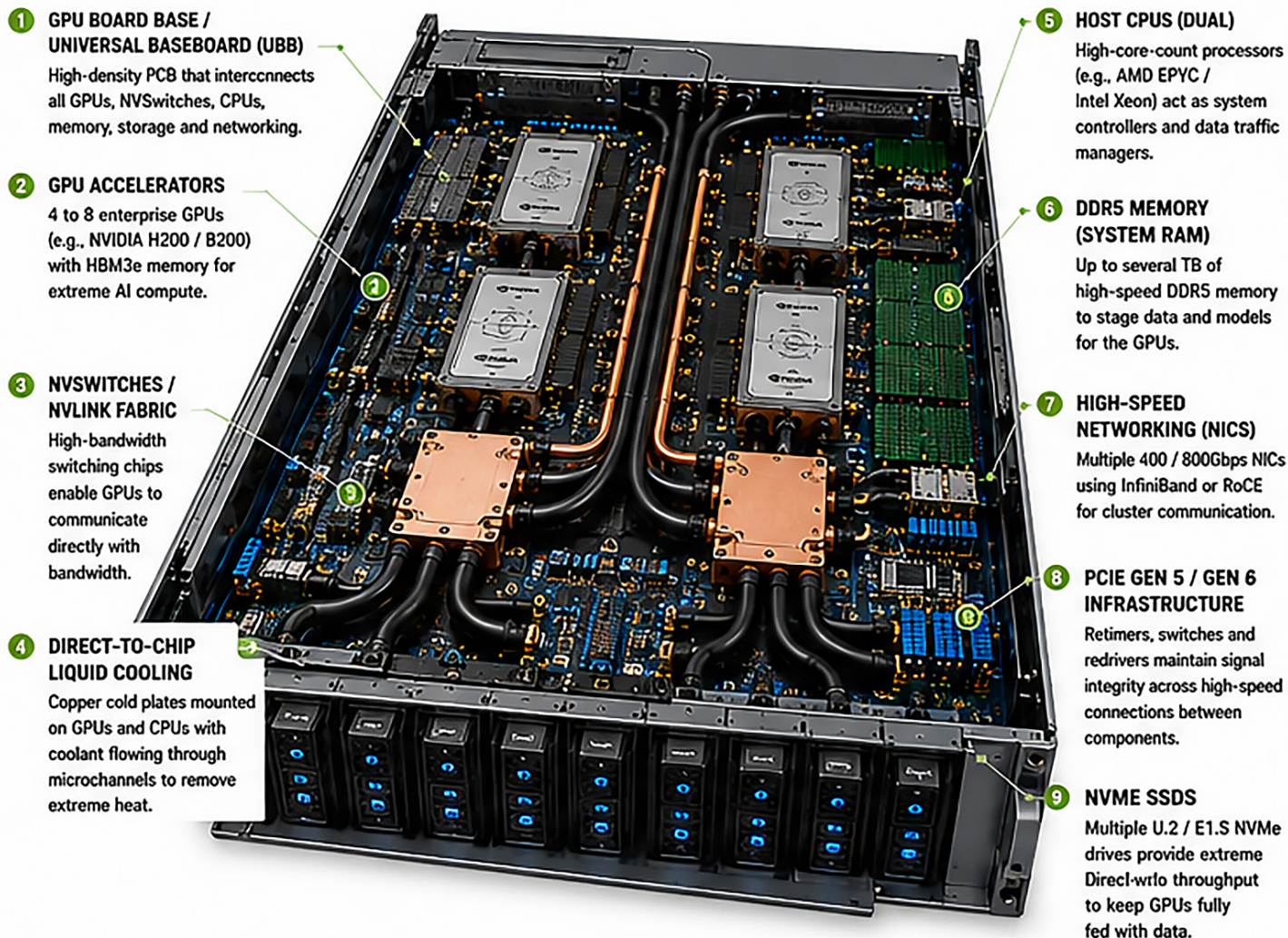


Scalable Infrastructure
Designed to scale from a single rack to thousands of racks

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2 INSIDE THE AI GPU COMPUTE TRAY (4U)

Engineered for Massive Parallel Processing



3 AI SERVER TRAY: SYSTEM COMPONENTS AT A GLANCE

COMPUTE & ACCELERATION



- GPUs (4-8 per tray)
- NVSwitches / NVLink
- High Bandwidth Memory (HBM3e)
- Universal Baseboard (UBB)

CONTROL & COORDINATION



- Dual Host CPUs
- DDR5 System Memory
- PCIe Controllers
- System Management

NETWORKING FABRIC



- 400 / 800Gbps NICs
- InfiniBand / RoCE
- PCIe Gen 5 / 6 Switches
- Signal Retimers

STORAGE & INFRASTRUCTURE



- NVMe SSDs
- Power Management ICs
- Direct-to-Chip Cooling
- Thermal Sensors

LIQUID COOLING ARCHITECTURE



Coolant from CDU
(Cold Supply)



Manifold Distribution
Across Tray



Cold Plates on
CPUs and GPUs



Heat Absorbed
At the Source



Warm Coolant Return
to CDU

The AI Data Center Boom

Technology, Capacity, and Society



AI may begin with a chip, but its impact ripples across the entire electronics supply chain. From advanced substrates and copper foil to power distribution, thermal management, and data center construction, the race to build AI infrastructure is reshaping manufacturing priorities worldwide, including for PCBs. That is where Schneider Electric becomes important.

Schneider Electric's Role in AI Infrastructure

As a global energy technology leader, Schneider Electric exists to “electrify, automate, and digitalize every industry, business, and home, driving efficiency and sustainability for all.” One of its most important business areas is supporting data center (DC) facilities and cooling the IT inside them—the

infrastructure that enables AI to run.

A modern AI data center is a different animal from data centers built before cloud computing and AI. They must be massive in size to meet the demand that AI and high compute present. They consume a tremendous amount of power, prompting their comparison to large cities and small countries. Importantly, this results in a tremendous amount of heat that must be dissipated at the server rack level as opposed to the facility building level, making traditional air cooling inadequate for the task. By 2030, AI is expected to drive approximately 60% of new data center deployments, necessitating significantly more data center capacity than exists today.

At this time, most large AI data center activity remains in the United States, driven by hyperscalers such as AWS, Meta, Google, and Microsoft. Schneider is involved in most new projects under development worldwide through its partnerships with leading technology providers, hyperscalers, and co-location operators. The company collaborates directly with NVIDIA and others to stay ahead of chip and silicon evolution.

A Closer Look at DCs, Cooling, and Supply Chain

During a recent visit to Schneider Electric's liquid cooling operations in Buffalo, New York, I visited with Andrew Bradner, senior vice president of the cooling business, to discuss how AI has transformed data center design, why liquid cooling has suddenly become a necessity rather than an option, and what these changes mean for the broader electronics ecosystem that supports the AI revolution.

Marcy LaRont: Andrew, it is nice to meet you. Tell us about yourself and your career. How long have you been with Schneider?

Andrew Bradner: I have been with Schneider for nearly 24 years, joining American Power Conversion (APC) in 2002. APC, based out of West Kings-



ton, Rhode Island, was acquired by Schneider Electric in 2007. Prior to that, I owned a human resource management startup software company in California, a precursor to today's software-as-a-service platforms.

I am originally from Rhode Island and moved back several years later to be closer to family. I wanted to continue working in technology, and the closest thing I could find was APC, where technology was part of operations. APC and Schneider have taken me

on a journey all over the world, to Shanghai, Beijing, and Barcelona. I am now based in Italy, moving through different parts of the business.

I've been in the data center business for over 20 years, five of which were leading our prefabricated data center business. When you talk about supply chain and the evolution of how data centers are built, I've seen that from the modular side. I have been leading the cooling business for more than seven years.

Italy is Schneider's engineering and industrial hub, but given the big builds in the U.S., you've been spending time here. What does that mean in relation to the Motivair facility we toured here in Buffalo?

Buffalo is our North American hub for liquid cooling, while Conselve, Italy, remains the location of our largest global cooling facility in terms of employees, manufacturing capacity, and engineering resources. We also maintain engineering and manufacturing centers in Bangalore, India and Zhuhai, China.

The Evolution of Data Center Cooling

Now that you've been in the server business for more than 20 years, what is the most significant change you have witnessed?

The most important change in the server journey is this pivot we began to see about four years ago. Historically, servers operated at power levels that could be effectively managed with fans and heat sinks. For years, CPUs and GPUs remained in the 200–300 watt range, making air cooling a practical and economical solution.

We learned in some of the technical sessions here that modern liquid-cooling solutions use less water and power than air cooling. That being the case, why didn't the industry just go to liquid cooling first?

Remember, these data centers at the time weren't built for the optimum data center design. They were built around the chip technology they were supporting. So, the data center design was very agnostic to the IT itself. At that time, air cooling was a logical solution. But now, with the incredible amount of heat that modern AI data servers generate, we must take a different approach to both rack and data center design.

Is this a trend that continues to ramp with each new chip design?

Yes, the generational shift between chipsets is immense. If you are deploying NVIDIA and deciding whether to deploy a GB200 NVL72 or a GB300 NVL72 rack system, each choice shifts how you need to distribute power and cooling.

Today, liquid cooling has become a necessity. Yet just five years ago, we were still looking at liquid cooling from a sustainability angle. We knew it would happen at some point, but weren't sure when.

Liquid cooling existed before AI, particularly in parts of Asia where climate and efficiency concerns made it attractive. However, the public launch of ChatGPT in late 2022 was an inflection point, accelerating AI adoption dramatically and turning liquid cooling from an efficiency strategy into an operational necessity.

Is there more upfront OEM involvement in data center and infrastructure design than there had been previously?

Yes, these changes are being driven by the OEMs, which have significantly affected the white-space design of servers. These server racks are being built plug-and-play ready for liquid cooling. ("White space" refers to the area inside a data center that is available for IT equipment: servers, storage, networking gear, and racks.)

We used to have thousands of server vendors. At one point, the guiding intelligence was that only

25% of servers would ever be liquid-cooled. Now, new server designs are released only with liquid cooling built in. That's what has driven the industry's shift toward liquid cooling.

This also changes the supply chain side. Today, only a few qualified organizations can build the right kind of server rack and data center facilities. OEMs like NVIDIA are working with that market, helping to bring up more qualified vendors.

Retrofitting Existing Data Centers

As these new data centers emerge, what will happen to all the old server farms? Will they always have utility as air-cooling facilities, be retrofitted for liquid cooling, or go defunct and become idle?

The older server facilities were generally built for enterprise computing, not the newer cloud-based applications that require more power and generate more heat. It's difficult to retrofit such facilities, but not impossible.

On the Motivair tour, you saw some heat-dissipation units at the end of the production line that were being developed into liquid-to-air coolant distribution units (CDUs). Those are often seen in brown-field or existing air-cooled data centers that don't have facility water going into their white space.

Theoretically, then, at least some of those older data centers could still be useful.

Yes, where you could deploy liquid cooling into those environments, modernization will be a big part of what happens. The access to power that those sites already have is primary for any data center location. You can leverage some of the electrical infrastructure even if you must rebuild into a more modern facility.

You may need to modernize some of the cooling infrastructure and look more at the physical build. What's the slab density? If it's multi-story, what weight can it manage? The weight that must be supported and the amount of steel and concrete infrastructure involved are different and much more substantial than what you would have for an existing enterprise compute data center.

We are seeing the larger companies do this at some of their older cloud computing sites.

Will circularity become a bigger part of the conversation again soon?

Yes, circularity is important, and part of Schneider's mission. When it comes to facility modernization, we try to minimize the work required and use what is already in place as much as possible. Even the retrofits are focused on the smaller parts that can be changed out rather than the housing and metalwork.

We are also paying attention to the expected lifecycle of the data center as chip technology continues to advance. Extending a center's lifecycle, especially as AI is applied to more and different use cases, is an important question.

Where AI Data Centers Are Being Built

Where do you see the greatest geographic push for new data center builds?

North America currently leads AI deployments, driven by access to advanced GPUs and significantly higher rack densities than many other regions. It is the difference between 132–600 kilowatts historically, to racks now pushing around 1 megawatt, then to skidded solutions enabled by modular CDUs ranging from 105 kW to 2.5 MW, with Motivair by Schneider Electric's liquid cooling portfolio scalable to 10 MW and beyond to meet the demands of next-generation AI data centers. So, the scale of deployments is very different. We're starting to see that change in Southeast Asia and Europe as chip availability shifts.

What is an optimum power arrangement for a modern AI data center?

The answer is not simple, and differs geographically, by climate, and by state. AI data center development is underway in Texas, Virginia, Nevada, and Phoenix. Each state has different rules and regulations as to how it can build and where it can access power. Some can build their own substations; others cannot.

Outside the U.S., Saudi Arabia is a good example of a country funding access to power, much of it through gas turbines that drive desalination, providing low-cost power for that region. The Nordics have strong access to renewable energy, especially hydro. So, each place has different dynamics that drive the "optimum" data center design for power.

What do you think about Phoenix specifically? We have a lot of semiconductor development there, but we have issues with water and power. Our reality is that we are 115°F for several weeks out of the year, so, to the average person, development here seems counterintuitive.

Phoenix has good access to power and land. The trade-off is that you need more mechanical cooling year-round. But the desert is dry, which helps cooling, and in the evenings, temperatures can drop 20 or more degrees. Those big swings are advantageous for natural cooling.

AI data centers are working with hot water temperatures of 40°C (104°F). A location that lets you take advantage of free cooling hours and days throughout the year is very important.

A regular person is considering the worst-case temperatures in the middle of the day. They want to keep their house around 70°F. That isn't needed for a data center. If it drops to 90°F at night, a data center can take advantage of that delta, providing cooling without using compressors or water to cool the chip. That wouldn't be comfortable for you and me, but it's fine for the IT equipment.

Building a Resilient Supply Chain

With manufacturing sites in many countries, what does Schneider's primary supply chain look like? Do you have local supply chain partners for your different manufacturing locations?

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Andrew, it has been a pleasure meeting and talking with you. This has been a real learning experience for me. Thank you. I-CONNECT007

The Relevance of VeCS as an HDI Process Option

Almost 10 years ago, Pete Starkey interviewed Joan Tourné, inventor and CEO of his new company, NextGin Technology.¹ Joan's resume included many years as a director at Mommers Print Service in the Netherlands, and then as advanced technology and business director with Viasystems Group. He had just secured his IP for a vertical conductive structure (VeCS), a novel means of creating high density vertical interconnections for semiconductors and complex, high layer count PCBs.

This month, we re-examine VeCS technology, a method for HDI PCB fabrication with large backplane-type boards developed in partnership with Wus, which uses the technology in its factories. VeCS has not gained much traction in other areas or among smaller shops, and as domestic U.S. and European fabricators struggle with whether and how they will meet next-gen density requirements, having all options on the table seems prudent.

Whether some fabricators find it controversial or problematic, Pete's original 2017 interview with Joan holds up, and it is incumbent upon technology journalists to keep the spotlight on innovation with the hope for more discussion. Whether, ultimately, VeCS is more widely adopted, other innovative solutions to our high density challenges may be discovered as a result of this discourse.

What Does VeCS Offer PCB Fabrication?

A fundamental challenge when building very high density PCBs is the difficulty in reliably plating vias that are beyond a 1:1 aspect ratio. In his work, Joan partnered with Wus to experiment with various oblong slot dimensions that tested the throw of the plating chemistry, as a supplement to the traditional round hole/via shape, which inherently has shorter plating throw capacity.²

Importantly, VeCS does not require different

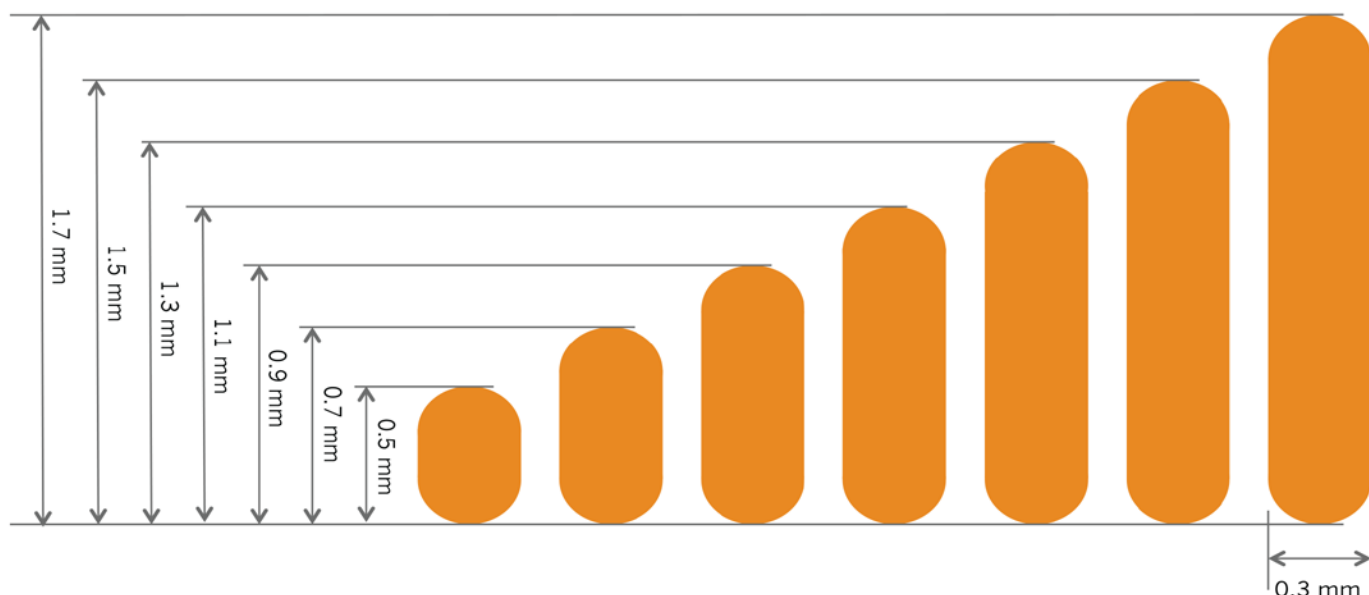


Figure 1: Slot dimensions used to conduct initial “throw” testing.²

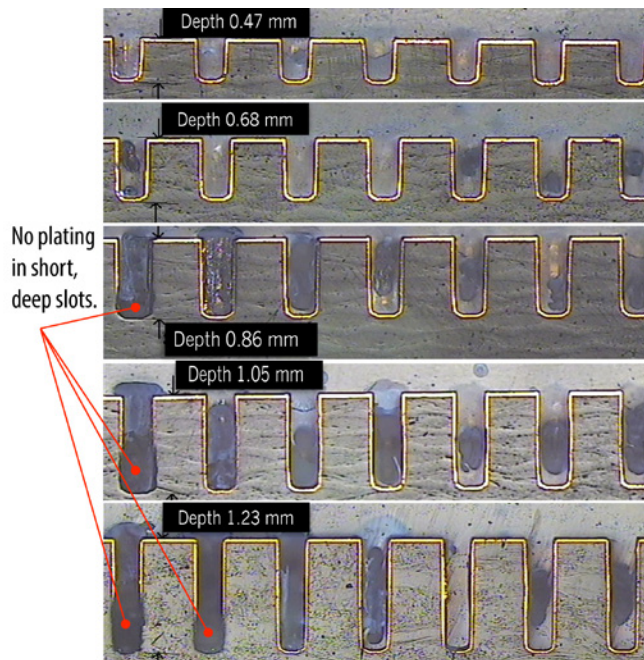


Figure 2: Test results, demonstrating that the more a slot resembles a circle, the shorter the plating “throw” capability, and that the longer the slot, the easier it is to plate.²

equipment or processes from those used in traditional PCB fabrication for drilling/routing or plating. The slot system in VeCS is created through standard CNC drilling, or micromachining to create the specific shape at different slot depths for VeCS-1 (blind vias) and VeCS-2 (buried vias) connections.

In his 2019 article,³ he acknowledged that this idea was not completely new, but there was limited research available, which he sought to rectify with his work: “Cutting holes into multiple sections has been on the research and development agenda of the interconnect industry for some decades, how-

ever, work to turn the technique into a process has not been successful to date.”

He addressed the challenge of CAF migration in bringing vias and microvias closer together and stated that forming slots reduces or eliminates this potential defect. He also stipulated that this method may require more lines of code than some older CNC machines can handle and that achieving good depth control remains a challenge. By 2021, Joe Dickson of Wus stated that most CAD programs had caught up and could provide the necessary software support for VeCS programming, and that the bigger issue was simply learning how best to use VeCS concepts.

It is noteworthy to mention that Joan acknowledged that it took time for NextGin and Wus to perfect their cross routing technique, and that alternate drill or rout bits may be required for the intended result. Also, via fill prior to routing is a critical part of this process.

In the early stages of R&D and testing with a handful of OEMs and fabricators at that time, results showed a significant cost reduction between 15–40% when VeCS was employed due to the reduction in lamination cycles and use of more standard materials. CNC drill/rout time remains significant, creating a potential process bottleneck, but newer VeCS techniques (VeCS-R, VeCS-X) have been added to the VeCS profile to increase speeds.

Though researchers initially believed cost would be the key driver to more substantial adoption of VeCS technology, that has not been the case. There remains a strong interest in any cost savings to be

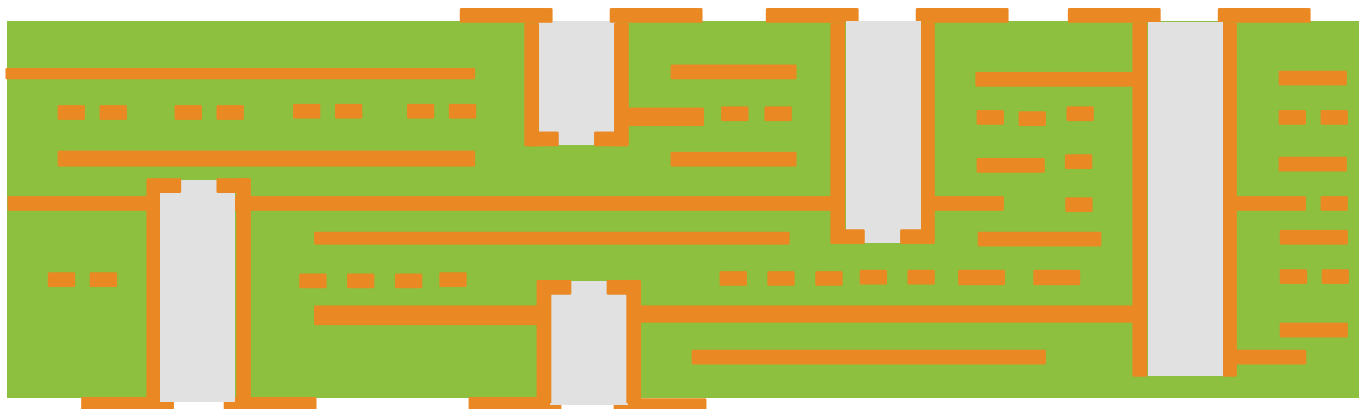


Figure 3: Practical examples of plating deep blind structures with VeCS.²

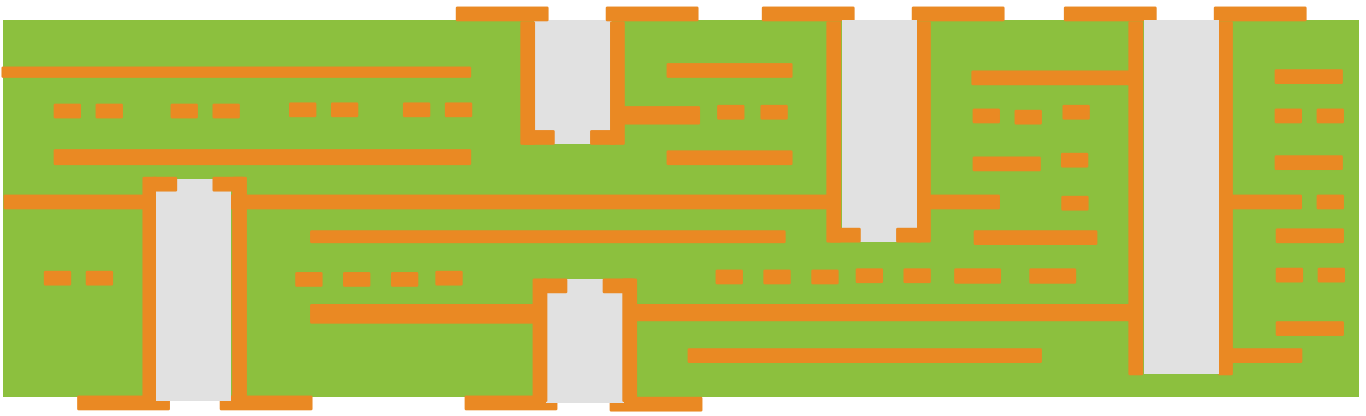


Figure 4: Traditional microvia constructions that can be replaced by VeCS.²

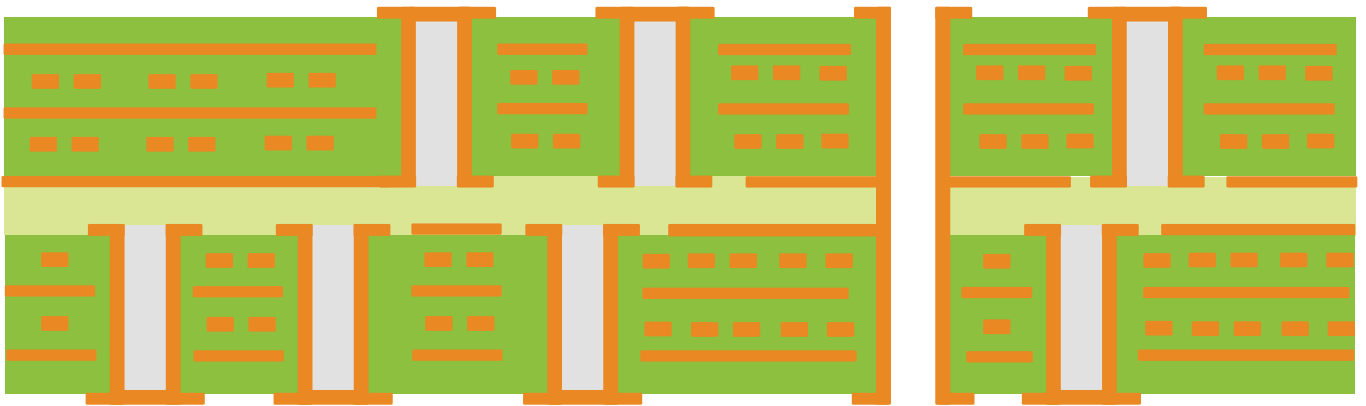


Figure 5: Single-lamination VeCS with a blind slot.²

achieved, but product reliability is the key driver for VeCS, given the challenges naturally present with stacked microvias. VeCS allows for thicker dielectrics between layers, contributing to better aspect ratios in some designs. Though some of the individual techniques of fabricators and their reliability results have, no doubt, advanced in a world where every layer interconnect (ELIC) is becoming more mainstream, the problems associated with them remain core considerations.

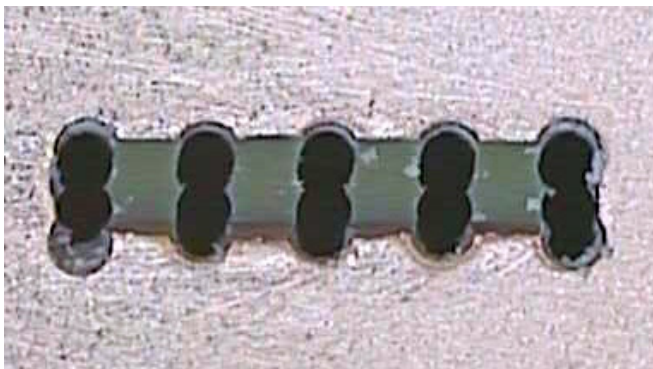


Figure 6: Cross rout results using a standard bit.³

From a broader perspective, though, this technique for building HDI PCBs will likely be additive to other technologies currently in use and under development. When we explore advanced electronics packaging and the advent of the UHDl PCB or substrate, all process technologies and techniques at our disposal will come into play—some developed from standard PCB and machining experience, others adapted from semiconductor manufacturing, as we are seeing in mSAP and SAP processes.

In Nolan Johnson's 2020 interview,⁴ he asked, "Theoretically, a board could be using VeCS, HDI, and traditional at the same time—three different topologies—depending on what you need?" to which Joe Dickson responded, "I expect that. If you look at where the industry is going, as well as the roadmap of system-on-chip and FPGA-type technologies, you're trying to do more and more on organic substrates outside of the PCB. That's going to work well as an enabling process to leverage technology and get it to the forefront for performance now. Right behind that should be some level of value

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Figure 7: Alternative bit from HPTec.³

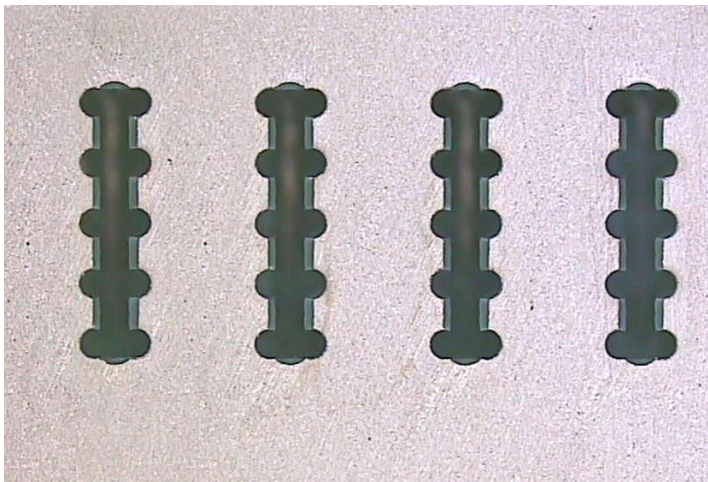


Figure 8: Clean cross routs using alternative bits and parameters.³

engineering, where those systems can be utilized and moved into the PCB. That's where some of the transformational value engineering will come. You'll enable it."

It was also noted that the PCB designer should be obligated to explore all possible ways a product can be built, with reliability, manufacturability, and cost in mind. Once designers become more open-minded about using alternative processes, doors will open to broader adoption of these now-proven methods for constructing reliable vertical connections in dense PCBs.

We are, indeed, seeing a great need for more innovative solutions to come to the fore, and I believe we are just scratching the surface of what will come over the next two decades.

I challenge PCB designers and fabricators to read the articles in this issue with an open mind. We know that change comes slowly to our industry, but we no longer have the luxury of allowing this slow pace. To my knowledge, large Asian fabricators like Wus are resisting prototype and small run production. As yet, adoption of VeCS industry-wide is still relatively low. Considering our business diversification topic in the July issue and the realities of today's global PCB market (and tomorrow's), there may well be a lucrative opportunity here for those willing to take a hard look. **I-CONNECT007**

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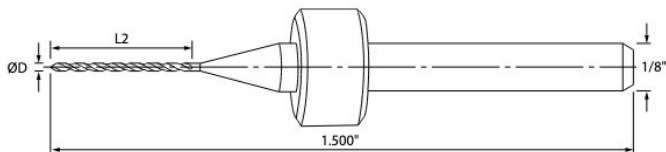


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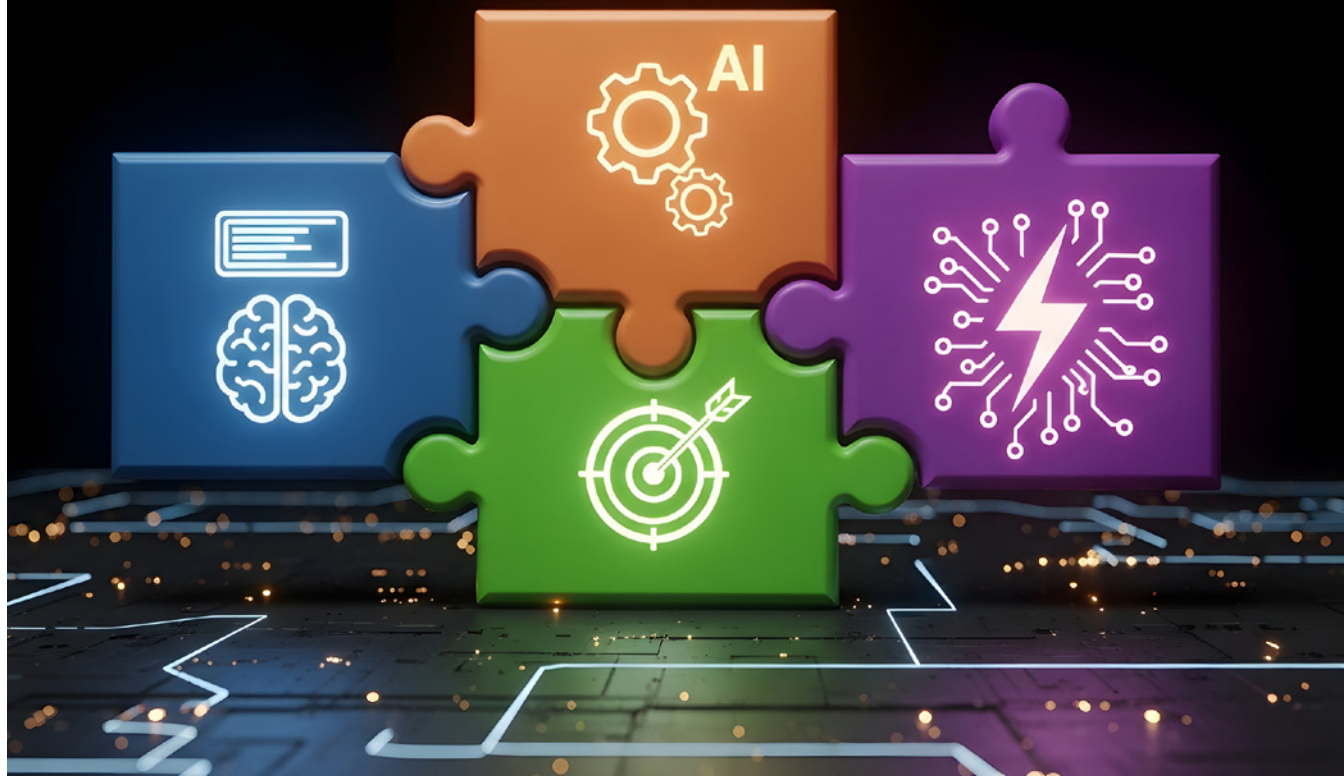
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4 Facet Point Geometry

REPOINTING will be a new service offered by Insulectro through Kyocera. The company has recently invested in automated, state-of-the-art equipment and all repointing will be done in Southern California.

Implementing Strategic Planning Principles for PCB Design



BY VERN SOLBERG, CONSULTANT

Developing multiple-processor system-level products involves a broad range of engineering disciplines (commonly referred to as co-design), often led by a designated program manager who divides the development program into technical disciplines.

The primary member of this team is the electrical engineer (EE), who prepares the overall schematic diagram of the product. This effort includes simulation and modeling, developing a BOM, and defining all active components and any specialized passive

elements (often stipulating preferred or prequalified sources).

When developing a product for use in a specific environment, such as harsh operating conditions, avionics, or automotive, for example, an engineer specializing in product certification, electrical test, and physical stress testing may be assigned to confirm that the end product will meet all designated standards or special requirements defined by the end user. The mechanical design engineer assigned to the program will then furnish the PCB

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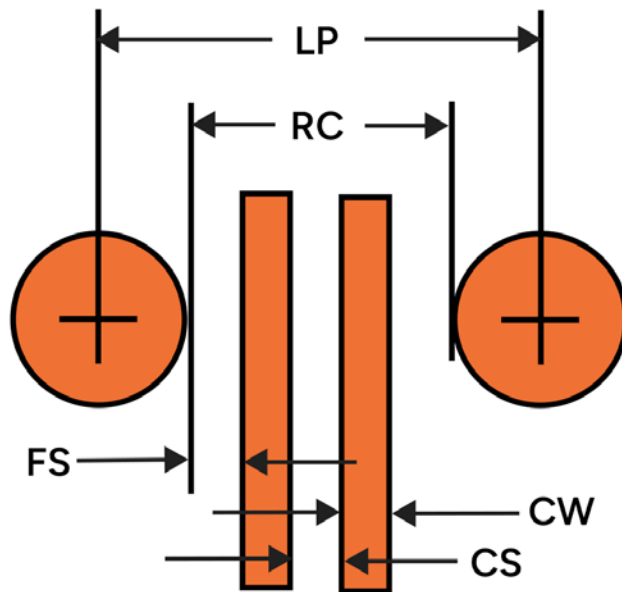
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LP = Land Pitch
 FS = Feature Spacing
 CW = Conductor Width
 CS = Conductor Spacing
 RC = Routing Channel

Figure 1: Defining channel width for conductor routing paths.

design engineer with the overall physical specification for the circuit board, physical outline, the base materials best suited for the application, laminate type and source, and finished plating and coatings (solder mask), as well as establishing the finished board's maximum thickness.

The key member of this team, after all, is the PCB design engineer, who is responsible for converting the schematic representation of the product into a tangible, physically functioning PCB ready for assembly.

Establishing PCB Design Strategy

Before beginning the design process, the PCB designer will perform an interconnect capacity analysis to establish the basic component area requirement. In preparation, the PCB design engineer must first gather mechanical outline specifications and electrical data for all active and passive component parts. From this data, the designer assigns the associated land pattern geometries and pad stack data from the pre-established CAD library. For those components without existing descriptions and pad-stack data, the manufacturer's mechanical and electrical information must be documented to enable creation of the new part(s).

To calculate the basic area required for component placement and circuit interconnect, designers must contemplate the land pattern features for

mounting the components, define keep-out zones, and establish clearances reserved for the assembly process and post-assembly evaluation, as well as the allowances needed for rework and repair. The final analysis will provide the designer with an estimated maximum surface area needed to complete all circuit interconnects.

Conductor routing protocols must be established in advance. The space separating via-hole lands, microvia lands, and/or component attachment lands is referred to as "channel width." The channel widths for routing array-configured (BGA, FBGA, WLBGA) semiconductors are calculated using the terminal pitch (center-to-center distance) and the land pattern size. This defines the maximum number of conductors that can be routed between each channel (conductors per channel), as demonstrated in Figure 1.

The factors that define the limits of circuit conductor routing ability in a substrate are:

- Pitch (distance) between land patterns and via-hole lands in the substrate
- Number of conductors that can be routed between those features
- Maximum number of sub-surface signal layers required

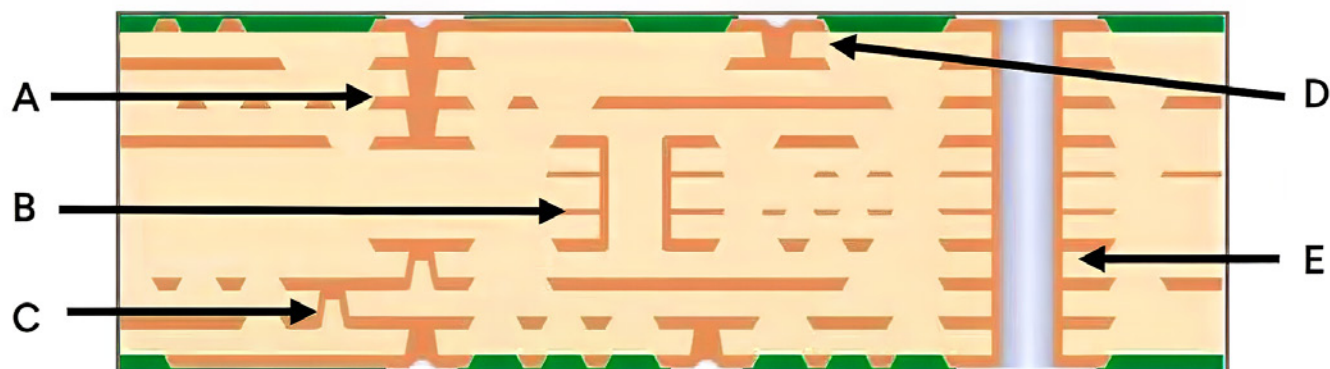


Figure 2: Sequential 3-4-3 build-up circuit board cross-section view: a) Vertically stacked, laser-formed, Cu-filled microvias joining build-up layers; b) Buried, mechanically drilled, and plated via in four-layer core section; c) Stagger-stacked, laser-formed microvias to join build-up layers; d) Blind and plated laser-formed and Cu-filled layer-to-layer microvia; e) Mechanically drilled and plated through-hole. (Source: KSG Europe)

The spacing between circuit conductors must account for the established minimum electrical clearance for fabrication process variables, solder mask surface adhesion, land pattern features, via-hole lands, and other fixed elements on the board.

PCB Circuit Density Analysis

When defining the board's complexity level, the designer will first establish a criterion for fabrication, including the board outline and thickness limitations. Regarding the specified circuit board thickness limit, clear objectives must be established to determine how many circuit layers are dedicated to signal routing and how many are reserved for power and ground distribution. This helps determine the component density and interconnect complexity.

While a significant number of semiconductor packages will have a moderate level of complexity (I/O and terminal pitch), others may have an excessively high I/O density. One solution to conductor routing roadblocks is to adopt blind via-in-land techniques to assign a majority of the interconnect to the sub-surface layers. When component density restricts circuit routing on the outer surface, subsurface circuit routing can be justified. Adapting blind and buried microvia holes as well as predefined conductor routing channels will help the designer facilitate efficient interconnection of these often

very fine-pitch and high I/O array terminal configured semiconductor packages.

The complexity of fabricating the circuit board must always be a consideration in cost control so a limit may be preestablished to restrict the number of circuit layers.

Figure 2 represents a 3-4-3 multilayer circuit board with a four-layer core and three additional circuit layers sequentially laminated onto both outer surfaces.

Sequential Build-up (SBU) PCB Processing

SBU offers a variety of design options. Designers can choose sequential build-up using stacked microvias for layer-to-layer interconnect or the staggered microvia, where via-holes are offset from one layer to another. The SBU board's complexity is ultimately determined by component density, circuit interconnect density, and the number of signal conductor layers plus the number of layers dedicated to power and ground.

The sequence in which the circuit board layers are assembled (signal, power, ground, etc.) is a key factor affecting signal transmission performance. Layer count and the method selected for interconnect between circuit layers, for example, will have a significant influence on controlling process complexity.

Implementing blind microvia technology for layer-to-layer interconnect can enable significantly greater circuit routing density, but the build-up process substantially increases the manufacturing complexity since it will affect the number of lamination cycles.

Some of the more complex SBU designs, for example, may require 15 or more lamination cycles. With each lamination cycle, the core materials are subjected to repeated exposure to elevated temperatures and high pressure. The concern is that excessive lamination cycles can contribute to material decomposition, especially a concern for the very thin, multiple layer circuit boards commonly developed for hand-held or portable communication products. These PCBs, in particular, will be more prone to board warping during assembly.

Planning PCB Fabrication

Although rarely an employee of the actual product development company, a key member of the engineering co-design team is the circuit board fabricator, which commonly furnishes practical guidance that helps ensure efficient fabrication processes, maximize yield, minimize cost, and reduce complications.

“One of the more common mistakes designers make in creating multilayer structures is that they are often unnecessarily complex.”

A prominent PCB manufacturer in Silicon Valley made the following observations:

1. Space constraints, due to the increasing number of signal conductors, increased component density, and number of terminals, will limit the open area on the PCB's surface. This factor can impede the designer's effort to provide the most efficient interconnect circuit routing. Circuit routing becomes increasingly challenging as the spacing between terminal lands decreases.
2. As the component density increases and board surface area becomes restricted, it will force the designer to rely on additional circuit layers for subsurface circuit routing. An excessive increase in circuit layers, however, will impact both fabrication efficiency and manufacturing cost.

Challenges facing the fabricator include:

- Tolerance control when aligning all layers in the stackup
- Maintaining layer-to-layer registration during lamination
- Consistent thickness control of the finished board
- Avoiding hole breakout of mechanically drilled holes

Fabricators should caution designers to exercise restraint in layer count and in implementing overly complex layer-to-layer interconnect schemes. The cost impact attributed to process complexity can adversely affect the competitive position of the end product. Yes, refinement of the board design will require more effort and a little more time, but simplifying the design at this stage of development can reduce fabrication complexity, processing time, and cost. **I-CONNECT007**

Note: I have learned that establishing a business relationship with the fabricator early in the development cycle will contribute to both end product reliability and performance. They can assist in selecting the most suitable materials and fabrication method for the application, i.e., subtractive vs. semi-additive circuit definition, conventional multilayer vs. sequential buildup, mechanical drilling vs. laser microvia processing (stacked or staggered). Their goal is to give you a reliable, high-yield product at an acceptable cost.



Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. He is the author of several books, including *Design Guidelines for Surface*

Mount and Microelectronic Technology. To read past columns, [click here](#).



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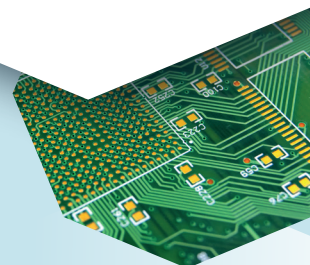
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SYL	Autolad 3G	S7045G S7045GH S7040G	S7038	S7439 S7439C S7439G S7439HW	Synamic 6 Synamic 6X Synamic 6G Synamic 6N	Synamic 8 Synamic 8G Synamic 8GN	Synamic 8NE Synamic 9GN Synamic 9N2
ITEQ	IT-858G	IT-170GT IT-170GRA1	IT-180A	IT-958G IT-170GRA2	IT-968 IT-968G IT-968GSE	IT-988GSE	IT-988G
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PREPARING FOR A New Laminate Supply Reality



The global laminate industry has entered a period of structural change unlike anything seen in recent decades. Explosive investment in AI infrastructure, including AI servers, advanced networking, optical communications, and data centers, is driving demand for laminate materials at a pace the supply chain cannot match.

The warning signs have been building for months. Extended lead times, repeated price increases, customer stockpiling, raw material allocation, and major capacity expansion announcements all

point to an industry increasingly under strain. How prepared are individual companies to respond to these changes?

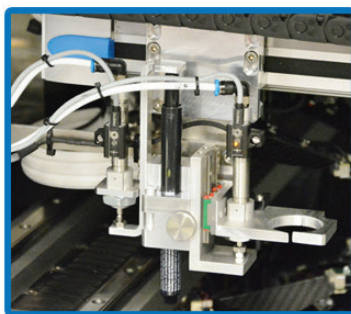
Experience from previous supply chain disruptions has shown that resilience cannot be created once a crisis begins. Alternative materials, qualified suppliers, strategic inventory, and long-term partnerships all require time to establish.

Compounding today's challenge are less visible pressures that extend beyond material shortages. As production capacity shifts toward higher-value

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AI applications, we see secondary constraints in conventional PCB materials. Rising inventory values are placing unprecedented demands on working capital throughout the supply chain.

For example, major vertically integrated groups such as Kingboard Holdings and Nan Ya Plastics Corporation are reducing merchant sales of glass yarns and fabrics in favour of internal consumption. They operate extensive downstream prepreg, copper-clad laminates (CCL), and PCB manufacturing businesses, and given their scale and reach across the value chain, these groups can shape pricing dynamics throughout the broader PCB industry. The consequence is less material reaching the merchant market, increased pressure on independent manufacturers, and a further acceleration of allocation-driven supply conditions.

So, for many organizations, the greatest competitive advantage over the coming months may not be simply securing material, but having the financial resilience and supply chain strategy to secure it before constraints become critical.

Key Industry Developments

1. AI Demand Is Reshaping the Entire Electronics Materials Supply Chain

The rapid deployment of AI servers and supporting infrastructure extends well beyond semiconductors and packaging, and is driving substantial increases in consumption of CCLs, prepregs, copper foils, glass yarn and glass fabric, and high-performance resin systems. Industry analysts view AI infrastructure as the dominant demand driver across the PCB and laminate sectors for the remainder of the decade.

2. Lead Times Continue to Extend

Industry reports indicate significant increases in lead times for laminate materials, up to 140 days for advanced laminate grades, and beyond historic norms for FR-4 products. PCB manufacturers are placing unusually large forward orders to increase inventory holdings, indicating a shift toward allocation-based supply management and a higher priority than short-term price optimisation.

3. Capacity Expansion Is Underway Across the Industry

Major laminate manufacturers throughout Asia have announced significant investment programmes designed to expand prepreg and laminate capacity. However, industry participants report long lead times for new laminating equipment, and 18–24 months for capacity expansion projects to become fully operational.

4. Upstream Raw Materials Remain the Primary Constraint

The most significant risks are concentrated upstream. Industry reports consistently identify shortages and allocation measures affecting glass yarn, glass fabric, very low profile (VLP) and hyper very low profile (HVLP) copper foils, specialty resin systems, and certain chemical intermediates.

These constraints directly impact prepreg and laminate production regardless of downstream manufacturing capacity. Consequently, the industry's ability to increase output is becoming increasingly dependent on the expansion of raw material supply rather than on laminate manufacturing capacity alone.

The Hidden Working Capital Challenge

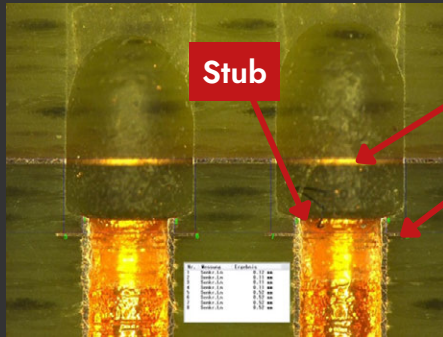
As demand shifts toward premium laminate systems, advanced resin technologies, and HVLP/VLP copper foils, companies face a double financial burden. Not only are they being forced to carry higher inventory levels to mitigate supply risk and secure allocation, but the value of every square metre of inventory is increasing significantly.

This combination means working capital requirements can rise substantially faster than revenue growth. Inventory that previously represented weeks or months of supply may now tie up as much as four times the capital. The result is additional pressure on the balance sheets of distributors, PCB manufacturers, CCL producers, and OEMs alike. For many organisations, access to material may not be the only constraint and could become an equally important competitive differentiator.

In these situations, financial risk also increases, so greater vigilance over debtor exposure, credit

EAGLE EXY

HIGH-END EQUIPMENT FOR **BACKDRILLING**
AND **DEPTH DRILLING** APPLICATIONS

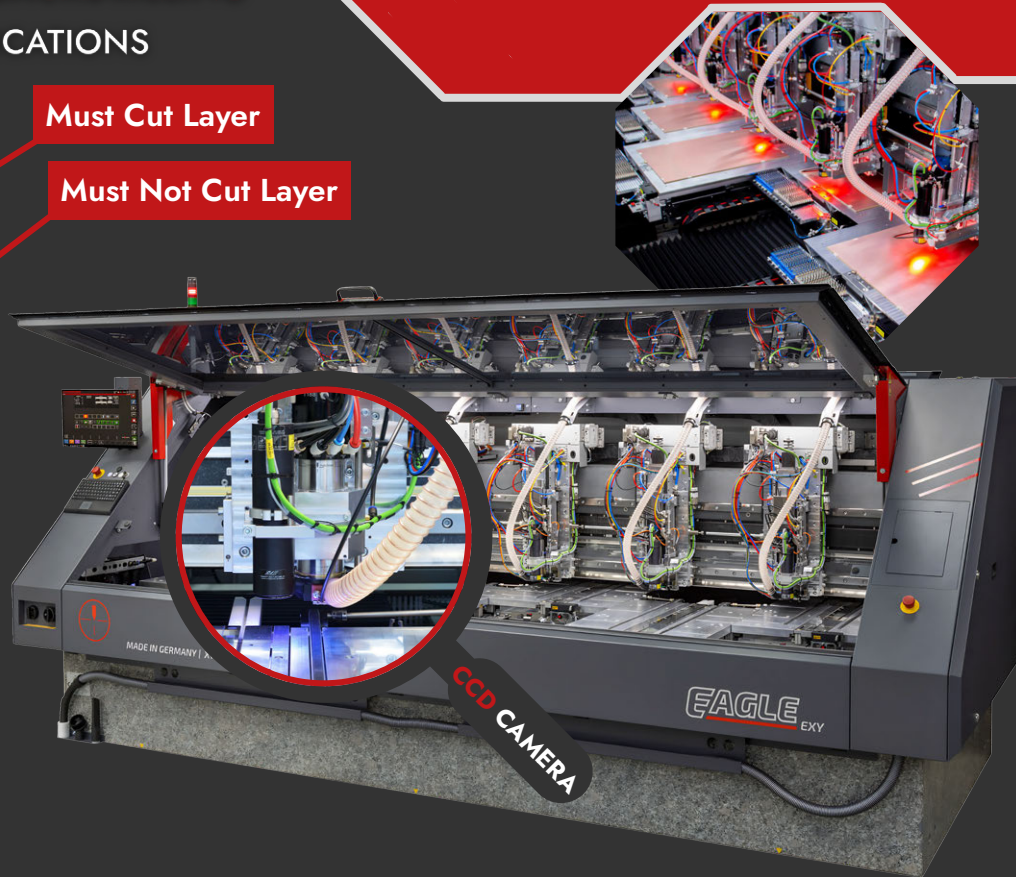


Back Drilling: stop of depth drilled hole before must-not cut layer within stub length tolerance

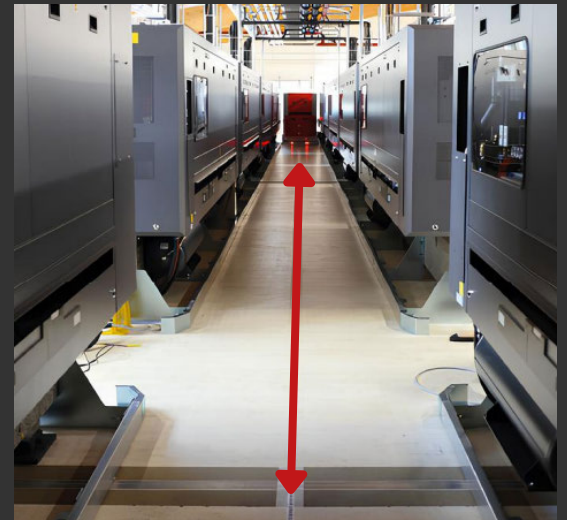


Depth Drilling: precise and reliable drilling to defined inner layers, enabling high-quality blind vias.

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AUTOMATION**



management, and cash flow becomes essential. Organisations that have historically relied on extended payment terms or loosely managed working capital may be difficult to sustain. It is reasonable to expect tighter payment terms, reduced credit availability, and growing pressure to unwind vendor-managed inventory arrangements as suppliers seek to protect liquidity and reduce balance sheet risk.

Rather than material availability, the first signs of disruption may appear in the amount of cash required to secure future supply. Companies with stronger balance sheets, earlier commitments, and closer supplier relationships are likely to gain a significant advantage.

The reallocation of capacity toward higher-growth and higher-value market segments has led to a series of secondary constraints. These effects are often less visible but may ultimately have a broader impact across the PCB supply chain.

How Manufacturers Can Allocate Scarce Materials

As AI infrastructure drives demand for premium materials, laminate suppliers are directing investment, engineering resources, and production capacity toward higher-margin products. The result is that conventional materials can become more difficult to source even as overall industry capacity expands.

Glass Reinforcement

Glass manufacturers are accelerating investment in advanced low-CTE and low loss materials such as T-glass and LK Glass, often using manufacturing assets that would otherwise support conventional E-glass production.

As a result, the industry is seeing:

- No investment in conventional E-glass capacity in Japan and Taiwan
- Growing dependence on Chinese suppliers for new capacity
- Conversion of production resources toward higher-value glass products
- Longer lead times for standard glass yarn and fabric constructions
- Reduced availability of heavier-weight glass styles used in traditional FR-4 laminates

The proportion of glass yarn and fabric available through traditional merchant channels is declining as vertically integrated groups reserve production for internal consumption. This reduces the industry's ability to balance supply through open-market transactions and increases its dependence on a smaller number of integrated supply chains.

Copper Foil and Resin Systems

The same pattern is emerging in copper foil and resin systems. Investment is increasingly focused on VLP/HVLP copper foils and advanced low loss resin systems that support AI, high-speed networking, optical modules, and advanced computing applications. While this expands capacity for premium products, it places pressure on conventional HTE and RTF foils and standard FR-4 systems, which remain essential in PCB manufacturing.

The conflict with Iran adds further uncertainty and risk to an already constrained laminate supply chain. Disruption to energy, petrochemical, and logistics markets puts cost pressure on epoxy resin feedstocks, while separate disruption to bromine and TBBPA flame-retardant supply chains risks further inflation in FR-4 production costs.

Laminate Manufacturer Prioritisation

When glass fabric, copper foil, or resin systems are constrained, manufacturers naturally seek to maximize output, revenue, and contribution from the limited resources available. Historically, shortages have often resulted in the prioritisation of the highest revenue contribution per unit of constrained raw material consumed.

This is particularly relevant in glass fabric shortages. A fixed quantity of glass fabric can typically generate significantly more square metres of thin laminate or prepreg than thick laminate products. Manufacturers, therefore, have a strong economic incentive to allocate constrained materials toward products that maximize throughput, revenue, and profitability.

This allocation behaviour illustrates why current market conditions appear less like a conventional cyclical upswing and more like a structural supply chain realignment. Even with new capacity, the demand for AI infrastructure and continued upstream constraints is likely to keep supply-demand imbalances in place for years.

Several indicators support this assessment:

- Multiple rounds of price increases across the supply chain
- Extended lead times for both standard and advanced materials
- Significant stockpiling activity across the supply chain
- Major capital investment programmes by laminate manufacturers and upstream raw materials producers
- Continued reports of raw material shortages and allocation enforcement
- Ongoing acceleration of AI-driven demand

Even with additional capacity throughout the supply chain, demand growth appears to be outpacing the industry's ability to respond.

Preparing for a Prolonged Supply Constraint

The key challenge is shifting from price management to supply assurance. Transactional purchasing models, short forecast horizons, and single-source material strategies are becoming riskier as availability replaces price as the industry's primary constraint. Companies that secure allocation, maintain material optionality, and engage proactively with suppliers will be better positioned than those relying solely on price-driven procurement strategies.

Organisations should consider:

- Longer-term forecasting and demand visibility
- Earlier purchasing commitments
- Qualification of alternative materials and suppliers
- Strategic supplier partnerships
- Design-for-availability principles during product development
- Ensure sufficient working capital to support higher inventory values and longer procurement cycles



The key challenge is shifting from price management to supply assurance.”

The warning signs have been visible for months, but we are likely to enter the most challenging phase in the coming months of 2026, and which will likely persist into 2028. Don't wait. Resilience programmes, material qualifications, and alternative supply chains require time to implement, and options are diminishing rapidly. Those waiting for shortages to become apparent in their own operations may discover that the market has already moved beyond the point at which effective mitigation is possible. **I-CONNECT007**

Resources and Further Reading

Industry Supply Chain and Lead Time Reports

- “AI Demand Tightens CCL Supply, Drives Advance Orders, Price Hikes, and Expansion,” TrendForce, May 5, 2026.
- “Global Shortage of Glass Fiber Cloth Continues,” by Raymond Goh, CONFIDEE, March 4, 2026.
- “How OEMs Can Navigate AI-Driven PCB and CCL Supply Constraints,” Vexos.
- **Market and Capacity Expansion Information:** EMC Investor Relations
- “Laminate Industry Capacity Expansion Reporting,” DigiTimes.
- **Industry Associations and Market Data:** Taiwan Printed Circuit Association and Global Electronics Association.



Mark Goodwin is chief operating officer, EMEA & USA, Ventec International Group.

VeCS HDI Process Technology

Has the Time Come for Broader Adoption?

Editor's note: Vertical conductive structures (VeCS) is a PCB fabrication approach developed by Joan Tourné, CEO of NextGin Technology. By replacing many of the sequential-build processes associated with stacked microvias, VeCS offers PCB fabricators a potentially simpler manufacturing approach to HDIs. The technology can reduce or eliminate multiple lamination cycles, ease some stackup constraints, and achieve greater vertical interconnect density while leveraging conventional PCB fabrication equipment and processes.

Yet, in some circles, VeCS is controversial. More than five years ago, we took a hard look at VeCS, but in our industry, that is a long time. Every layer interconnect (ELIC) is experiencing broader adoption in HDI builds, but it also carries significant processing and reliability challenges. In this article, Tourné re-examines VeCS, explaining the how and why, and expanding on its pros and cons.

Packaging Trends Driving PCB and Substrate Technology

Packaging technology has always driven the PCB, but today's AI and high-performance computing devices are accelerating that relationship. As compute density, bandwidth, and power requirements increase, package, substrate, and PCB design become more interdependent.

Modern AI processors, such as NVIDIA's Blackwell architecture, require thousands of package connections, support multiple stacks of high-bandwidth memory (HBM), and can dissipate as much as 1,000 watts of power or more. These demands are driving new approaches to package substrates, redistribution layers (RDLs), thermal management, and PCB fabrication, where manufacturing itself is becoming a limiting factor. As bandwidth increases and tolerances tighten, maintaining acceptable production yields with conventional PCB processes becomes more difficult. Testing every high-speed

node is both costly and technically demanding, and requires sophisticated equipment and specialized expertise.

For some applications, RDLs with pitches approaching 150 μm and below provide sufficient interconnect density. As previously discussed, technologies such as VeCS are one such approach, as they increase vertical interconnect density while leveraging largely conventional PCB manufacturing processes.

Signal and power performance are the key drivers toward adopting advanced process technologies. As the bandwidth/frequencies climb, building a perfect transmission line is a significant challenge. Not Df and Dk values so much as minimizing reflections and GND return paths—tuning impedances to minimise the reflections from component to component. These optimizations are done in 3D field solvers that address and tune every element in the transmission line: pad sizes, antipads, inductance, capacitive responses, etc.

Ultimately, advanced packaging is no longer simply about connecting silicon to a circuit board. It has become a multidisciplinary optimization exercise that balances electrical performance, mechanical reliability, thermal management, manufacturability, and cost. As system complexity increases, innovations in both packaging and PCB fabrication will play an equally important role in enabling the next generation of electronic systems.

The Benefits of VeCS for HDI PCB Fabrication

VeCS was developed as an alternative means of providing interconnection for large form factor, very high layer count bare PCB products (a minimum of 24 layers). A more traditional HDI approach requires complex builds with multiple lamination cycles (e.g., 24 + 20 layers) to increase the vertical interconnect density per unit area.

VeCS avoids the multiple lamination cycles that not only add tremendous time to the product build but also creates potential reliability issues due to material movement and tight cumulative tolerances. VeCS gets around the need for such complex builds, requires less experimentation with new materials, and lessens the need for extraordinary efforts toward copper balancing to achieve the surface flatness required to mount large size BGAs.

Building such high layer counts in traditional HDI fabrication through many lamination cycles will always be an option for fabricators and will, indeed, be the most appropriate option in specific cases, but that method tends to produce lower yields, especially where the physical dimensions of a typical backplane board built using VeCS are large form factor and only one or two up on a panel.

VeCS Slots Allow for Better Plating Coverage

HDI fabrication has always had hard limitations due to a microvia's aspect ratio and the limits of wet-chemistry exchange in blind holes when the depth exceeds the hole's diameter, i.e., when aspect ratios are high. Talented industry engineers have been trying to overcome this issue since the mid 1990s, without much success.

Hence, the development of VeCS, where a blind slot is created adjacent to a blind via hole, and where the slot size allows for better wet chemistry coverage than just the microvia alone. Slots, or cavities, ranging from 2 mm to greater than 3 mm are created, using a venting hole that is flexible in its position at the bottom of the slot. The venting hole supports power integrity as it is connected to the GND shielding of the slot. During the early design phase of our work, we observed that there is often no hard boundary or limit to the placement of a venting hole, which is beneficial.

Another advantage of VeCS is that it helps when you find yourself in a situation where you must compensate for DC and AC losses and match impedances. Naturally, one would want to use thicker and wider traces and create thicker strip-lines. But doing so strictly by manipulating Dk will only get you partway there, and increasing the size of your microvia may not be feasible due to routing constraints.

Figure 2 shows a cross-section of two VeCS stacks, where the slots are filled with a high performance, low loss resin and are overplated. On the right side, this signal shows facing the GND shielding on the left. Also shown at the base of each stack is the zero stub length technology used to stop the signal at the correct layer with no overshoot. This is the same for the bottom GND of the strip line. This enables the area just below the VeCS to be open and available for routing.

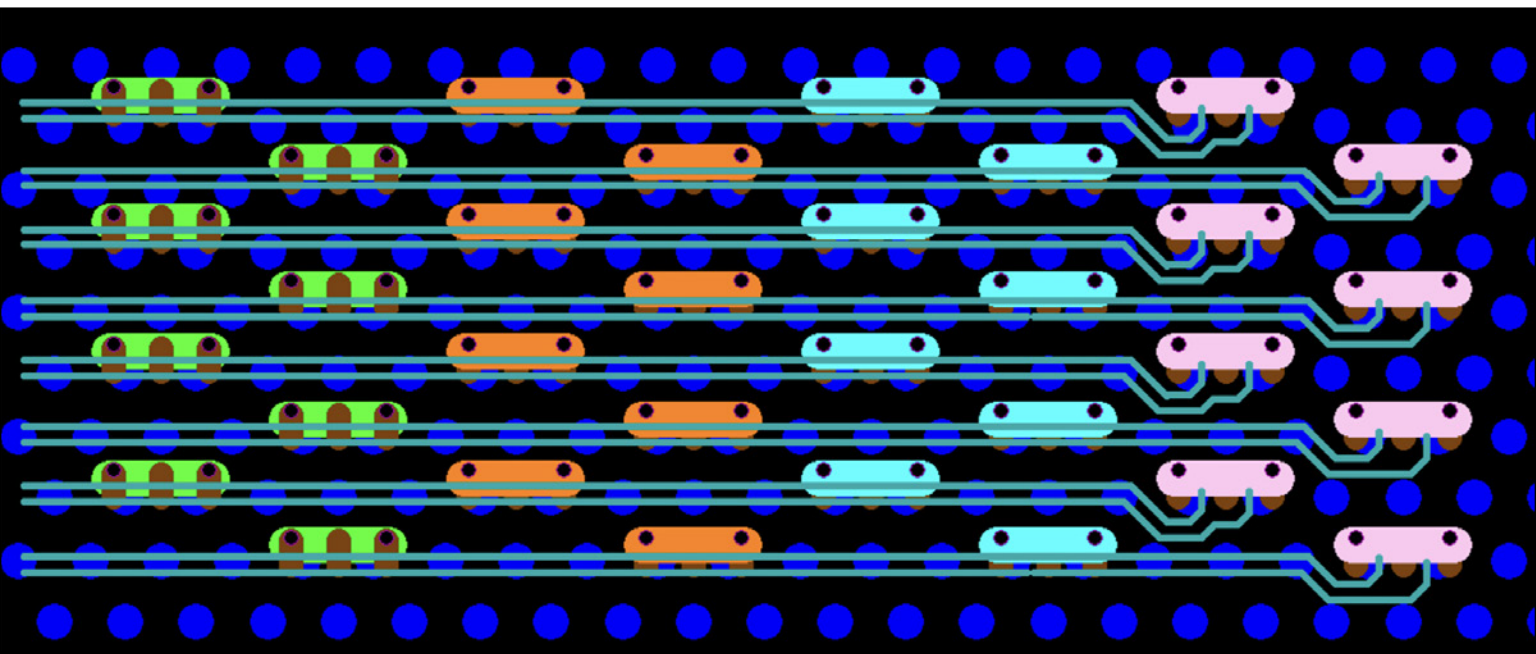


Figure 1: Every color is a different VeCS depth, going from left to right, starting with e.g., Layer 3, Layer 5, etc. The two black holes in the oval-shaped slot are the venting holes. This is no more than a via hole starting at the bottom of the slot and going to the back side of the board/sub-assembly.

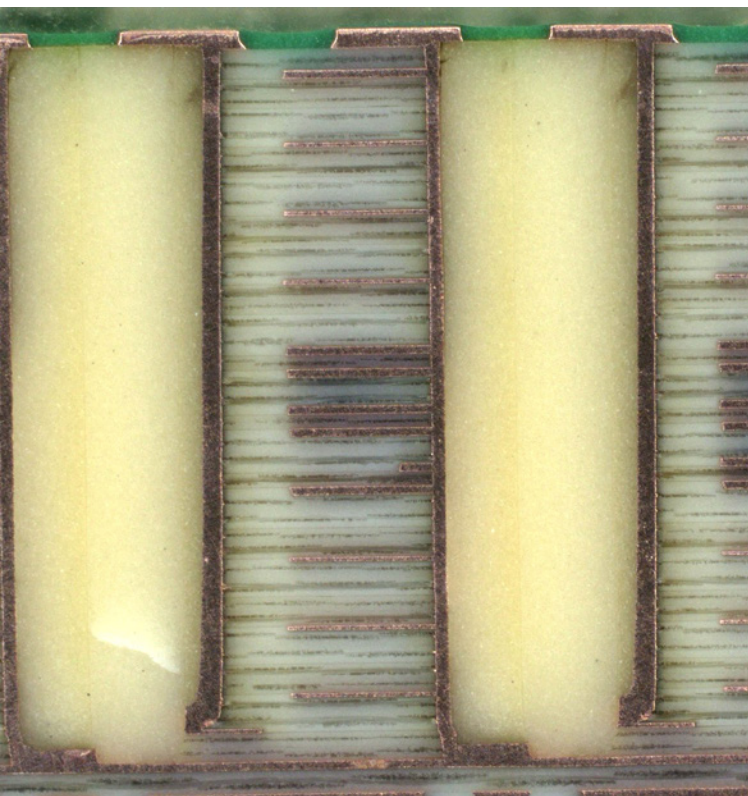


Figure 2: Cross-section of two VeCS stacks. The slot is filled with a high performance, low loss resin and overplated. At the base of each stack is the zero stub length technology used to stop the signal at the correct layer with no overshoot, enabling the area just below to be open for routing.

Disadvantages: CNC Drilling/Routing Time

Perhaps the single greatest disadvantage of the VeCS approach is the amount of time it requires on a mechanical CNC routing/drilling machine, which is relatively slow (when compared to laser drilling), and has always been a traditional manufacturing bottleneck.

For this reason, we have optimised VeCS for faster processing with the introduction of Recessed VeCS (R-VeCS), an evolution of VeCS where two vertical traces are part of plating the primary slot. For this, we can use slightly larger bit diameters, which help feed parameters. It is important to note that for the diameters we are processing, we recommend spindle RPMs of 100k or higher to get optimum chip loads.

After filling and plating, select areas of plating are removed at specific positions to create two vertical traces. With R-VeCS, we create extra slots at the same time the primary slot is created. After plating and face rout, we cut away part of the two smaller slots. This is called a “shielded VeCS.” The two differential contacts face the shielding. These 2.5D–3D structures are becoming more complex, with side and front shielding containing an electromagnetic field within the shielding.

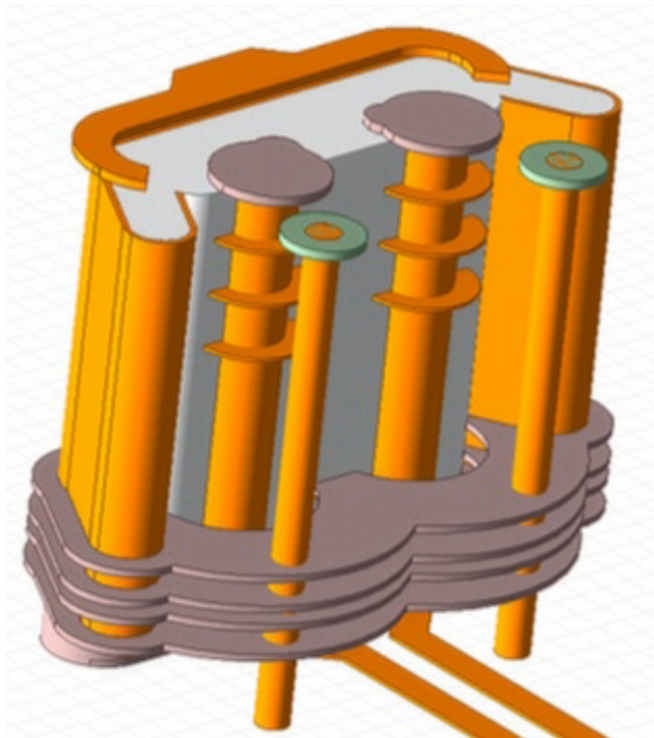


Figure 3: An R-VeCS using side wing shielding and additional pads for compensation of the inductance effect of the differential connections.

Process Steps for R-VeCS

The R-VeCS uses a router bit to form the various elements of the slot. The flow in Figure 4 shows the process without the side wings, but they are added in the first routing step. After plating and filling, the second rout step is removing part of the plat-

ing, creating a shield, and individual contacts. All examples use differential pairs, but a single-ended single-differential is also possible. Having multiple differential pairs in a single slot is also possible, but in high-bandwidth applications, this can create excessive crosstalk, as the electromagnetic wave will travel through the shielded slot to the next pair.

The formation of stubless slots, or contacts, will be made using laser ablation, acting as a self-limiting process that stops at a copper surface.

The correct layer to stop the mechanical formation can be identified through active feedback from the internal contact method. This saves time in setup and achieves much greater consistency in processing.

Optimisation of the TDR Response of the R-VeCS Using Side Wings

In Figures 5 and 6, the green line is without the optimisation, showing a high inductance response due to the half-vias. The blue line is an optimisation after adding extra capacitance across the length of the half-vias. The TDR behaviour is directly improved.

The capacitive spike after the half-via is the bounce pad at the bottom of the half-via. There are different ways to eliminate this effect. One option is to make an opening below the bounce pad in the GND plane. Depending on the stripline routing shown below, this can affect crosstalk and imped-

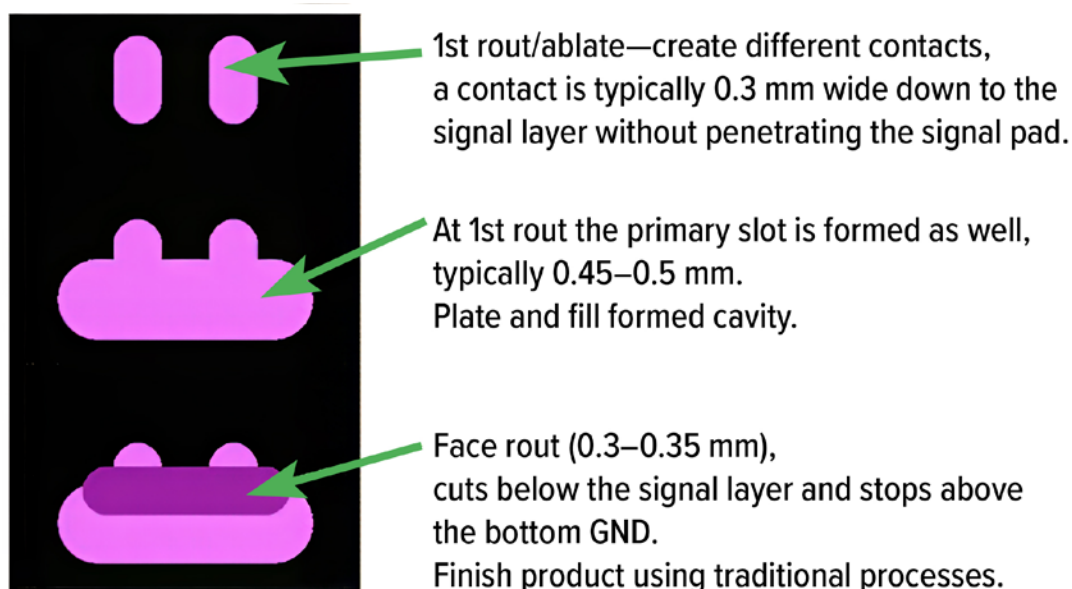
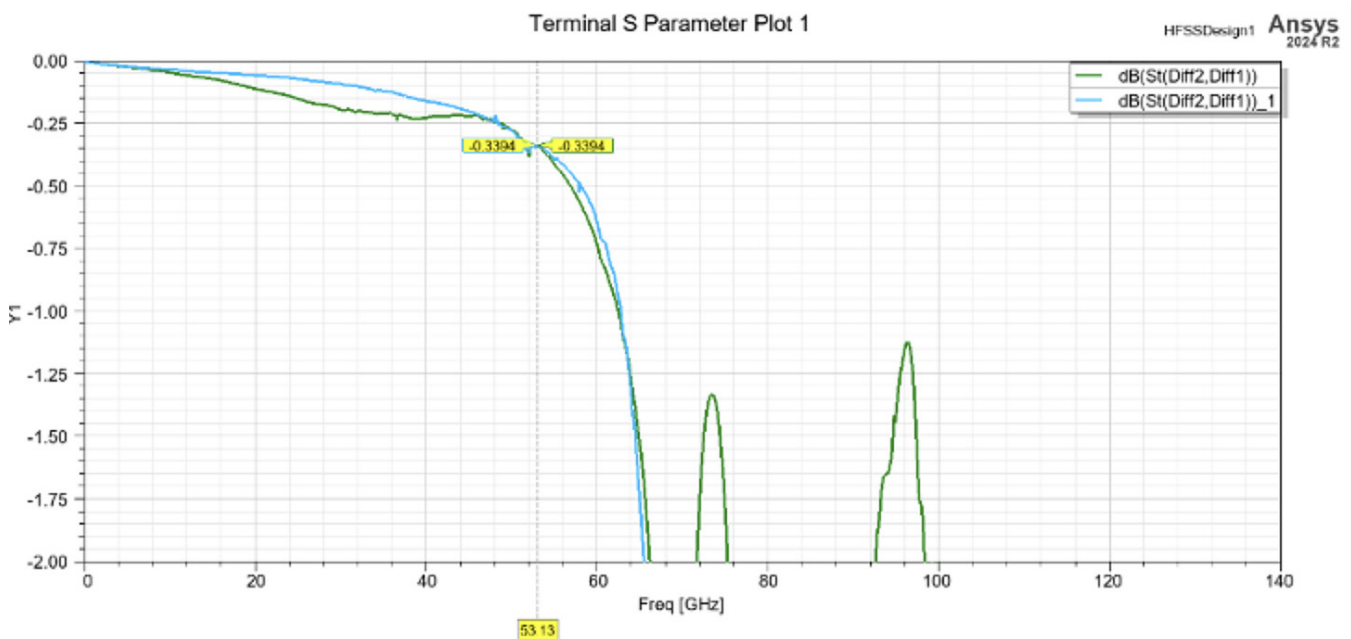
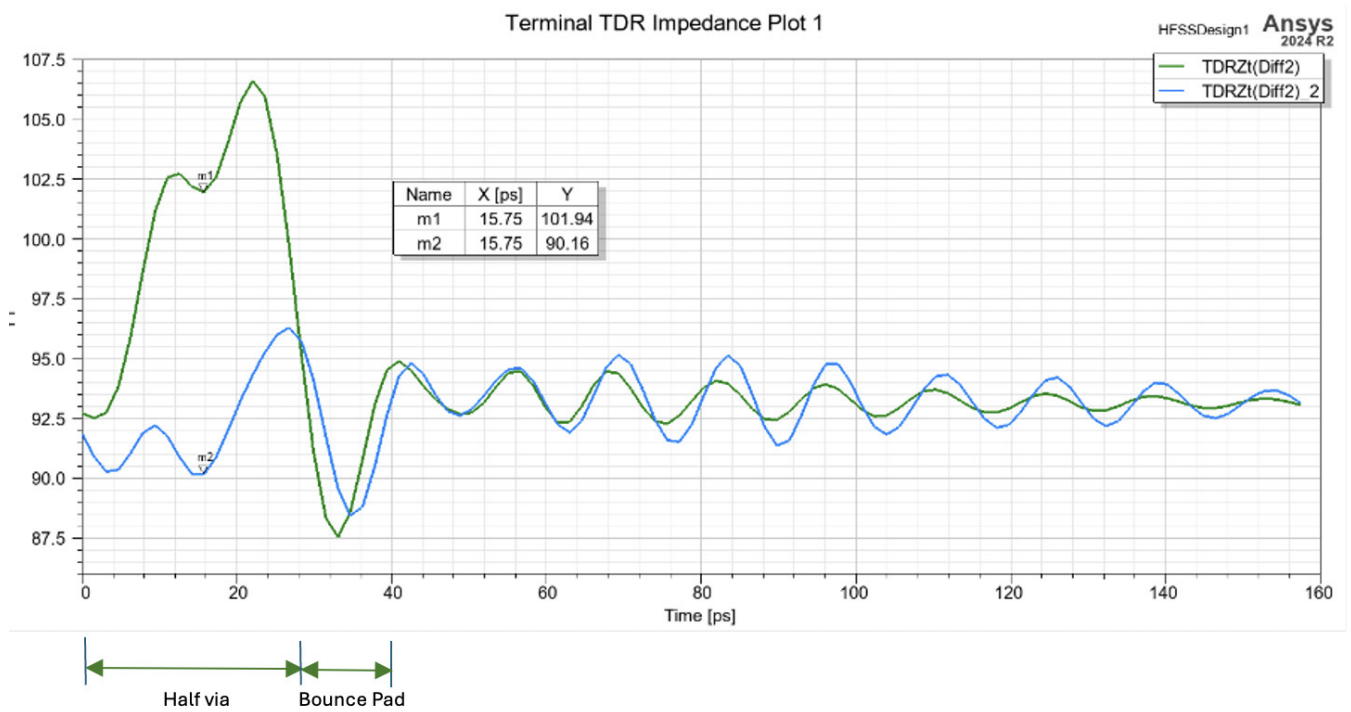


Figure 4: Forming the R-VeCS.



Figures 5 and 6: Optimization of the TDR response of the R-VeCS using side wings and measurement of insertion and return loss.

ance when a trace runs below the opening in the GND plane.

The TDR is optimized to the loss parameters, S21 and S11, insertion, and return loss can also be calculated for near-end and far-end crosstalk (NeXT and FeXT).

In Figure 6, the insertion loss plot of the optimized 2.4mm deep structure R-VeCS. The loss is reduced between the 20 and 50GHz mark after adding

capacitive elements to the half-via. The response became smoother as well.

We also see that the cut-off frequency becomes evident around 60 GHz.

SI Performance of R-VeCS

The application area for R-VeCS is shown up to 60GHz. This is defined by the inductive and capacitive values of the construction. It can be optimized

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to slightly higher frequencies but not where we need to go for the next generation requirements.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The cutoff frequency is determined by various elements, but here, we show the LC combination of the vertical connection is the main contributor. If we want to go to higher frequencies, we need to reduce the LC value. For differential pairs, we want to have a certain coupling which influences the C value.

Aside from capacitance, the slot itself has a limit in terms of resonance. We plotted a graph showing the main resonance as a function of slot length. The slot length is, of course, related to the component (ball) pitch. If we need to go to higher bandwidths, we need to reduce the slot size. The applies for VeCS, but if we were to build a shielding using stitching vias or stacked micro-

vias, this would have a similar response.

We see the trend to smaller pitches driven by the required bandwidth. For the large ASICs, we see trends below 0.5 mm, including the connectors required to achieve the bandwidths. This will drive PCB technology further and will do so relatively quickly.

The limit for R-VeCS in terms of physical dimensions (in thick/high layer count boards) is around a 0.5 mm. We have developed a modified approach, X-VeCS, for technologies below 0.6 mm down to 0.12 mm, created using a laser, and often with milling.

Reliability Studies and Results

IST reliability studies have been performed on every batch of VeCS and R-VeCS product we have manufactured. (X-VeCS is still in the early stage of R&D, so IST reliability studies have not yet been conducted.)

Starting with blind VeCS-2, we saw that the hole wall roughness affected the reliability of the copper plating. Even with thick copper, a rough hole wall with fibers sticking out can lower the number of IST cycles.

The development of R-VeCS creates a kind of half via which shows a very robust hole wall structure.

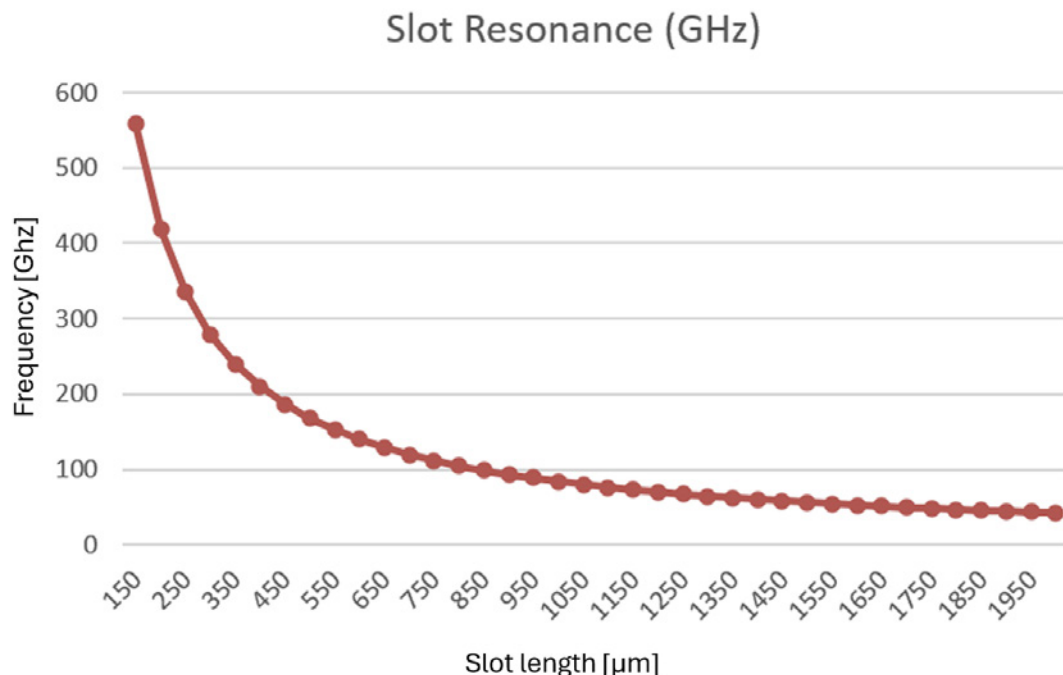


Figure 7: Resonance as a function of slot length.

Overall, the IST testing yielded results equal to or better than those of PTH. All products had a depth of R-VeCS up to 3.0 mm and showed high reliability.

X-VeCS HDI Process Technology for Small Pitch Devices

Best Fit Applications for VeCS

Though most of our work at NextGin has been performed on backplane type PCBs—large panels, very high layer counts, and thickness—we have begun lower layer counts and smaller form factor projects. As yet, we have not seen a limit in applications using VeCS. Competing head-on with other HDI-type applications, VeCS benefits from fewer lamination and plating cycles, resulting in better yields overall. An additional benefit is that VeCS-constructed inner layers can be repaired in a manner similar to traditional PCB inner layers. Signal performance for traditionally constructed HDI PCBs and those constructed by VeCS is similar.

Therefore, we can expect to see competition between the two technologies over the next few years: traditional HDI multiple-lamination-cycle build-ups and VeCS. It will come down to pricing and total cycle time.

X-VeCS for Smaller Pitch Devices

The reason we address inorganic materials is that these new materials are difficult to use, as no B-stage versions are available for building ELIC HDI-type constructions. We call these constructions N+1, adding one layer (one each side) per lamination cycle. This technology has some great advantages, but the problem of yield is a big one, as is writing off all that added value when a defect occurs.

The same construction can be made with X-VeCS with less lamination, drill and plating cycles.

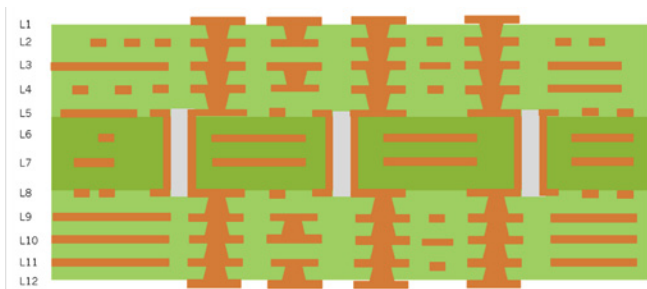


Figure 8: A traditional N+1 construction build-up on a 4-layer core requires five lamination, drilling, and plating cycles.

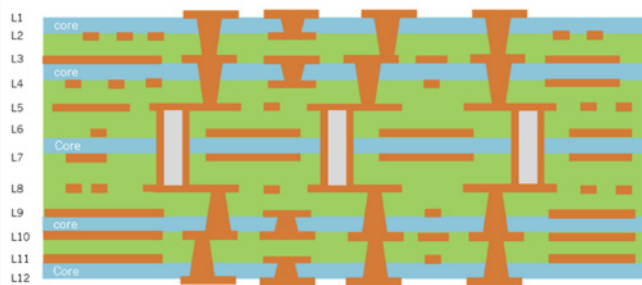


Figure 9: The same construction in N+2. This construction required three lamination, drilling, and plating cycles.

X-VeCS for Fine Pitch, Small Form Factor

The principle of processing X-VeCS is similar to that of R-VeCS. For X-VeCS, we create one or multiple slots. In this case, we do so in the form of an X, but it can be done in any other shape. We form the slot, plate, and selectively remove parts of the slots to create individual contacts. There is flexibility in the number of contacts, the shape of the VeCS, the depth, the shielding shapes, etc.

The differential signal connections are placed on the right side of the X, where the left side of the X is connected to the GND below. So, we have two different depths in the X. The X is shown as a full connection except that when finished, it will have two endpoints at the end of the signal slots. For the GND connection, we can leave the legs on so they can carry more current.

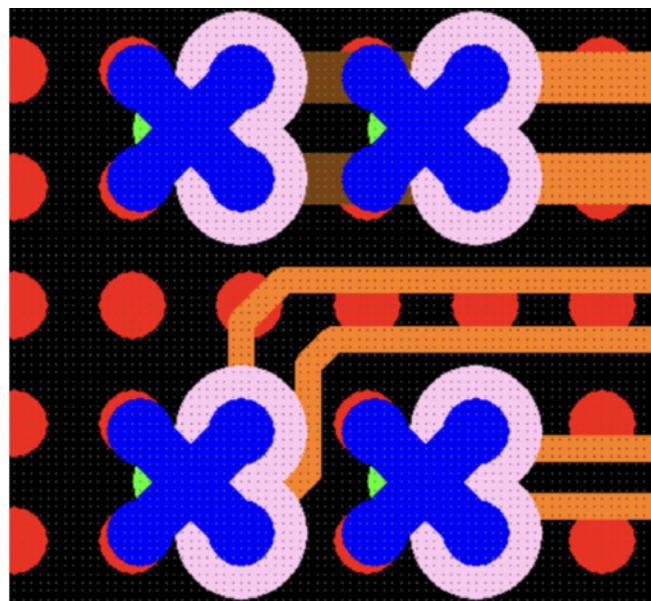


Figure 10: The X-VeCS in a design example. Notice that we are varying the trace width and using different routing schemes. We are not showing the GND connections and GND shielding in these images.

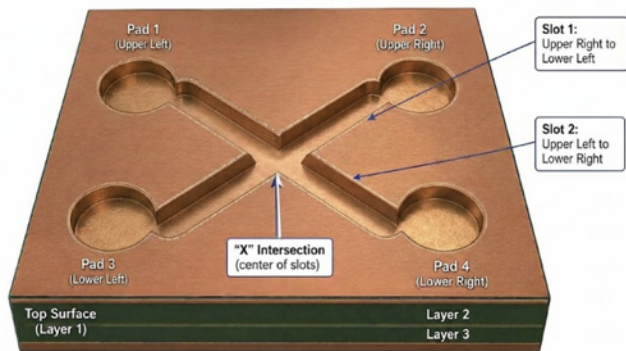


Figure 11: Step 1 of the X-VeCS process: Cross slots machined and pads positioned at ends of the X slots.

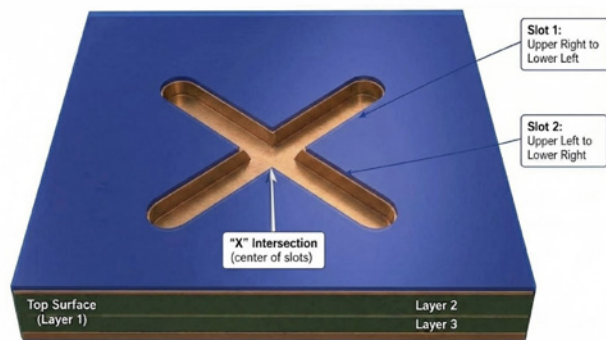


Figure 12: Step 2 of the X-VeCS process: A blue solder resist layer has been applied, covering the top copper surface and removing the pad structures. Only the surfaces within the two diagonal slots (Slot 1 and 2) are left uncovered and exposed.

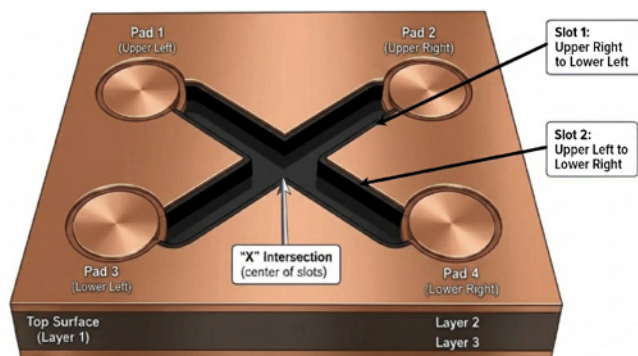


Figure 13: Two diagonal slots are machined to form an X shape. Four circular BGA pads are positioned at the distal ends of the formed X pattern.

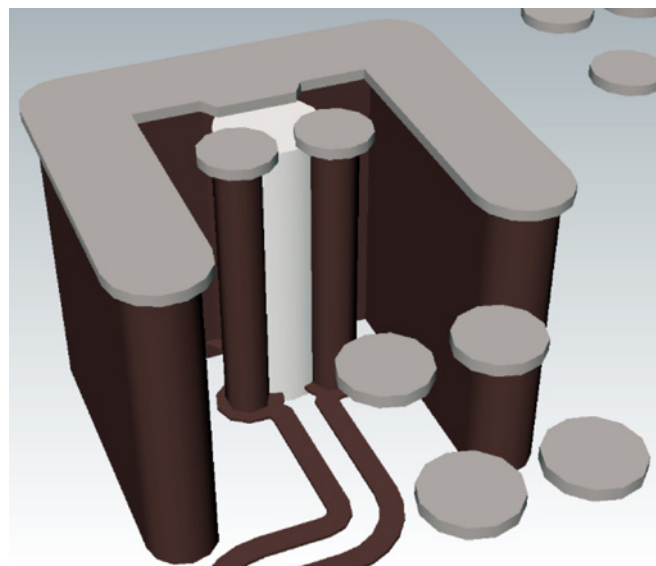


Figure 14: Example of X-VeCS showing a differential pair surrounded by shielding.

We show the X-VeCS process steps in three major steps. In this example, we do not show the multi-depths per X-VeCS. The depth of the X-VeCS would not go below the bottom GND of the strip-line. With this depth in the design, we can choose to drill the GND positions all the way through the board or sub-assembly.

The complexity of X-VeCS is not as much in processing as in the design. We use traditional machines and processes to build VeCS. Equipment needs to be set up for the specific task, but that is not different from traditional processes. For the people starting with it, you can always contact us for questions. For a fee, we can lead projects, perform design, and assist on the side in process set-up for these activities.

Acknowledgements



Joan Tourné

I want to thank WUSTEC for their years of cooperation in developing VeCS technology. In cooperation with OEMs and ODMs, they are becoming a centre of expertise for high bandwidth applications in signal integrity and power integrity.

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American PCBs in Big Demand and Short Supply



BY SHANE WHITESIDE, PCBAA

The PCB industry faces challenges that are only now being recognized by government agencies. Against the backdrop of conflicts in Europe and the Middle East and the ongoing threat of Chinese business and military aggression, the microelectronics industry overall has been upended.

American PCB production has been hit especially hard. This happened because of a combination of

three decades of offshoring, fighting for market share against heavily subsidized Asian countries, single sources of key inputs, and facing conflict-driven chokepoints across the supply chain.

Much has been written about the offshoring of the industry and the unfairness of American companies competing with other countries. Likewise, single sources like copper and woven glass have received attention.



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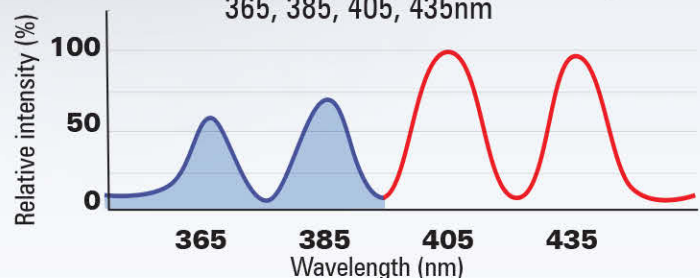
4 Smart Automation
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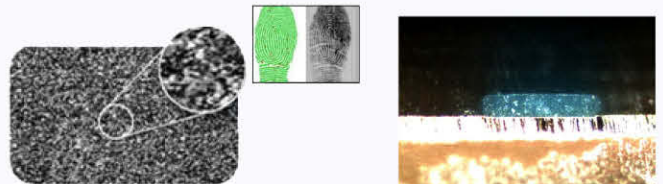
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There is another major factor getting renewed focus at the Department of Defense (DoD): supply chain security. U.S. defense and critical infrastructure systems too often depend on foreign components. Some are benign and can be safely integrated into these systems.

However, there are four countries where components are prohibited. Section 841 of the National Defense Authorization Act (NDAA) for FY 2021 and section 851 for FY 2022 require the DoD to mitigate supply chain risks by prohibiting the procurement of PCBs from entities located in or controlled by these four nations: The People's Republic of China, the Russian Federation, the Islamic Republic of Iran, and the Democratic People's Republic of North Korea.

To take steps to remove PCBs from those countries, Congress required DoD to have a plan by Jan. 1, 2027, to implement this prohibition by focusing on where bare PCBs or partially manufactured boards are made. DoD is in the process of establishing trusted supply chains and operational security standards for the procurement of microelectronics and their associated PCBs.

As DoD prepares to comply with the NDAA, PCBAA and our member [companies have until Aug. 31, 2026, to comment](#) on how this can be best executed. We encourage every company with a defense business to comment so that DoD can implement the best rules and regulations. American industry is ready to get China out of our supply chains, and we need to provide DoD with our best counsel on smart compliance with this important regulation.

PCBAA is also in constant dialogue with the Department of Commerce and other executive branch agencies to help reshore and restore the American PCB industry. Join us today to continue to fight for our industry. **I-CONNECT007**



Shane Whiteside is chair of the Printed Circuit Board Association of America and president and CEO of Summit Interconnect. To read past columns, [click here](#).

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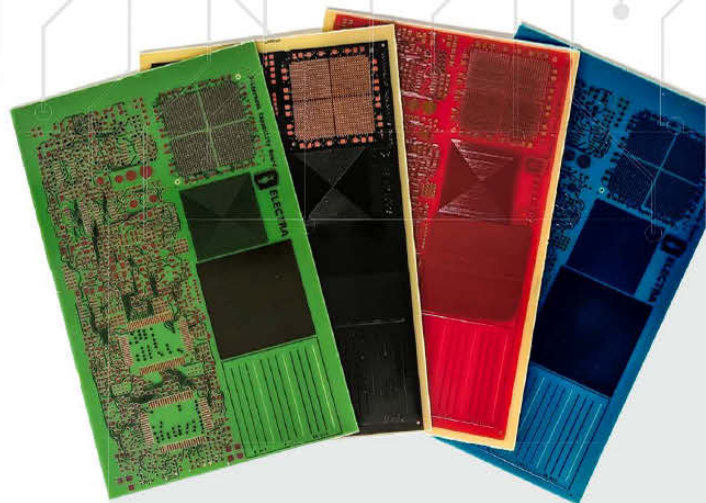
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- Ink stable under a range of temperatures and environmental conditions
- No change in ink viscosity or particle size during use or shelf life of product
- Ink robustness critical for ensuring consistent printing with minimal problems
- Approved for use on leading inkjet printheads:
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 - Konica Minolta – KM1024iSHE
 - Konica Minolta – KM1800i
 - FUJIFILM Dimatix – Samba®

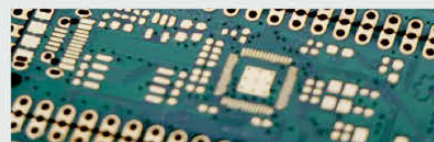
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AS9100D and PCB Fabrication: What Supplier Quality Should Evaluate ►

When a supplier quality engineer supporting aviation, space, or defense programs reviews a new PCB fabricator, one of the first checkpoints is simple: Is the AS9100D certificate current? That is an appropriate starting point. In regulated aerospace environments, configuration control, traceability, corrective action, and internal audit discipline are not optional.

Defense Speak Interpreted: Will Defense Become a Totally New Supplier for Drone Electronics? ►

When I recently read that Tobyhanna Army Depot would begin manufacturing up to one million circuit cards annually for military drones, I immediately wondered whether this opens a whole new chapter in volume electronics manufacturing within Defense. Historically, Defense has had access to some aspect of printed circuit production. My research confirmed what I already knew from my own experience as a subcontractor to the Naval Surface Warfare Center Crane in Indiana.

dSPACE Achieves CMMC Level 2 Certification ►

dSPACE, a global leader in simulation and validation solutions for the development of embedded systems, announced that it has successfully achieved the U.S. Department of Defense's Cybersecurity Maturity Model Certification (CMMC) Level 2. This achievement reinforces the dSPACE commitment to protecting Controlled Unclassified Information (CUI) and supporting the cybersecurity objectives of the U.S. Department of Defense (DoD).

TrueMark Investments Expands FLDZ Focus with Dedicated Defense and Aerospace Strategy ►

TrueMark Investments announced enhancements to FLDZ, now the TrueShares Patriot Defense ETF, providing investors access to companies across the defense and aerospace ecosystem while continuing its distinctive commitment to supporting the mission of the Folds of Honor Foundation

by donating the entirety of the fund's management fee, less operating expenses to the cause. The fund continues to trade under ticker FLDZ.

Airbus Awarded Contract for SpainSat NG-III Secure Communications Satellite ►

Airbus Defence and Space has been awarded a contract by Hisdesat to act as prime contractor for the development and construction of SpainSat NG-III, Europe's most advanced secure communications satellite.

U.S. Marine Corps MV-22 Program of Record Reaches Milestone ►

Bell Textron Inc., a Textron Inc. company, and Boeing celebrate the achievement of the MV-22 Program of Record (POR) for the U.S. Marine Corps (USMC). Bell and Boeing commemorated the V-22 Osprey production milestone during a ceremony at the Bell Amarillo Assembly Center on July 28.

Astro Digital Selects Everspin 64Mb STT-MRAM for GEO Satellite ►

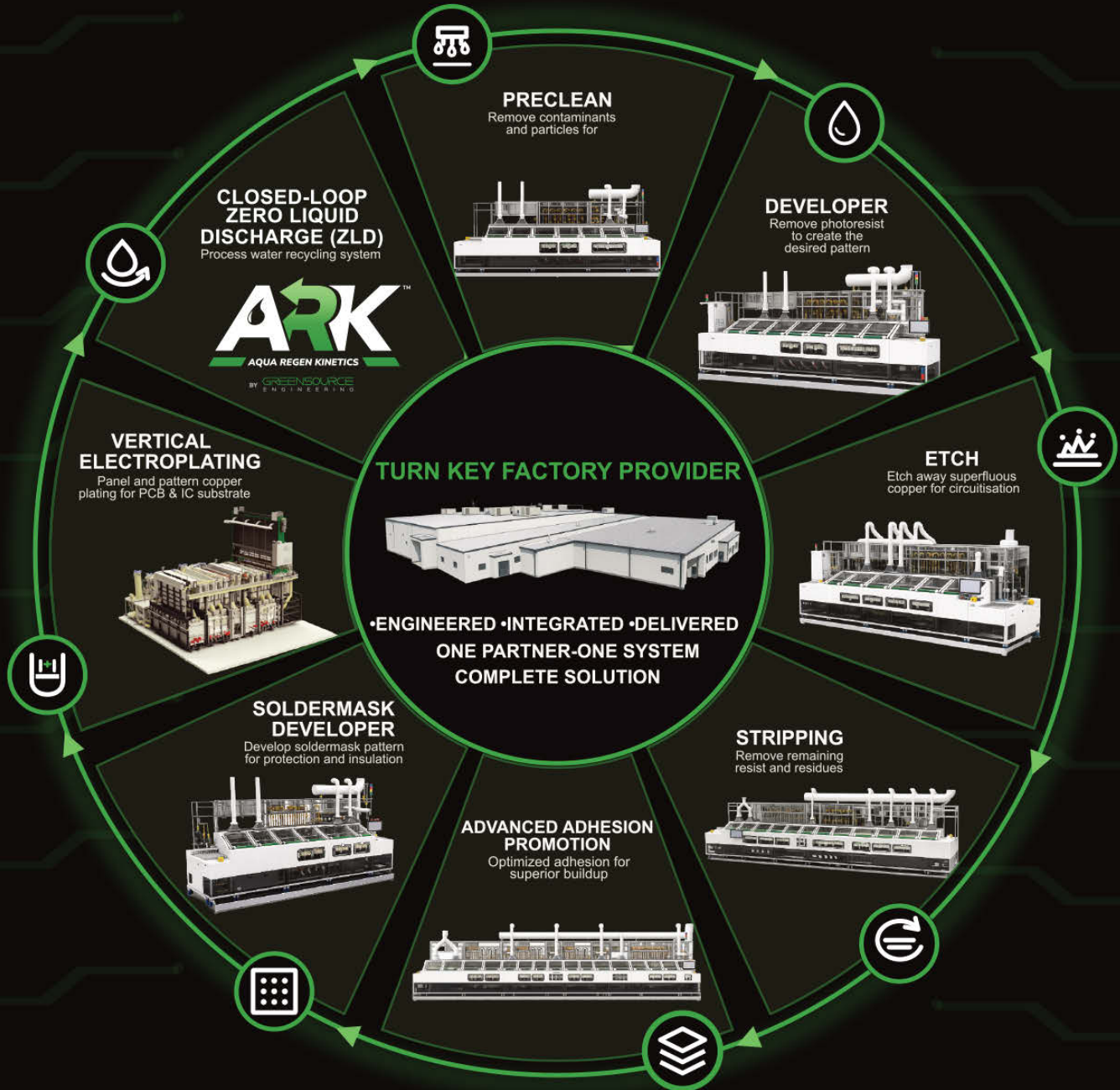
Everspin Technologies, Inc., the world's leading developer and manufacturer of Magnetoresistive Random Access Memory (MRAM) solutions, announced that Astro Digital has selected Everspin's PERSYST 64Mb STT-MRAM for use on an upcoming Raven bus geosynchronous Earth orbit (GEO) satellite mission.

CACI Continues Modernization of U.S. Navy's Military Sealift Command's Integrated Business Systems ►

CACI International Inc has been awarded a five-year technology contract valued at up to \$113 million by the U.S. Navy's Military Sealift Command (MSC) to continue modernizing a portfolio of mission-critical business applications used by both ashore personnel and MSC's global fleet. "The Military Sealift Command plays a vital role in sustaining U.S. and allied operations around the world, and CACI is proud to continue supporting that mission," said John Mengucci, CACI president and chief executive officer.

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What PCB Designers Should Know *About Materials*



BY MATT STEVENSON, ASC SUNSTONE CIRCUITS

What questions does your manufacturer ask when they receive a design? I can tell you one: “How will we build this?”

Every PCB design has specific parameters for elements such as impedance, thermal conductivity, and SI. Designers choose material properties based on the functionality requirements of the boards they design. Does the PCB have to operate in high heat? Be flexible enough to fit into a tiny device, such as a wearable? Maintain SI without distortion or data degradation?

These are important, foundational considerations for designers. I believe it is also important for designers to consider how a manufacturer thinks

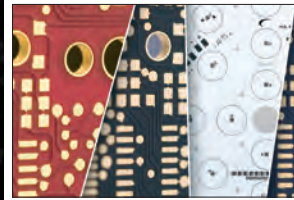
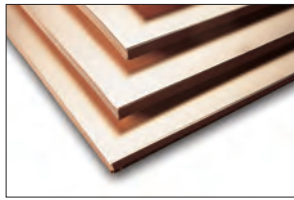
about materials. PCBs are manufactured using layers of conductive materials, surface coatings to protect conductive layers from oxidation, and substrates. The materials dictate the board's flexibility, heat dissipation, and electrical performance.

So, it's important for designers to match design requirements to the manufacturer's list of materials available for production. Those materials represent a means to an end—the smooth, cost-effective production of a reliable PCB that meets the designer's requirements. In general, a longer list is better.

More complex designs, boards, and electronic devices mean material requirements must expand and diversify. Designers working in product devel-

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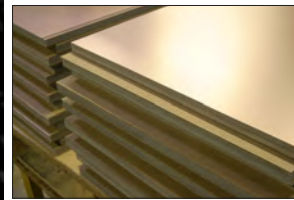


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Coatings



Electro-deposited
Copper Foils



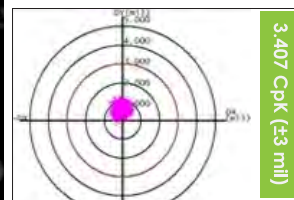
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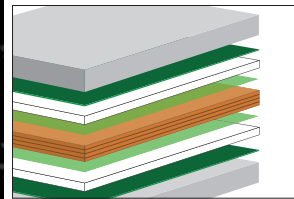
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opment are often called upon to create a wide variety of boards, everything from specialized RF and microwave boards to rigid, flex, and rigid-flex circuits. In those situations, it helps to have a manufacturer with experience in the wide universe of substrates, sizes, and shapes.

Materials manufacturers generally offer similar options for conductors (copper, aluminum, gold, and silver) and surface finishes (e.g., solder mask, nomenclature, HASL, and ENIG).

Things get a little trickier when it comes to substrates, the insulating base material that serves as the foundation for a PCB. A substrate is non-conductive, provides mechanical support to hold electronic components in place, and acts as an electrical insulator to maintain signal integrity.

Breaking Down the Types of Substrates

PCB designers generally know how substrate materials can affect a board's electrical, thermal, and mechanical performance. The material properties you choose determine signal integrity, impedance, heat dissipation, and reliability under thermal stress.

There are several commonly used substrates in PCB manufacturing. They include:

FR-4 Fiberglass

Commonly used for rigid, multilayer PCBs found in laptops and consumer electronics, FR-4 is composed of woven fiberglass cloth bonded with an epoxy resin. It is favored in these applications for its durability, electrical insulation, and cost-effectiveness.

High Speed Materials

Materials geared toward high speed designs make sense where signal integrity is important. These include PTFE, modified epoxies, and laminates that blend ceramic with hydrocarbon resins. All are expensive compared to standard materials, but they offer improved SI, as well as minimized distortion and signal loss.

Polyimide

If you are designing a flexible PCB, chances are polyimide will be the substrate of choice. Polyimide is comprised of resins instead of epoxies, allowing the board to bend and fold into tight spaces without

breaking. It is also lightweight and can withstand extreme temperatures, making it ideal for aerospace applications, motor vehicle electronics, and ultra-compact medical devices.

Metal Core

This substrate is structurally tough and dissipates heat more effectively than other materials. Made from aluminum, copper, or steel, metal core PCBs are often found in high-powered, commercial-grade electronics, high-frequency RF applications, and durable military hardware.

PTFE and Ceramics

For high speed and high frequency RF and microwave applications that require PCBs operating with minimal signal loss, delay, and distortion, there are two primary substrate material classes. They are PTFE (polytetrafluoroethylene, also known as Teflon®) and ceramics.

Both feature very, very low dielectric loss and offer stable dielectric constant at high frequencies, making them ideal for antennas, high-speed data networks, and aerospace applications.

Evaluating Material Properties

For PCB designers, choosing materials depends on how and where the board will operate. Sometimes, it is easy to choose. Other times, it's more nuanced. Design considerations include:

Cost

Though I often see this at the bottom of the list of evaluation criteria, the cost to produce a PCB can make or break product development. Specialty materials like polyimide are considered premium for a reason. They are not cheap. During design and prototyping, if your device's application does not clearly require specialty materials, it can be worthwhile to test the feasibility of cost-effective FR-4.

Electrical Performance

Electrical performance is another important attribute for material selection. The primary considerations regard signal integrity and power distribution. Your choice of substrate directly determines how fast and cleanly signals travel across your circuit.

Heat

Is your board going into space? After assembly, will it have a slew of hot components? I encourage designers to carefully evaluate the temperatures their boards will operate in. High heat environments or multiple soldering passes during assembly can cause certain substrates to soften or expand. It's also important to recognize how much heat components will create and if those temperatures will make one substrate preferable to another.

Strength

A board's strength is measured in many ways, but all those measures essentially pertain to the board's durability. It is important to choose substrates that will ensure the board can withstand everything the environment throws at it. This is especially so for flexible PCBs and those subject to vibration or repeated impacts that are often present in military and aerospace applications. Another consideration is excessive moisture absorption that can degrade board performance.

Availability

Substrate availability issues are becoming more common due to increased demand created by AI-related build-out and geopolitical disruption. Lead times are longer now, and substrate costs are increasing, sometimes even for standard materials. This can extend product development windows and drive up the cost of going to market. We encourage designers to consider materials availability in their design choices.

Manufacturability

Manufacturability is a key concern equal to cost considerations. FR-4 is the go-to for ease of manufacture. Every PCB fabricator works with it. But more designs are requiring other substrate materials that not every manufacturer can offer. Choosing the right manufacturer, one knowledgeable and experienced in the array of substrate materials, ensures the design is functional and structurally reliable, while also helping avoid manufacturing issues.

Why It Is Important to Choose Substrate Wisely

Choosing the wrong PCB substrate can lead to everything from manufacturing failures, such as rework

or reduced yield, to boards that operate with excessive signal loss, are susceptible to thermal damage, or are prone to mechanical breakdown in the field.

Signal Integrity Issues

If you are designing boards for RF or high-frequency applications, choosing FR-4 can lead to a slew of issues in the field. FR-4 is a solid, cost-effective base for basic circuits, but it opens the door for signal loss, signal reflections, data corruption, and electromagnetic interference (EMI).

Thermal Failures

If your board needs to operate in a hot environment and you pick the wrong substrate, the result can be solder joint cracking, warping, component failure, and even a melted board. When choosing a substrate, pay close attention to CTE, Tg, and thermal conductivity to avoid such issues.

Mechanical Failures

Polyimide is your best bet for applications requiring a board that can bend or flex. Using rigid materials in these instances can lead to delaminated circuits and broken copper or even cause the board to snap. But if your board is designed for structurally rigid application, flexible material will not work because of challenges associated with securely mounting components.

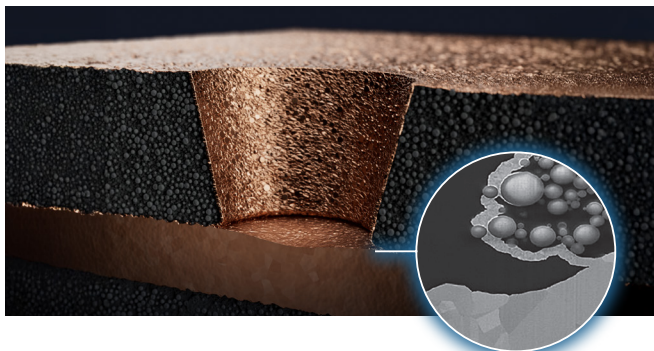
When your manufacturer gets the first peek at your requirements and design, their job is to ask, "How will we build this?" With modern materials and manufacturing techniques, more is possible than ever before. A good manufacturing team has the experience and capacity to help you select the materials that are optimal for your project. **I-CONNECT007**



Matt Stevenson is vice president and general manager of ASC Sunstone Circuits. To read past columns, [click here](#). Read Matt's book, *The Printed Circuit Designer's Guide to ... Designing for Reality* and listen to his podcast series [here](#).

Electroless copper for advanced packaging – From ultra-thin deposition to process flexibility

As advanced packaging architectures continue to push the limits of miniaturization, electroless copper deposition has become essential for sub-5 μm line-and-space designs. Meanwhile, manufacturers are facing increasing variability in dielectric materials, feature geometries, and thickness requirements. The question is no longer just how to achieve ultra-thin copper, but also how to do so with sufficient flexibility to support a broad range of process conditions.



Trends and manufacturing context

Next-generation package substrates demand tighter geometries, improved reliability, and compatibility with low-roughness dielectric materials. Electroless copper plays a central role in enabling SAP-based manufacturing, especially when uniform seed layers, strong adhesion, and reliable microvia coverage are necessary. However, while a single chemistry may meet the challenges of today, it is unlikely to meet the needs of tomorrow. For substrate manufacturers this means that as their technical demands change, they will need to investigate and test new chemical processes, and once a new candidate is identified, follow this with extensive customer qualification.

The solution – A flexible electroless copper platform

MKS' Atotech addresses this challenge with the Printoganth® MV TP3 series, an adaptable electroless copper platform designed for advanced packaging applications. Rather than being a single process, the series offers a flexible approach that supports a wide range of Cu thickness requirements, and by utilizing a common base formulation the process chemistry can be readily simplified to extend capability while minimizing the need for extended testing and re-qualification.

- Printoganth® MV TP3: Ultra-low thicknesses below 150 nm
- Printoganth® MV TP3 Mod: 150–250 nm
- Printoganth® MV TP3 Mod2: Above 250 nm

This flexibility means that manufacturers can retain the familiarity and experience gained when operating at higher deposit thickness

as they progress to the finer line and spaces that are supported by the variants within the Printoganth MV TP3 platform.

Performance and process benefits

Across all variants, the Printoganth MV TP3 series is built on a common performance foundation:

- **Best-in-class bath initiation** with zero dummy plating required, reducing waste and improving efficiency
- **Fine epitaxial crystal growth**, enabled by bottom-up recrystallization, supports reliable interconnect formation
- **Excellent adhesion to low-roughness dielectrics**, which is critical for next-generation substrates
- **Outstanding throwing power** for uniform coverage of high-aspect-ratio blind microvias (BMVs)

This combination enables manufacturers to achieve ultra-thin, uniform copper deposits while maintaining process stability and scalability for high-volume production.

Manufacturing impact

The Printoganth MV TP3 series simplifies process integration and reduces the need for multiple, disconnected chemistries by covering a wide range of copper thicknesses within a single product family. The series enables a more consistent and controllable metallization strategy, from ultra-thin seed layers to thicker functional deposits. When used with compatible activation systems, such as Neoganth® or Cupraganth® MV, the series supports uniform deposition across challenging material sets and advanced build-up films. This helps manufacturers meet technical and economic targets.

In short

As advanced packaging continues to evolve, flexibility in electroless copper deposition is becoming a key differentiator. The Printoganth MV TP3 series provides a scalable, high-performance solution, enabling manufacturers to adapt copper thickness to their specific requirements while maintaining reliability, adhesion, and coverage.

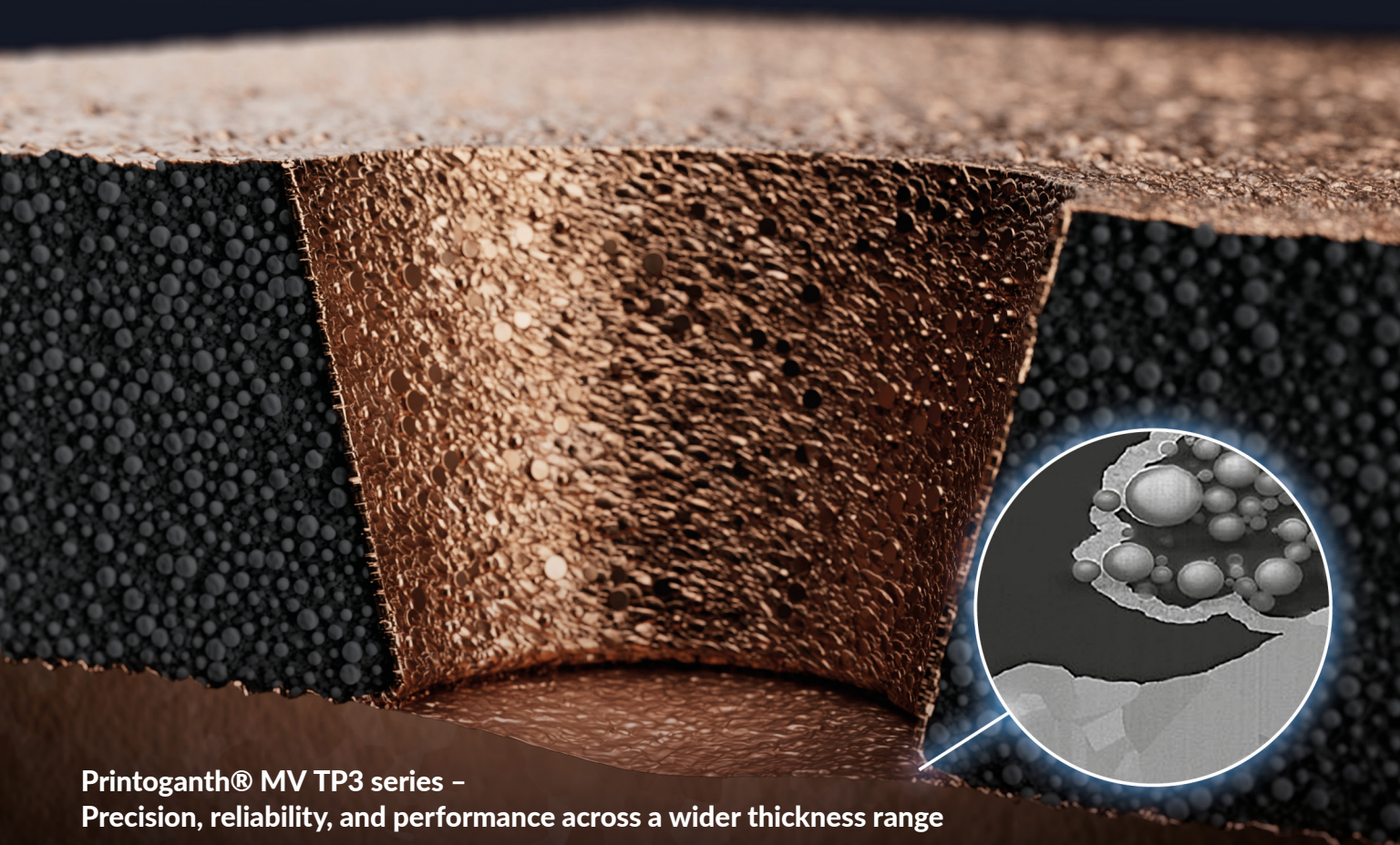
For greater flexibility in electroless copper deposition, the Printoganth MV TP3 series offers a practical path forward for next-generation advanced packaging manufacturing.



Roger Massey

Global Product Manager PTH/STT
at MKS' Atotech
roger.massey@mks.com
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Adaptable electroless copper for advanced packaging applications



Printoganth® MV TP3 series – Precision, reliability, and performance across a wider thickness range

Meet the Printoganth® MV TP3 series from MKS' Atotech, an adaptable electroless copper platform designed for advanced packaging applications. The series supports a wide range of copper thickness requirements, and includes Printoganth® MV TP3 for ultra-low thicknesses below 150 nm, Printoganth® MV TP3 Mod for 150–250 nm, and Printoganth® MV TP3 Mod2 for deposits above 250 nm. The series combines best-in-class bath initiation with zero dummy plating, excellent adhesion to low-roughness dielectrics, strong throwing power into BMV structures, and fine epitaxial crystal growth through bottom-up recrystallization. The result is a flexible, high-performance solution for next-generation advanced packaging manufacturing. If you're looking for greater flexibility in electroless copper deposition, look no further. Contact MKS' Atotech to learn how the Printoganth® MV TP3 series can support your advanced packaging process.

To find out more about Printoganth MV TP3 series, scan the QR Code to the right.



Pre-electroless Causes of Voids

BY MICHAEL CARANO, GLOBAL ELECTRONICS ASSOCIATION

To support advanced 2.5D and 3D heterogeneous integration, product and motherboard designs are now using higher layer counts. As layer counts increase, plated through-holes (PTHs) become deeper and higher in aspect ratio, making it more difficult to achieve a continuous, void-free copper deposit. Drilling these thicker panels and higher aspect ratio vias adds another layer of complexity. Since there are many potential causes of PTH voiding, I'll focus on pre-electroless copper causes, including drilling.

Where Are They Coming From?

You'll often hear seasoned engineers say that there are so many process steps and variables that influence the success or failure of achieving a continuous, void-free copper deposit in the hole. One of the obvious causes of voids, or at least poor copper coverage, is poor drilling. Figure 1 shows voids on the glass bundle fibers. A closer look at this section shows a very poorly drilled hole wall, with glass bundles protruding from the resin.

Many assume the plating process should compen-

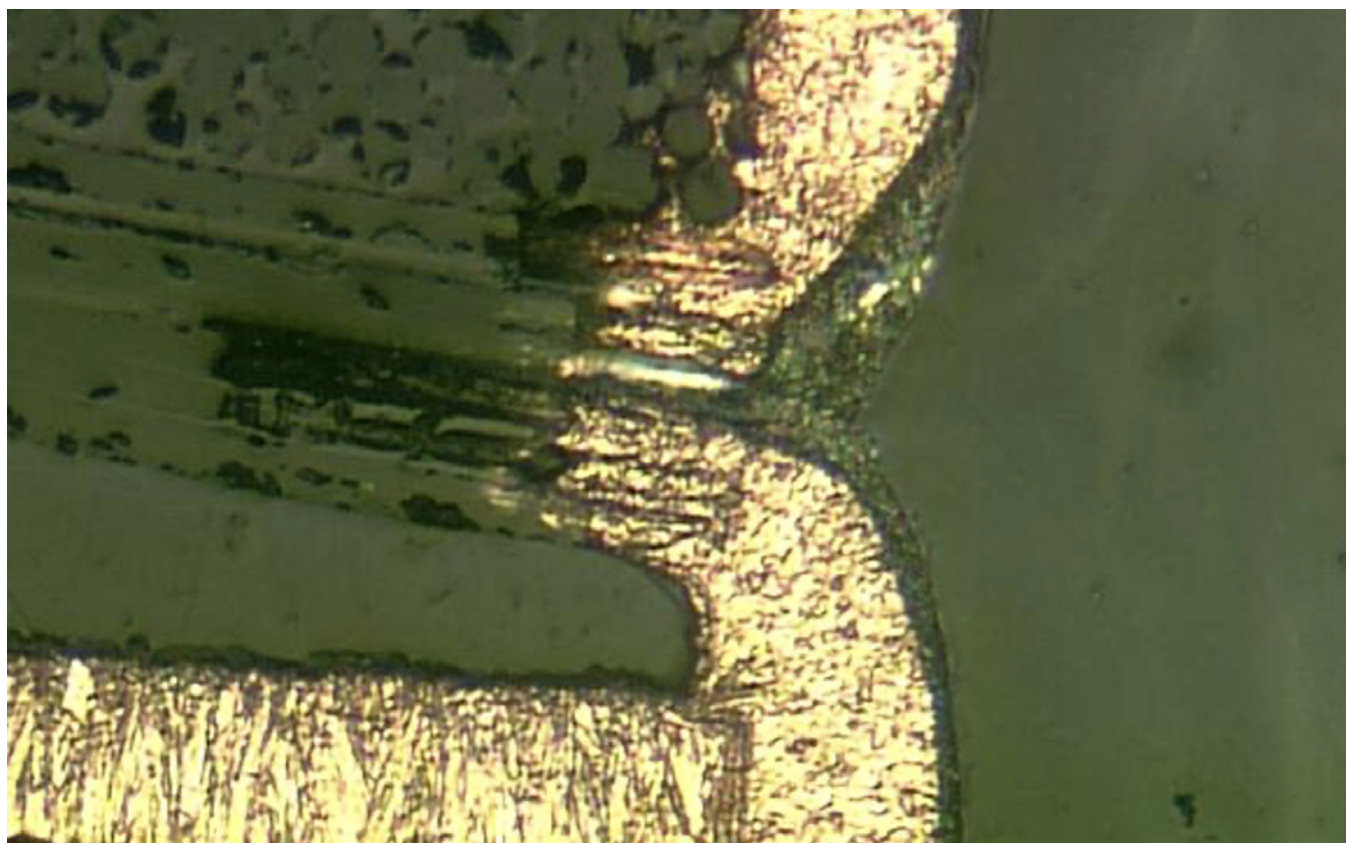


Figure 1: Glass fiber bundles are torn out, exposing a deep gouge in the resin.

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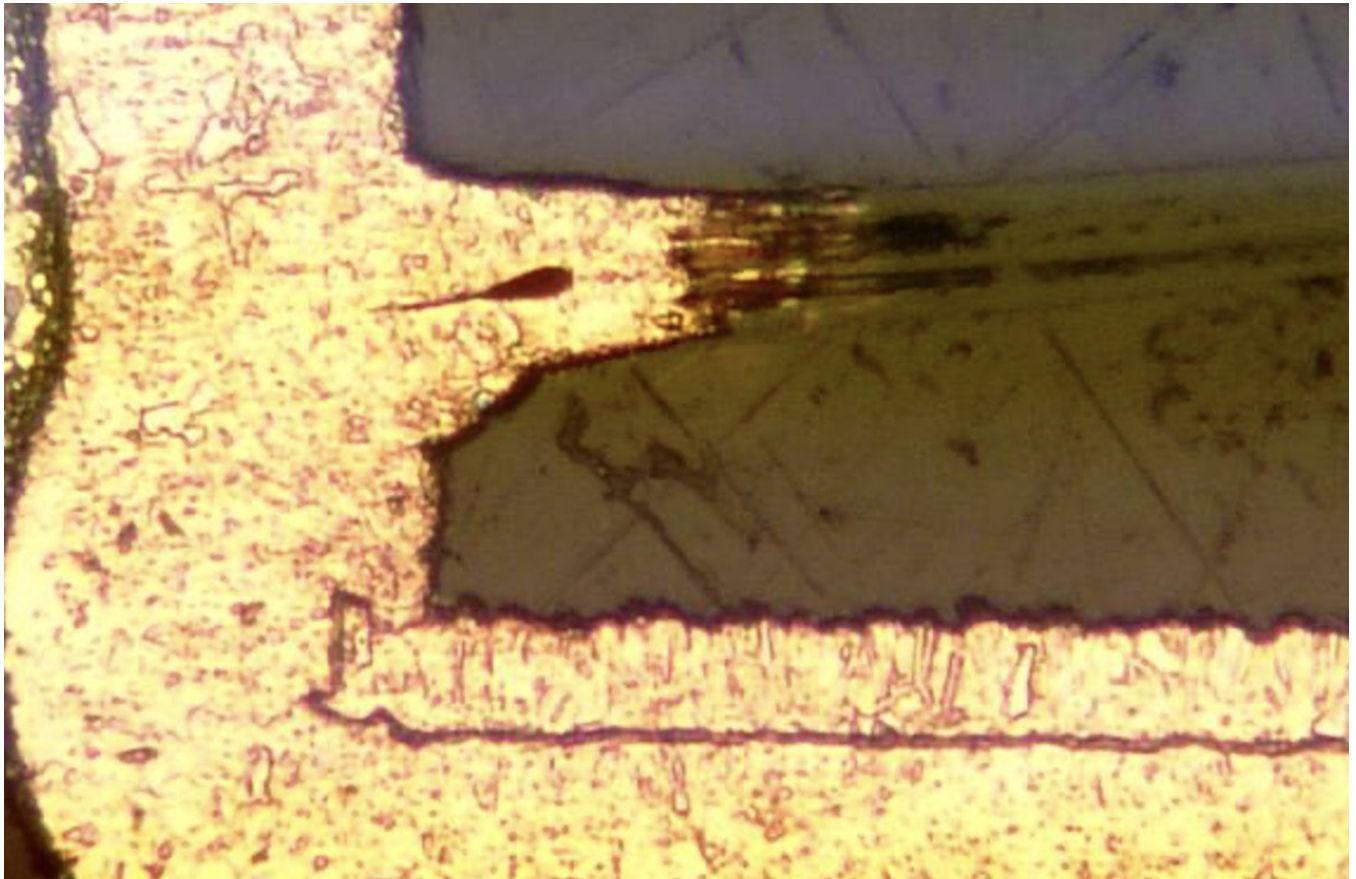


Figure 2: Deep resin gouge leading to plating folds. Note the thinned-out electrolytic copper plating. This situation is quite dangerous.

sate for damage like this, but surfaces of this kind are very difficult to activate with the palladium catalyst used in the electroless copper process. The drilling operation should be investigated immediately, with attention to the following:

- Drill bit condition: Review bit wear, number of hits, and the overall condition of the tool
- Spindle feeds and speeds: Confirm that the drill is cutting cleanly through the stack rather than punching through it
- Up-feed rate: Check whether a slow up-feed is contributing to torn glass bundles; it should typically be about twice the in-feed rate
- Chip load: Evaluate chip load settings and test adjustments to improve hole quality
- Stack height: Review the number of boards in the drill stack and consider reducing it to improve drilling quality

Another example of a rough hole wall is shown in Figure 2.

Figure 3 (p. 100) shows a section of a plated through-hole. Note the poor quality in the hole wall and its effect on the plating process again.

Even with all the issues shown in Figure 3, this board somehow passed in-circuit testing. Note the severe nailheading and some evidence of wicking along the torn-out glass fibers.

The desmear operation is another potential cause of PTH voids. The most effective desmear process available today is based on alkaline permanganate. In fact, the permanganate system is considered an industry standard. The use of alkaline permanganate for multilayer PCBs has had a dramatic effect on copper coverage and adhesion in the PTH. However, if not controlled, this process can be a major cause of voids. First, the process consists of four main chemical process steps:



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1. A solvent conditioner designed to penetrate the polymer matrix of the resin system and weaken the polymer-polymer bonds of the cross-linked chain.
2. The alkaline permanganate solution consists of sodium or potassium permanganate and its corresponding hydroxide salt.
3. A neutralizer (possibly in combination with glass etch) for removing manganese residues.
4. Glass etch as a separate step to lightly roughen (frost) or more aggressively remove glass fibers that may be protruding into the hole due to etchback.

If not controlled, any of these steps can lead to voids. If this is the case, even the most robust of electroless copper processes will not be able to compensate.

In Figure 4, the microroughened epoxy resin has been properly prepped by the alkaline permanganate process.

However, today's resin systems are far more complex than standard 140°C Tg epoxy, which remains one of the easiest materials to desmear. Modern resin systems require much tighter process control. These high-performance materials are highly cross-linked polymers that display very high Tgs and are more resistant to chemical treatments, including desmear. An effective alkaline permanganate process not only removes drill smear, but also microroughens the resin. This surface texture, often called a honeycombed appearance (Figure 4), is desirable for two reasons: The textured surface improves palladium catalyst adsorption, which supports electroless copper deposition and coverage. It also improves copper adhesion.

This improves solderability by reducing or eliminating blowholes during wave soldering. Inadequate texturing can increase the risk of voiding because reduced surface texture lowers catalyst adsorption. Electroless copper deposition requires sufficient catalyst on the hole wall to initiate and maintain uniform copper coverage. During troubleshooting, consider the following:



Figure 3: Poorly drilled plated through-hole with torn out glass and resin gouges.

- Is the solvent conditioner, or swellant, penetrating the resin matrix effectively, and is the solvent system compatible with the resin? Some higher Tg materials do not respond as standard FR-4 does. Because these resins are more highly cross-linked, the solvent may have difficulty penetrating and weakening the polymer bonds, reducing the permanganate solution's ability to remove resin and create the desired texture.
- Verify the operating temperature of the alkaline permanganate solution, along with the hydroxide and permanganate concentrations.



Figure 4: Desmear performance with microroughened texture to the resin.

Hydroxide increases the aggressiveness of permanganate's attack on the resin, while permanganate in the +7 oxidation state oxidizes and breaks down the resin. Manganate (+4), a reaction by-product, does not contribute to resin oxidation and should be controlled below 20–25 grams per liter. If manganate builds up, resin removal and texturing will slow. If solvent compatibility and penetration are adequate, consider increasing the permanganate concentration. Sodium permanganate can provide more available permanganate in solution than the corresponding potassium salt.

- Review the neutralizer and glass etch. A major source of voiding is manganate residue left on the resin and glass within the hole wall. Renew the solution regularly to maintain active chemistry, and verify the acid concentration because low acid reduces neutralization effectiveness. To reduce process steps, some fabricators combine the neutralizer and glass

etch in one tank; however, separate steps are generally more effective. As the glass etch weakens with use, its ability to frost or roughen glass fibers decreases, reducing catalyst adhesion to glass and increasing the likelihood of voids.

This about covers the pre-electroless copper causes of voiding. In another column, I will explore other causes of voiding. **I-CONNECT007**



Michael Carano brings over 40 years of electronics industry experience with special expertise in manufacturing, performance chemicals, metals, semiconductors, medical devices, and advanced packaging. To read past columns, [click here](#).

Micro-robot Exoskeletons With Rigid-flex PCBs

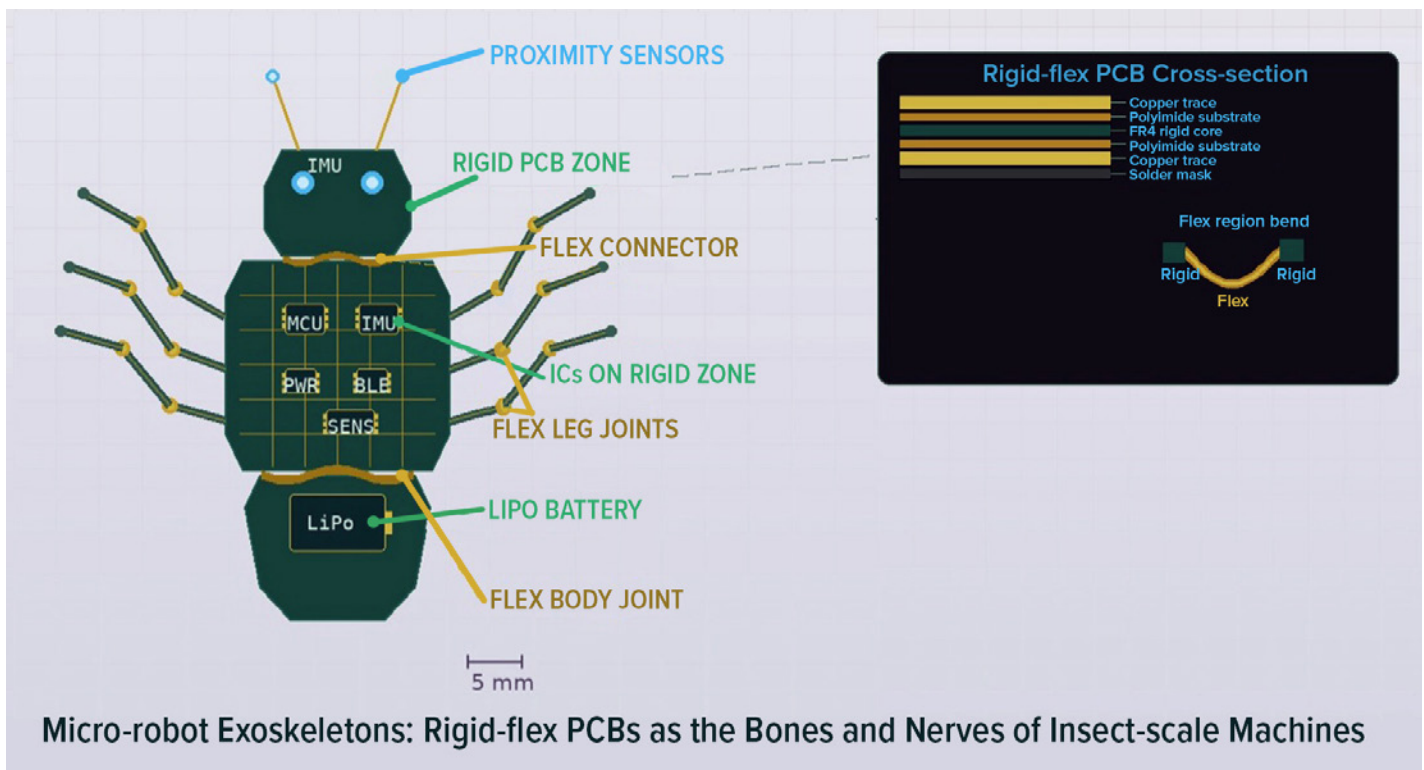
Building a robot the size of a cockroach requires rethinking every assumption of conventional mechanical and electrical engineering. At the centimeter scale, wire harnesses become unmanageable tangles, rigid chassis structures become disproportionately heavy, and conventional connectors dwarf the components they're meant to join. Rigid-flex PCBs offer a radical solution: Make the circuit board the skeleton.

Structural Electronics

This concept, sometimes called structural electronics, exploits a key property of rigid-flex PCBs: the ability to combine stiff regions that hold components

with compliant flex regions that serve as joints. In practice, rigid-flex PCBs are replacing the bones and nerves of insect-scale machines. In a conventional robot, motors, sensors, and processors are mounted on separate rigid boards and connected by wires. In a structural electronics design, all of these elements share a single multilayer rigid-flex PCB that, when folded along its flex regions, becomes a three-dimensional electromechanical assembly.

The Harvard Microrobotics Laboratory has been a pioneer in this space. Its RoboBee platform, a sub-gram flying robot inspired by insect flight, uses a laminate manufacturing process called smart composite microstructures. Though not a PCB in



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the traditional sense, it shares the same underlying principle: a flat-fabricated sheet that folds into a functional 3D structure. Later iterations have moved toward true rigid-flex PCB approaches as commercial fabrication capabilities have improved.

The weight savings are dramatic. A wire harness connecting a dozen sensors to a central processor in a robot this small might weigh more than the motors themselves. By routing all interconnects through the PCB substrate, which must exist in the design anyway, that parasitic mass disappears entirely. The board does double duty as conductor and structure.

Rigid-flex Exoskeletons

Turning the PCB into an exoskeleton also solves a connector reliability problem that plagues small robots. At insect scale, vibration, impact, and the repeated flexion of locomotion quickly fatigue soldered wire connections. When the traces are embedded in a continuous substrate, there are no separate connections to fail; the signal path and the structural member are one.

Current research applications include search-and-rescue micro-robots designed to navigate rubble fields, environmental monitoring robots that can be deployed by the thousands to map contaminated sites, and medical micro-robots intended for minimally invasive diagnostics. Each demands the smallest possible size-to-capability ratio, and each benefits from the structural electronics approach.

Fabrication challenges are significant. The tight bend radii required by folded rigid-flex designs

push the limits of standard PCB materials. Impedance continuity through flex folds requires careful trace geometry and via placement, and the thermal management constraints of sealing active components into a structural element with no airflow require creative heat-spreading solutions.

Summary

As fabrication tolerances shrink and flex materials improve, the insect-scale structural electronics robot will become an increasingly standard platform. The rigid-flex PCB that is simultaneously a skeleton, nervous system, and muscle interface may prove to be one of the most consequential engineering innovations in small-scale robotics. **I-CONNECT007**

Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit*

Designer's Guide to... Fundamentals of RF/Microwave

PCBs and Flex and Rigid-Flex Fundamentals. He

is the author of *Thermal Management: A Fabricator's Perspective*, *The Printed Circuit Designer's*

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Vertical Conductive Structures (VeCS)

BY HAPPY HOLDEN, I-CONNECT007

Editor's note: This column previously appeared in the October 2021 issue of PCB007 Magazine. It was the first of Happy Holden's series of technical columns based on the work of Karl Dietz.

The industry has not introduced many new structures in the last 60 years. Multilayers have continued to evolve with thinner materials and smaller traces and spaces as well as drilled vias. It's been nearly 40 years since Hewlett-Packard put its first laser-drilled microvia boards into production for its innovative Finstrate process¹.

Now we have a new structure, vertical conductive structures (VeCS), developed by Joan Tourné of NextGin Technology BV of the Netherlands.

This technology is a breakthrough because now any advanced board shop can produce HDI level high density interconnects without any new capital equipment—and at a lower cost with higher electrical performance. I first became aware of the technology from an interview in the February 2017 issue of *The PCB Magazine*². As seen in Figure 1, the key technology is the replacement of small or blind vias with a routed trench (slot), that is much easier to metallize and plate.

VeCS is a true 3D concept for interconnection by creating a routing channel (slot) in the printed circuit that can then be metallized and plated easier than high-aspect ratio vias while allowing a connection to the inner layers. The channels are easier to plate and can be created by existing PCB

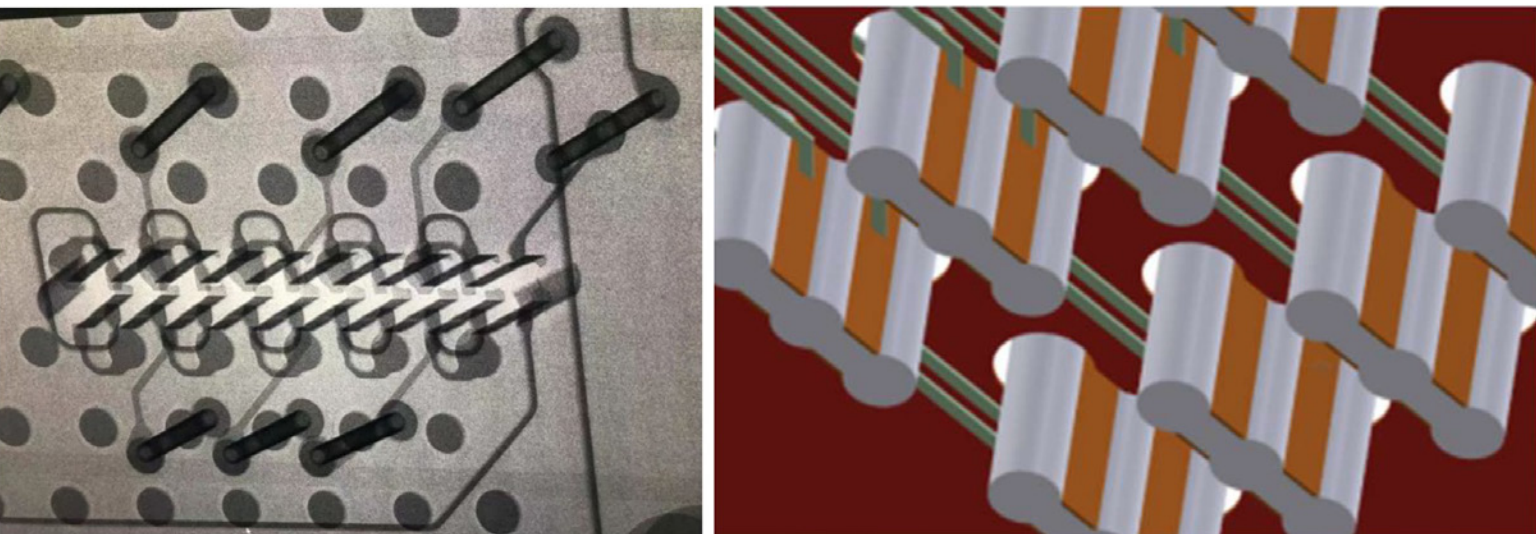
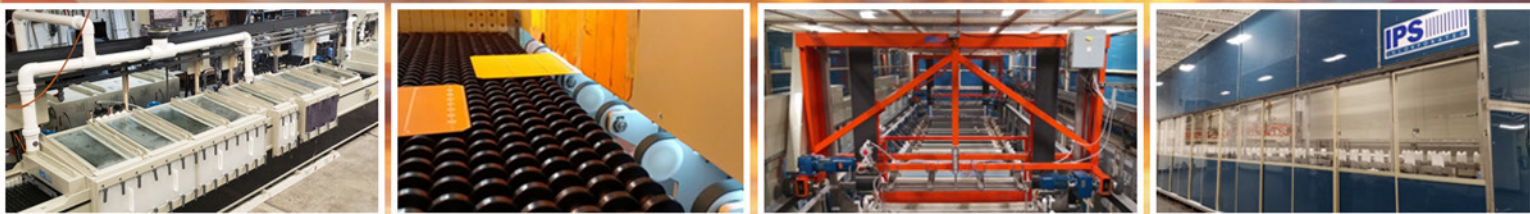


Figure 1: VeCS slot under magnification (left), bottom view of VeCS slot (right). (Source: NextGin)

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fabrication equipment. This allows HDI densities to be achieved without significant added costs along with easier fabrication processes and higher electrical performance and reliability. The process and applications already developed by NextGin Technology are: VeCS -1, -2, and -HDI^{2,3}. The three main combinations of their interconnect slot technology are defined as:

- **VeCS-1:** Where the channel (slot) goes through the substrate
- **VeCS-2:** Here, the slot is formed as blind or in a hybrid-blind and through-slot combination
- **VeCS-HDI:** Laser-drilled microvias are used for fine-pitch utility on ultra-fine-pitch components

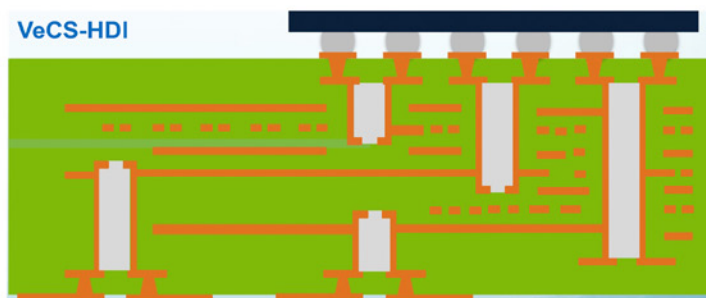
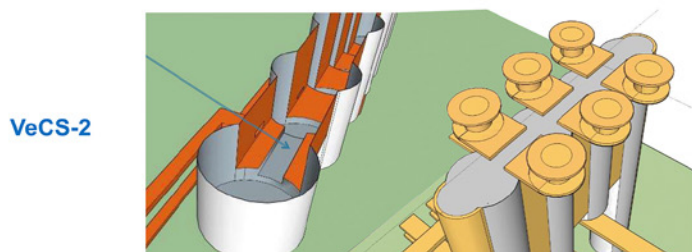
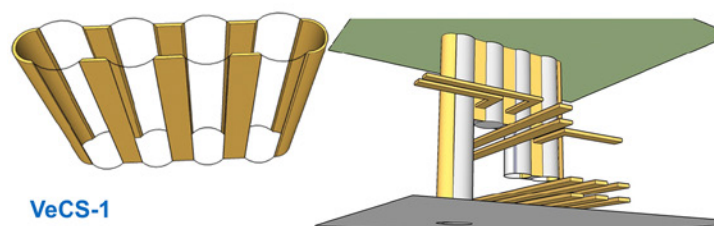


Figure 2 highlights these three structures.

With channels (slots) formed from both sides, the 3D vertical traces provide greatly increased density without sequential laminations. Replacing larger through-hole vias with slots provides better power integrity for new power-hungry chips while lowering inductance and capacitance for improved signal integrity.

The Channel or Slot

The all-important step of metallizing and plating the typical 0.3 mm blind slot is shown in Figure 3. for various depths and lengths (from depths of 0.47 mm to 1.23 mm and lengths of 0.6 mm to 1.8 mm). Some of the smaller aspect ratios have insufficient chemical exchange but the majority have excellent chemical

Trace Routes

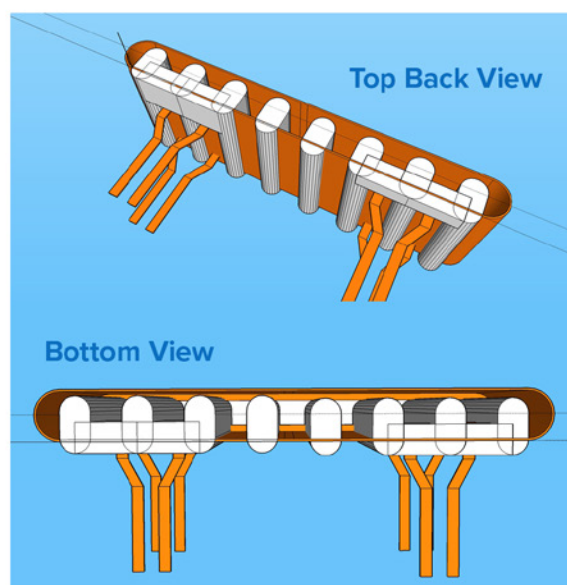
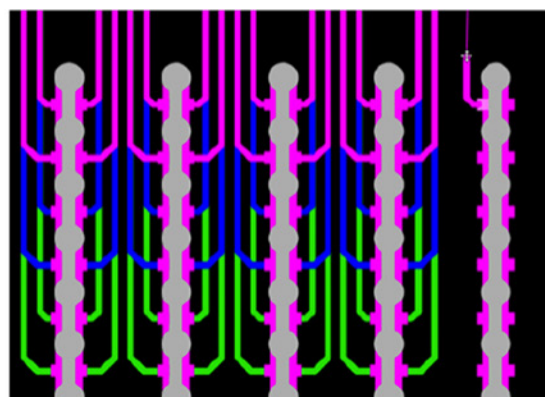


Figure 2: (Left) Three different structures, based on the original concept of a slot or trench, make up VeCS; (right) trace routes showing various layers, and 3D views of the construction. (Source: NextGin)

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TerraGreen 400G	3.15 / 0.0017	3.10 / 0.0017	3.07 / 0.0017

Values shown are typical across 10-30 GHz and demonstrate comparable electrical performance.

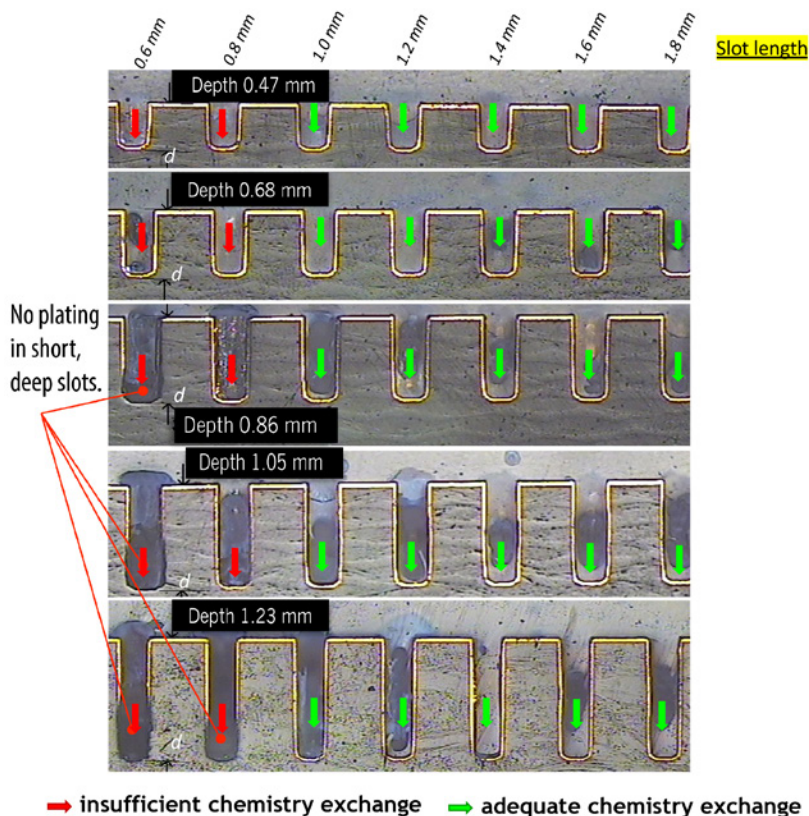


Figure 3: Creating and plating the blind channel (slot) is the key feature of VeCS-2 but is within the capability of any high-performance PCB fabricator.³

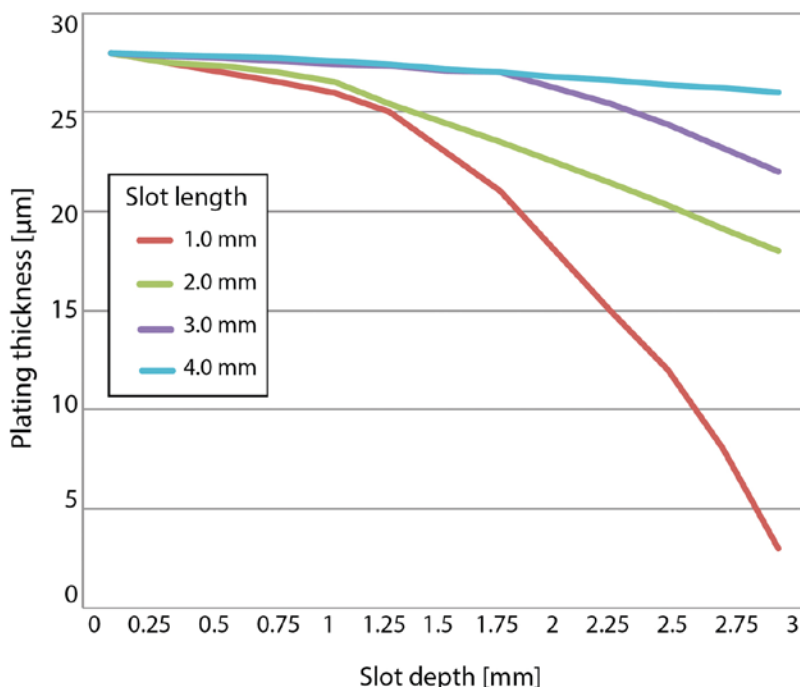


Figure 4: Plating thickness as a function of slot depth and length.³

exchange for normal plating baths. The new alternative drill/router bits have successfully created channels of 0.1 mm with straight walls and no burring. Figure 3 shows various blind channel depths plated with conventional plating equipment.

Figure 4 shows plating results with respect to the slot length and slot depth. Note that for these tests, NextGin used plating processes at standard parameters and chemistry types. The method of plating was electroless copper followed by a panel plate to the required copper thickness in the slot targeting a thickness of 25 μm .

Fabrication Process

Figure 5 presents the views of the VeCS fab process, starting with a conventional through-hole multilayer. The process has eight steps:

1. Create slot
2. Plate slot
3. Alignment in BGA pin field
4. Resin fill PR slot and PR stencil
5. Drill CR slots
6. If vertical traces are going to be used, drill BR slots
7. BR/CR stencil
8. Resin fill BR/CR slot

In Step 1, after drilled vias are completed, the primary cross-route (CR) slots are put in. Here, a special drill/router bit uniquely suited for this operation is used. Much work and experimentation were conducted to perfect an ideal drill/router bit for this task. Then in Step 2, metalliza-

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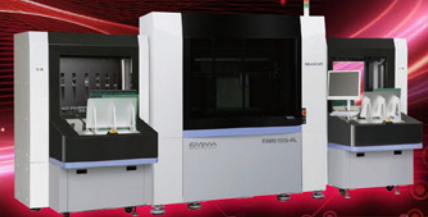
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VeCS Fabrication Process

0.5mm Primary Rout Steps VeCS-2

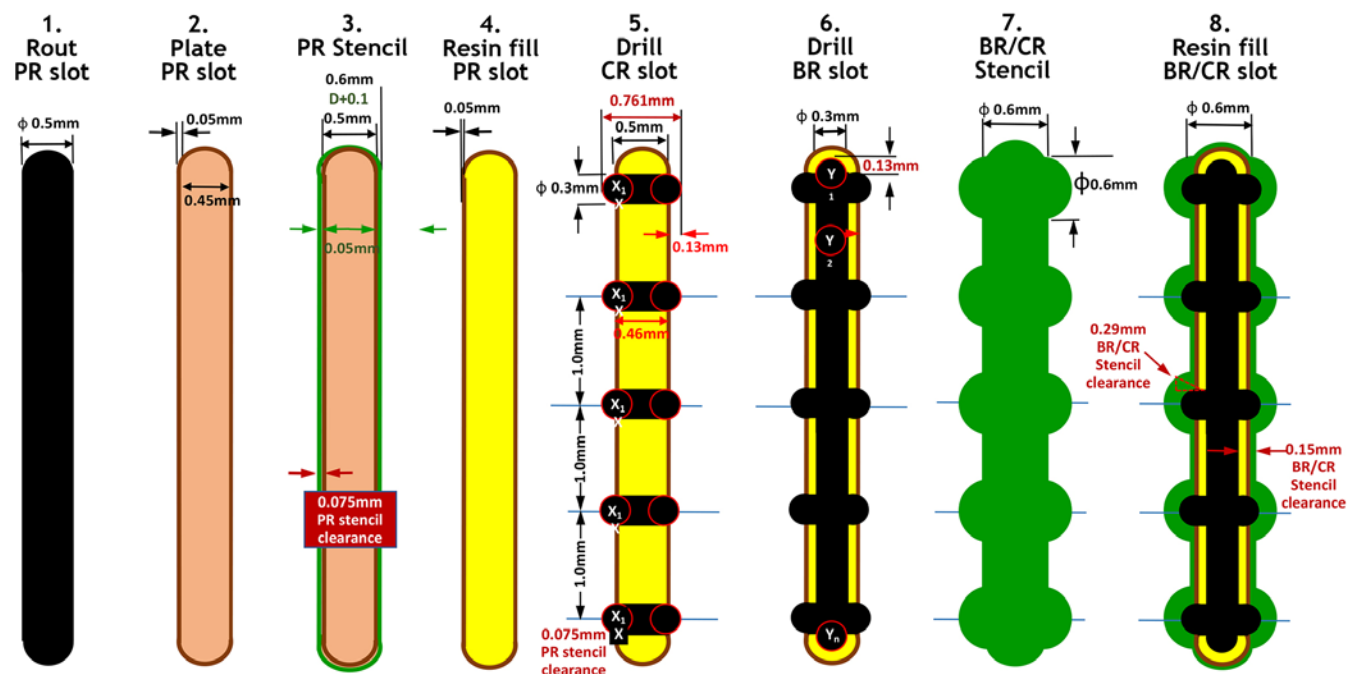


Figure 5: The VeCS fabrication eight-step process.⁸ (Source: NextGin)

tion and copper plating are performed. In Steps 3 and 4 the resin is now used to fill the CR slots. After curing, next is the important Step 5 where cross-routes create the vertical interconnects. If vertical traces are going to be used, Step 6, drill/rout out the back-route (BR) slots. Then selected vias and slots are resin-filled and cured. In Steps 7 and 8, for pattern plating, the normal process resumes of imaging, plating, stripping and final etching. In the final panel, the board would be solder masked, with any final finishes and fabrication.

Design Rules

To illustrate various routing densities, we like to illustrate 0.7 mm pitch because VeCS has a 600% increase over through-hole while HDI has only a 200% improvement.

The cross-route or CR step is also completed. Clearly you can see the glass dielectric removed between the VeCS circuits. This eliminates glass influence for issues like CAF⁴.

VeCS-2 design details: The middle part (conduc-

tive material) is removed to create two different potentials to the left and right of the slot. Not every position in the slot needs to be processed in this way as it depends on the design.

This design method for VeCS is another example of creative concepts. The VeCS-1 with back route or VeCS-2 differential signals are routed and surrounded by a “racetrack” type ground reference. This nearly creates a complete Faraday Cage for the connections. The SI performance is beneficial for speeds above 10Ghz.

Details of the 0.5 mm pitch VeCS breakout using standard VeCS design rules are in referenced in Table 1. Routing will depend on cross-route slot dimensions. But remember: HDI can only go one or two layers down, while VeCS can go three times deeper.

A complete set of design guidelines for VeCS-1 and VeCS-2 (Table 1, p. 114) are broken down into standard, advanced, and in R&D. Additional design illustrations and advice, including tool setups are in the August 2019 issue of *PCB007 Magazine*⁵.

Videos that show the routing of VeCS struc-



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Table 1: VeCS Design Rules.

VeCS-1	Standard	Advanced	R&D
A = Primary slot width	0.50 mm	0.40 mm	0.30 mm
B = Primary slot length, minimum	1.6 mm	1.6 mm	1.6 mm
D = Cross slot width	0.30 mm	0.30 mm	0.25 mm
E = Cross slot length, minimum	A + 0.20 mm	A + 0.15 mm	A + 0.15 mm
I = Vertical (VeCS) trace thickness, minimum	0.020 ~ 0.025 mm	0.020 ~ 0.025 mm	0.020 ~ 0.025 mm
W = Vertical (VeCS) trace width, minimum	0.30 - 0.40 mm	0.25 - 0.30 mm	0.25 mm
VeCS-2	Standard	Advanced	R&D
A = Primary slot width	0.50 mm	0.40 mm	0.40 mm
B = Primary slot length, minimum	1.6 mm	1.6 mm	1.6 mm
C = Primary slot nominal depth (C) below critical signal layer	0.125 mm	0.10 mm	0.10 mm
D = Cross slot width	0.30 mm	0.25 mm	0.25 mm
E = Cross slot length, minimum	A + 0.30 mm	A + 0.20 mm	A + 0.20 mm
F = Cross slot nominal depth below primary slot depth	0.125 mm	0.10 mm	0.10 mm
G = Bottom slot width	0.30 mm	0.25 mm	0.25 mm
F = Bottom slot nominal depth below primary slot depth	0.125 mm	0.10 mm	0.10 mm
I = Vertical (VeCS) trace thickness, minimum	0.020 ~ 0.025 mm	0.020 ~ 0.025 mm	0.020 ~ 0.025 mm
J = Nominal isolation (keep-out) depth below bottom slot	0.25 mm	0.20 mm	0.20 mm
W = Vertical (VeCS) trace width, minimum	0.30 - 0.40 mm	0.25 - 0.30 mm	0.20 mm

Design examples for Siemens Digital Industries Software, Cadence, Zuken and Altium

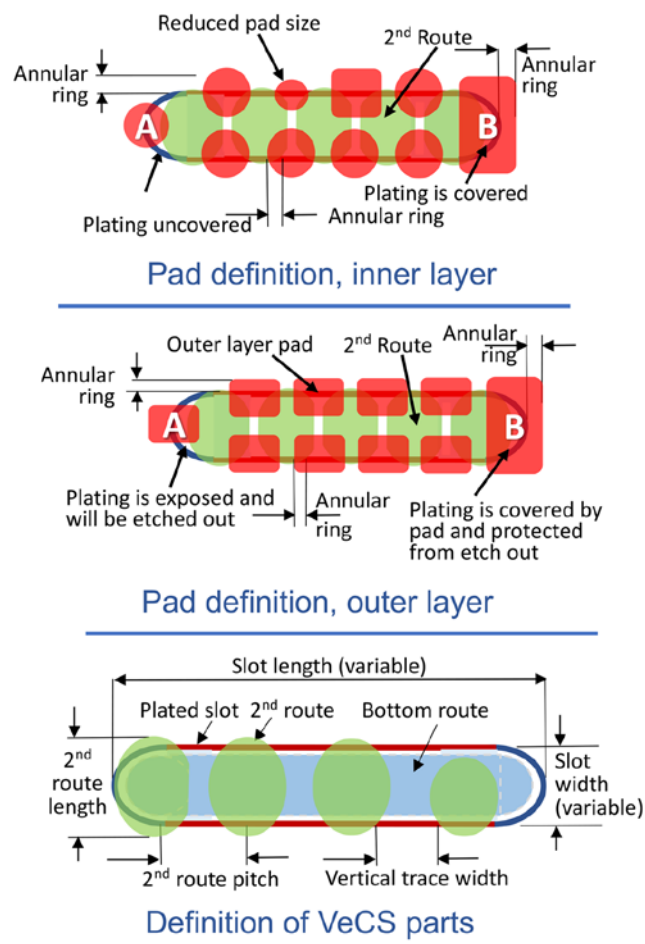


Figure 6: Recommendations for VeCS design rules from Table 1. (Source: NextGin)

tures on various EDA tools like Siemens/Mentor, Cadence, Zuken, and Altium are available by contacting NextGin Technology.

Electrical Performance

Electrical performance is another area (besides CapEx and costs) where VeCS outperforms plated through-hole and HDI. The vertical trace does not have the capacitance and inductance of a via. For extremely high-speed logic, the ability to create shielded differential pairs with minimum distortion is unique. As seen in Figure 7 (p. 116), experimentation was conducted to tune vertical traces in the slot such that there is almost no reflection/dispersion. BestPCB compared simulated vs. actual product measurements. Additional figures show the simulated tuning of a TDR response on VeCS-2 where we can vary it from a capacitance to an inductance response or make it as “flat” as possible on the NextGin website.

Modeling with Simbeor has determined the best performing layer transition. Can we use VeCS to make layer transitions and re-introduce Manhattan routing? First results look interesting. Manhattan/VeCS routing is an alternative for expensive point-to-point routing for dense boards. VeCS electrical performance is discussed in an October

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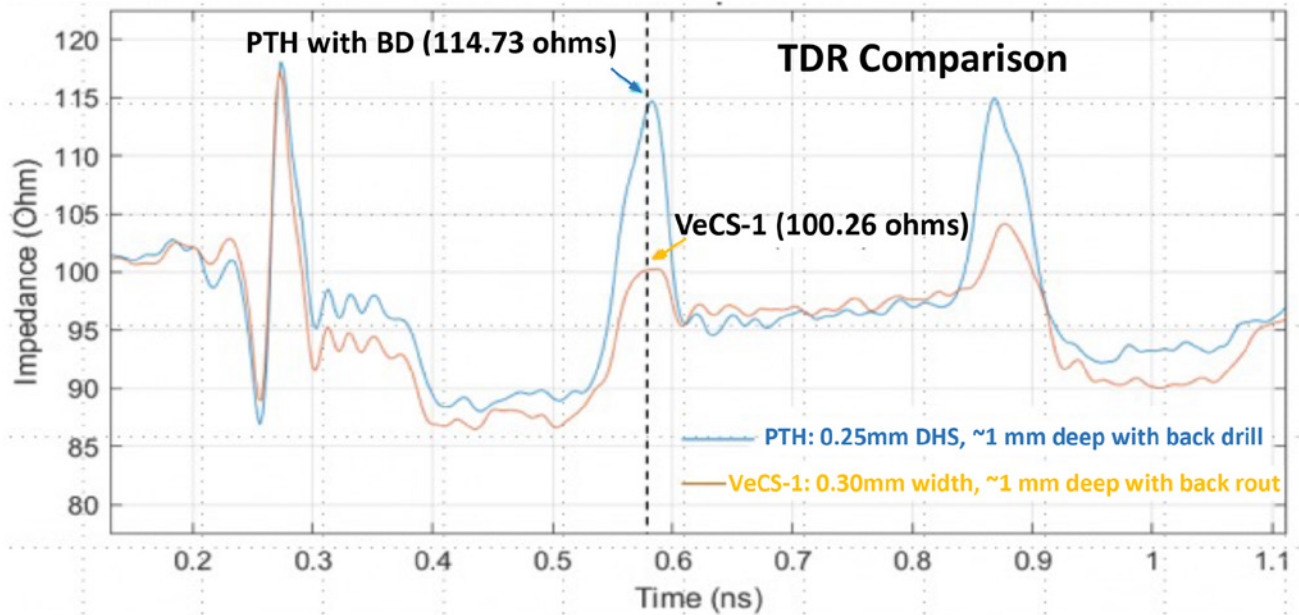


Figure 7a: A TDR comparison of a high-speed signal propagation (impedance) through vertical connections of a back-drilled PTH vs. a back-drilled VeCS-1 vertical trace seen in Figure 7b. (Source: BestPCB)

Figure 7b: Four figures of a high-speed signal propagation (impedance) through the back-drilled VeCS-1 connections;

7b1: Top view of test board schematic;

7b2: TDR measurements along test traces;

7b3: Top photo of test board;

7b4: X-ray image of the shielded VeCS-1 vertical connection to inner layers.

1 & 9: Molex 72351-1851 and launch via;

2 & 8: A short single-end routing on L1;

3 & 7: Differential routing on L1;

4 & 6: Test via (VeCS-1 or PTH);

5: Differential routing on inner layer.

(Source: BestPCB and WUS Printed Circuit Co.)

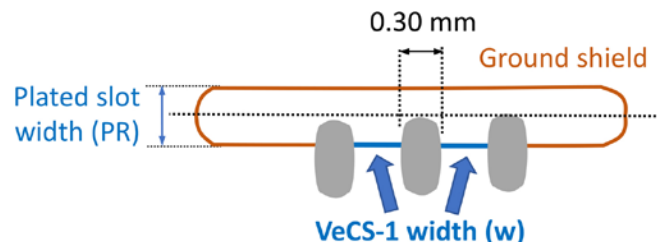
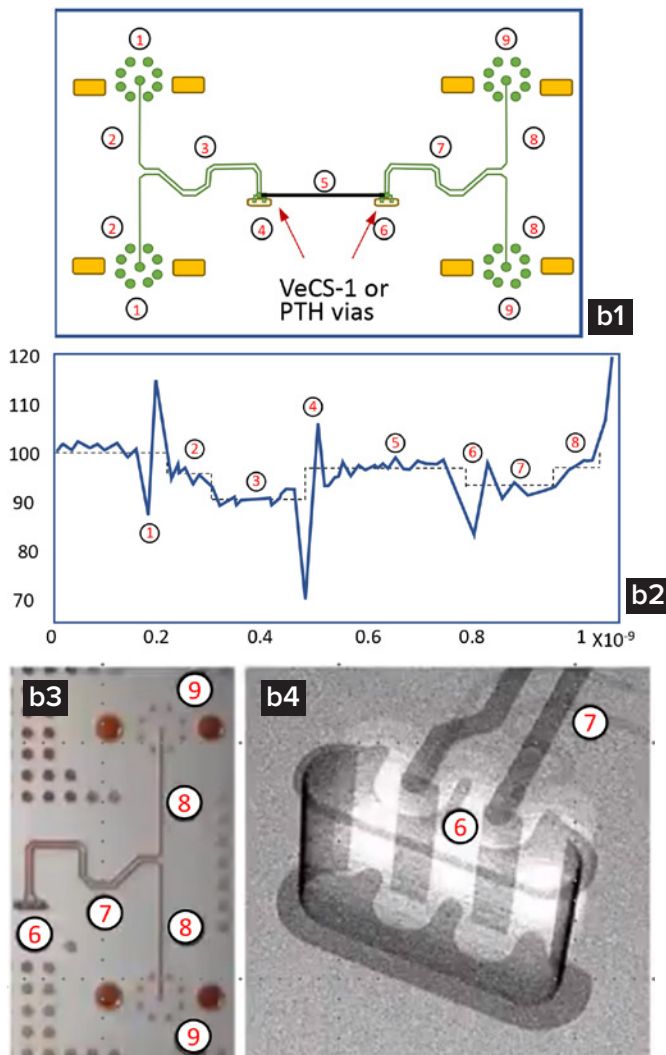


Figure 7c: A top view of the VeCS-1 vertical connections with plated ground shield as seen in Figure 7b4. (Source: NextGin and WUS)

2019 *PCB007 Magazine* article⁶. (It contains an eye diagram showing simulated layer transition in VeCS at 30 GB/s.)

Reducing reflections in transmission lines is one of the areas of focus with VeCS. Tuning the impedance of the vertical trace using, for example, a shielded VeCS slot enables the designer to match the vertical and horizontal impedances of the trans-

mission line.

Reliability

A VeCS laminate reliability review reported that on testing 370HR, it passed six cycles of 260°C reflow including CAF tests. IST VeCS coupons passed 250 cycles and 19 reflow cycles to 217°C. TCT performance on IST passed 100 cycles and TCT performance on CAF coupons passed 100

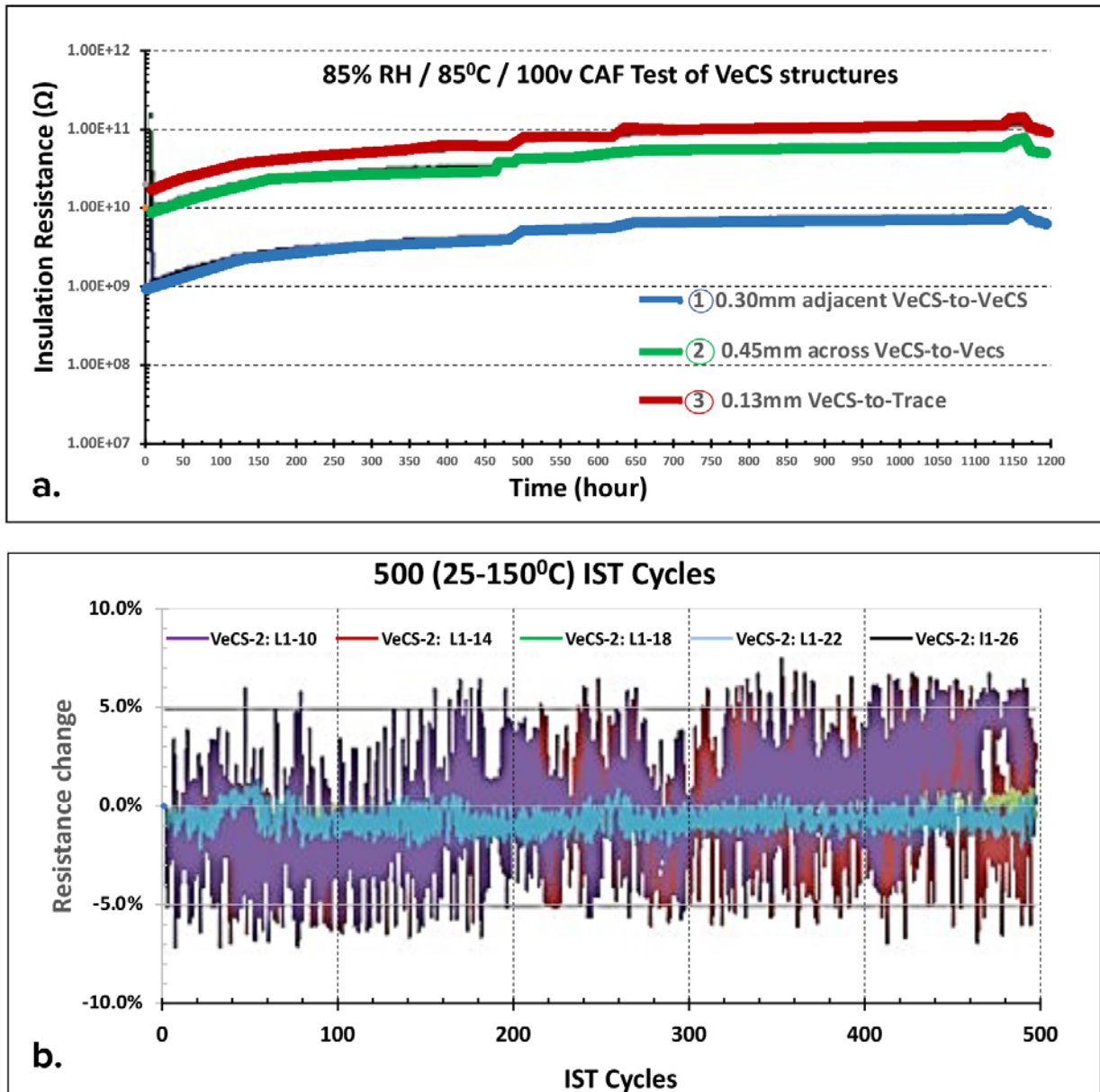


Figure 8: a) CAF test of three VeCS structures for 1090 hours at 85% RH, 850C at 100 volts; b) resistance change of five VeCS-2 slot structures for 500 cycles of 25 to 150°C. (Source: WUS Printed Circuit Co.)

Micro-VeCS Process

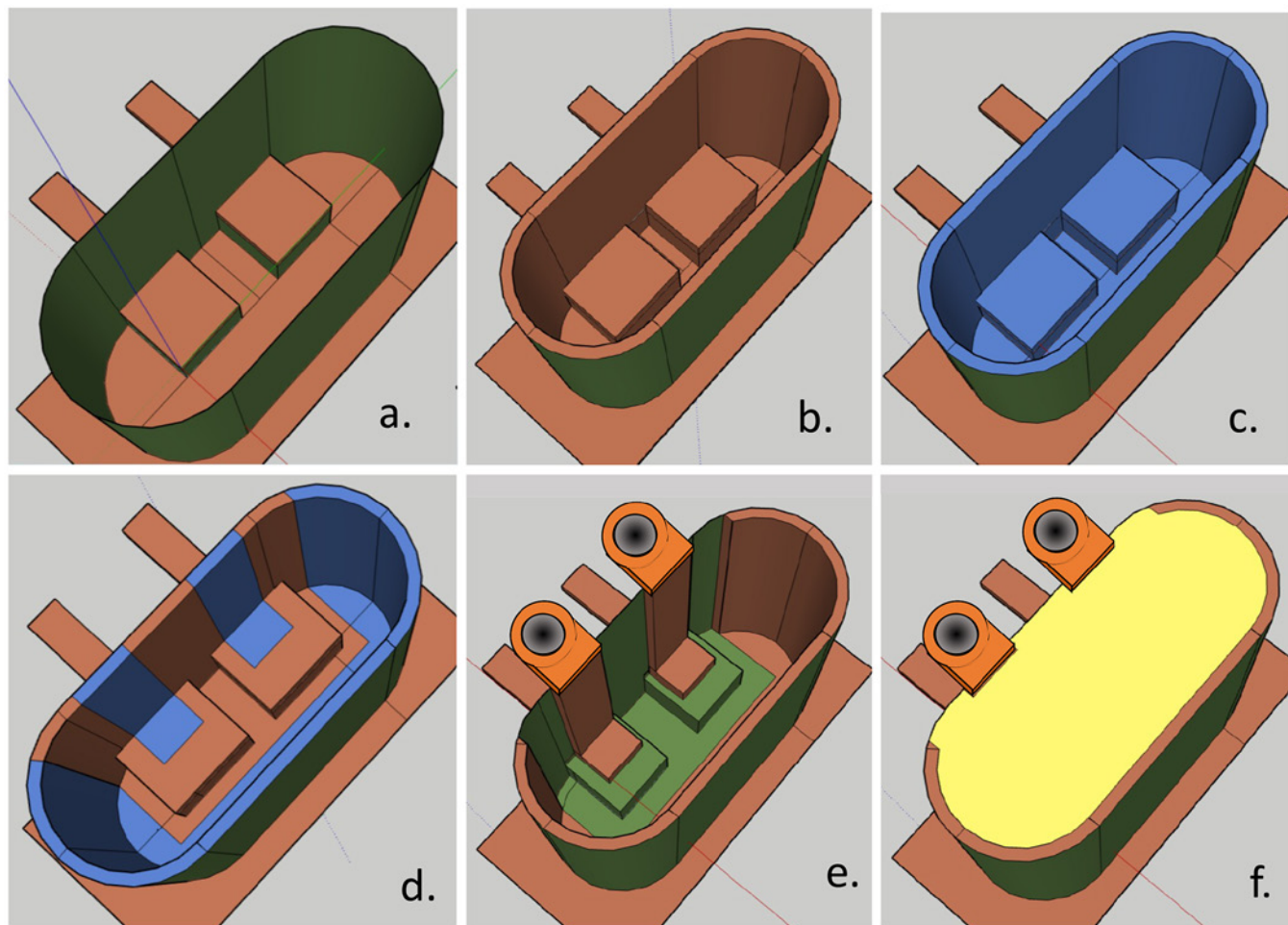


Figure 9: The micro-VeCS process as follows: a) laser cutting the cavity; b) plating the cavity; c) apply positive electrodeposited resist; d) direct expose the resist; e) etch and strip; f) fill VeCS slot.

cycles (Figure 8a).

Extensive IST testing has revealed that VeCS coupons achieved 10 to 30 cycles while conventional PTH had a range of seven to 10 cycles (Figure 8b). Additional data is available from NextGln.

Future Enhancements

The current focus is on the use of HDI microvias to enable VeCS applications for fine pitches down to 0.15 mm. The micro-VeCS process is shown in Figure 9 for inner layers.

VeCS/HDI will scale down the feature sizes for VeCS to enable it to run smaller devices pitches—device pitches down to 0.15mm are possible, as seen in Figure 10.

The benefits of VeCS/HDI are:

- No materials limitations. Use flat weave materials to support the laser processing
- Compete with HDI constructions and take advantage of reduced lamination cycles reducing lead time and complexity
- Single lamination process versus 5 or more laminations
- Reduce cost by 40–60%
- Higher yields

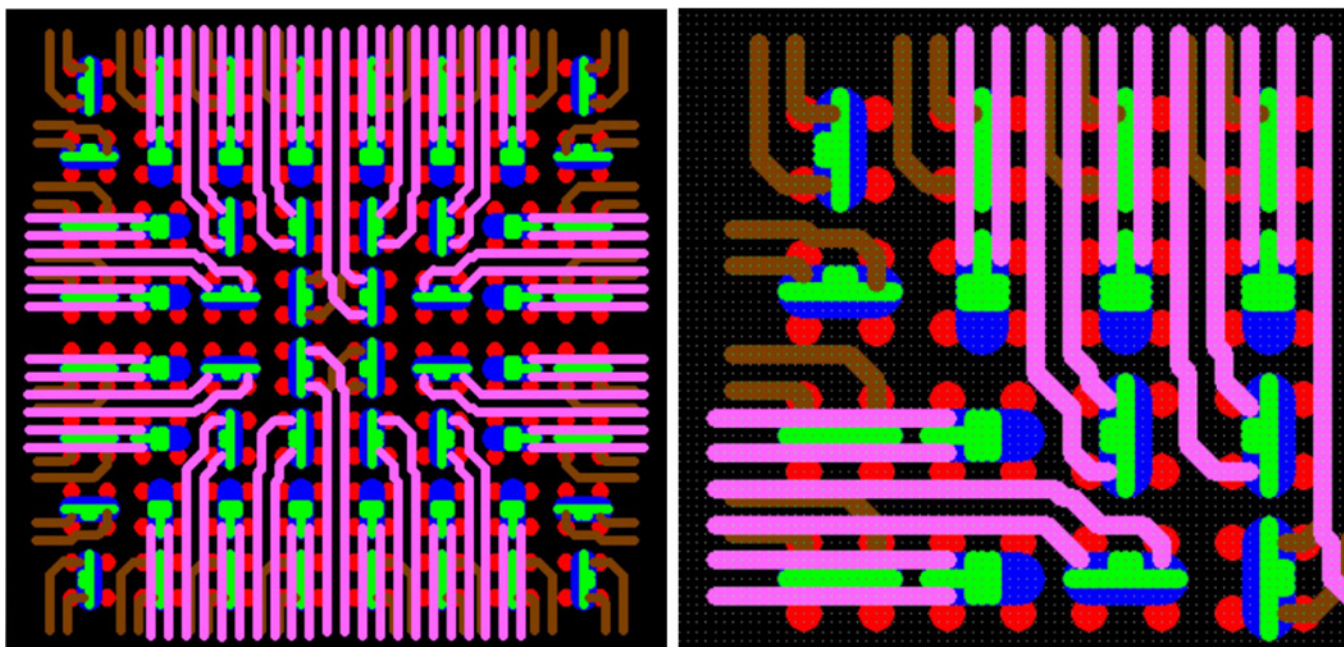


Figure 10: Routing of a very-fine pitch BGA using HDI, and VeCS-2 buried slots with close-up of quarter-pattern.
(Source: NextGin Technology)

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Happy Holden has worked in printed circuit technology since 1970 with Hewlett-Packard, NanYa Westwood, Merix, Foxconn, and Gentex. He is currently a contributing technical editor with

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Automation and Advanced Procedures in PCB Fabrication, and *24 Essential Skills for Engineers*.

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Looking Beyond Chemistry

GreenSource's vertical plating platform is a modular electroplating system designed for demanding applications requiring thick copper deposits and high aspect ratio blind microvias. Rather than relying solely on conventional process optimization techniques, the system incorporates several design features intended to improve electrolyte movement and mass transport throughout the plating cell.

Each module consists of four independently controlled plating cells with dedicated electrolyte circulation. A dense array of closely spaced fluid delivery nozzles directs electrolyte across both sides of the panel, while programmable horizontal and vertical mechanical agitation continually refreshes the boundary layer at the copper surface. Together, these features are designed to create a more consistent electrochemical environment across the entire work area.

Our goal was not simply to increase plating speed, but to improve plating uniformity while supporting the heavy copper requirements being demanded by advanced power electronics manufacturers.

Establishing the Baseline

One aspect of the study makes it particularly interesting. Rather than first optimizing the hardware through shielding, bussing modifications, or rectifier adjustments as would normally be done during equipment qualification, the engineering team intentionally evaluated the system in a largely unoptimized configuration.

The production rack used during testing provided electrical contact only from the top of the panel. Four-sided contact, commonly employed to improve current distribution, had not yet been implemented. Likewise, shielding and other electroplating refinements remained untouched.

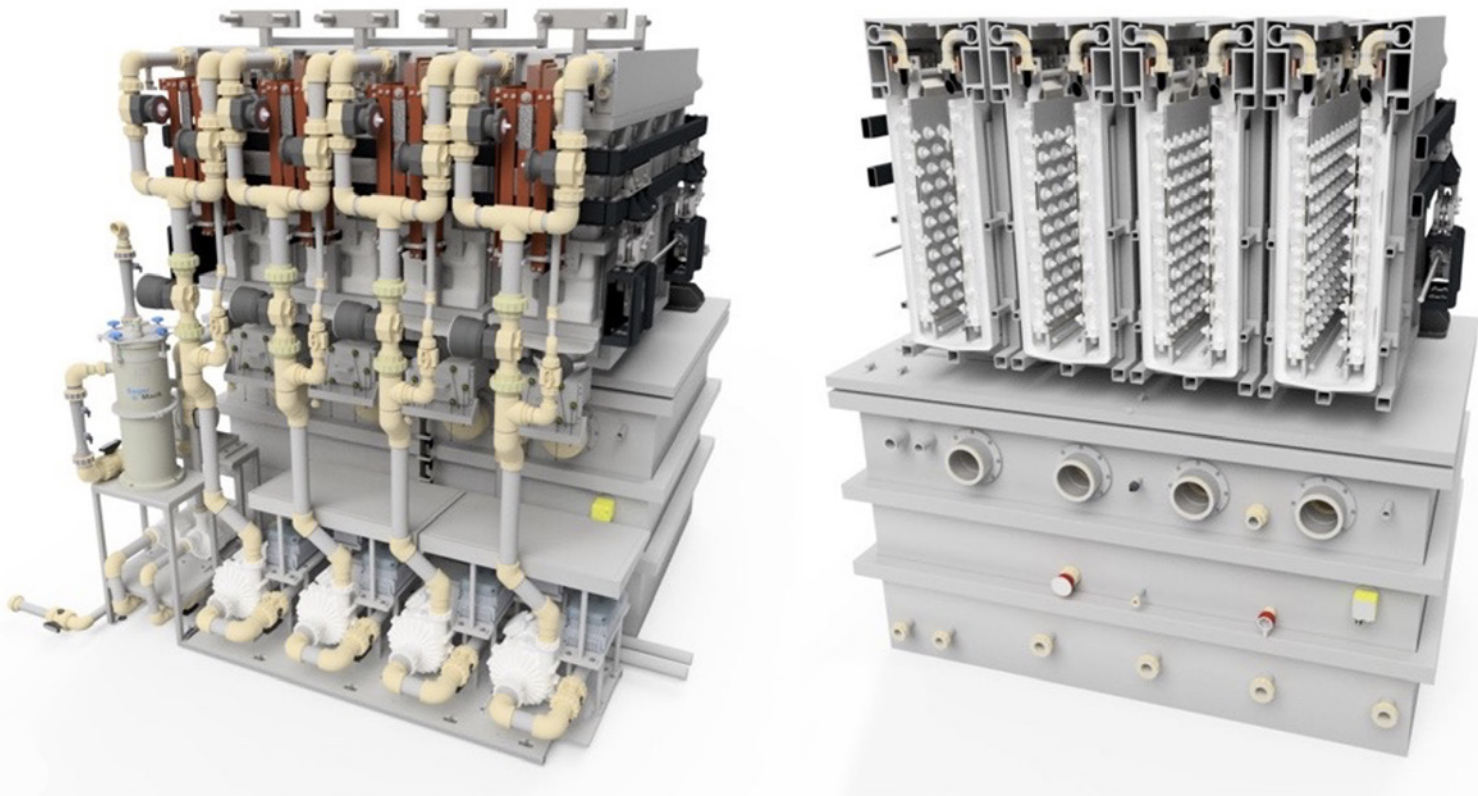


Figure 2: a) A rendering of the complete electroplating module; b) Crosssection of the electroplating cells.

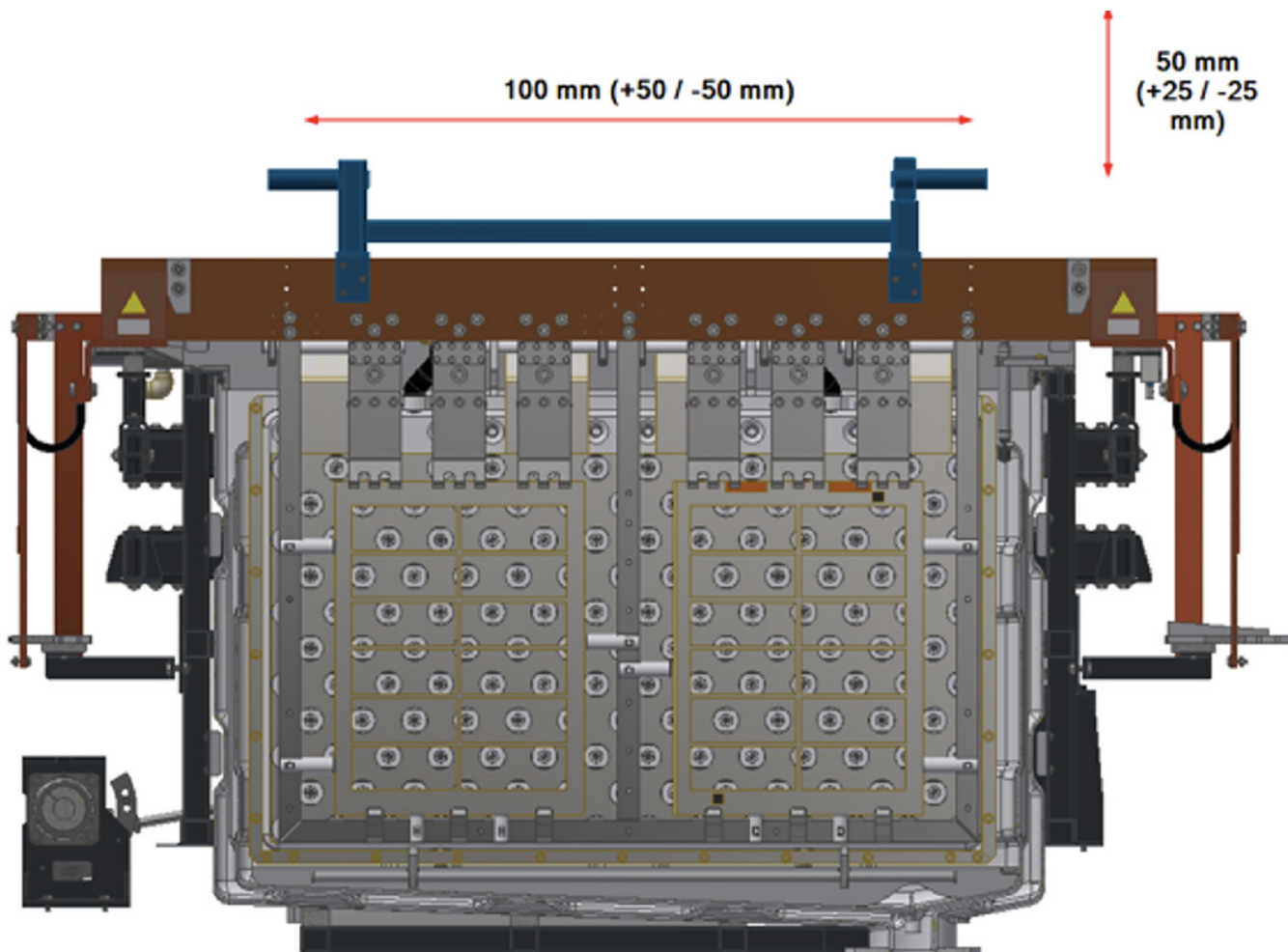


Figure 3: A schematic of the vertical and horizontal mechanical agitation illustrates the variables under study.

In effect, the team wanted to establish a baseline: How well could the system perform using process optimization alone?

Initial orientation testing already produced encouraging results. Copper distribution across the production panels measured approximately 9–10%, a level considered acceptable even before any mechanical optimization was performed.

Those results raised a natural question: If acceptable distribution could already be achieved, which process variables contributed most to that performance?

Isolating the Variables

To answer that question, the engineering team conducted a structured production-scale study using a nine-run Taguchi screening matrix.

Rather than changing multiple aspects of the plating process simultaneously, the investigation focused on three adjustable physical parameters:

- Horizontal mechanical agitation
- Vertical mechanical agitation
- Electrolyte pump pressure

All other processing conditions—including panel dimensions, plating chemistry, dwell time, current density profile, and plating module configuration—remained constant throughout the testing.

Each plated panel was measured at dozens of locations across its usable surface to evaluate copper thickness distribution while excluding nonfunctional edge regions. This allowed the researchers to isolate the influence of physical motion and electrolyte delivery without introducing additional process variables.

Unlike laboratory experiments performed under tightly controlled conditions, these trials were

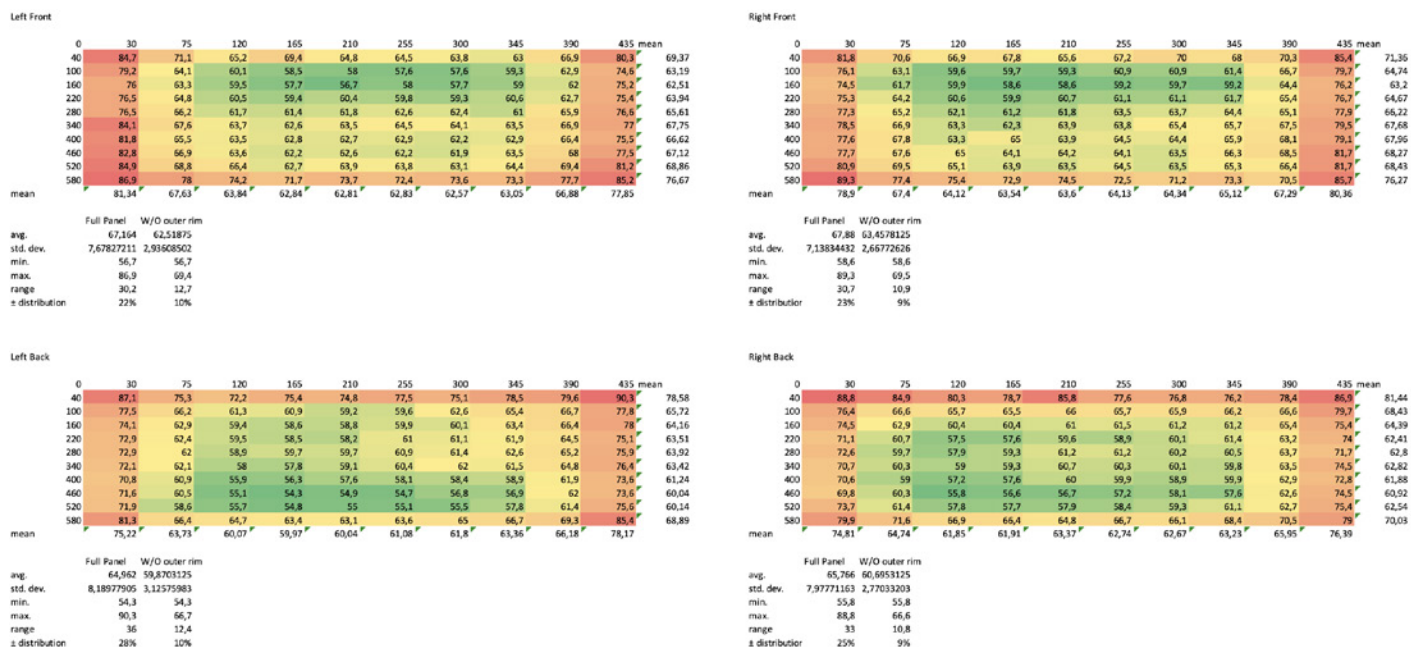


Figure 4: A distribution map of the Orientation Test, which led to interest in testing the potential influences of the physical parameters on the results.

conducted on production equipment, making the findings particularly relevant to real manufacturing environments.

What the Results Revealed

Although each of the nine test conditions produced its own distribution profile, the overall trends became clear once the data were evaluated collectively. Most importantly, the plating system consistently achieved copper distribution within $\pm 15\%$ across the panel, with many conditions approaching $\pm 10\%$ variation.

One experimental run emerged as an obvious outlier because of its lower overall plating thickness rather than an inherent distribution problem. Once that condition was separated from the broader analysis, the remaining results demonstrated remarkably consistent plating performance.

Perhaps more importantly, the data showed that the physical process variables did not contribute equally.

- Increasing horizontal agitation consistently improved copper distribution
- Increasing vertical agitation also produced measurable improvements in plating uniformity

- Conversely, increasing pump pressure beyond the lower settings proved detrimental to distribution

These findings reinforce an important principle in electroplating: More electrolyte flow is not necessarily better. Uniform mass transport depends not simply on fluid velocity but on how effectively fresh electrolyte is exchanged across the plated surface without creating localized disturbances. Mechanical agitation appears to promote that balance more effectively than simply increasing pump pressure alone.

Engineering Implications

The significance of these findings extends beyond this particular plating platform.

Electroplating optimization often begins with hardware modifications: adjusting shields, refining bussing arrangements, or altering current distribution. While those techniques remain valuable, they can also increase installation time, engineering effort, and qualification costs.

This study suggests that careful optimization of physical process dynamics may provide meaningful improvements before those additional mechanical adjustments become necessary.

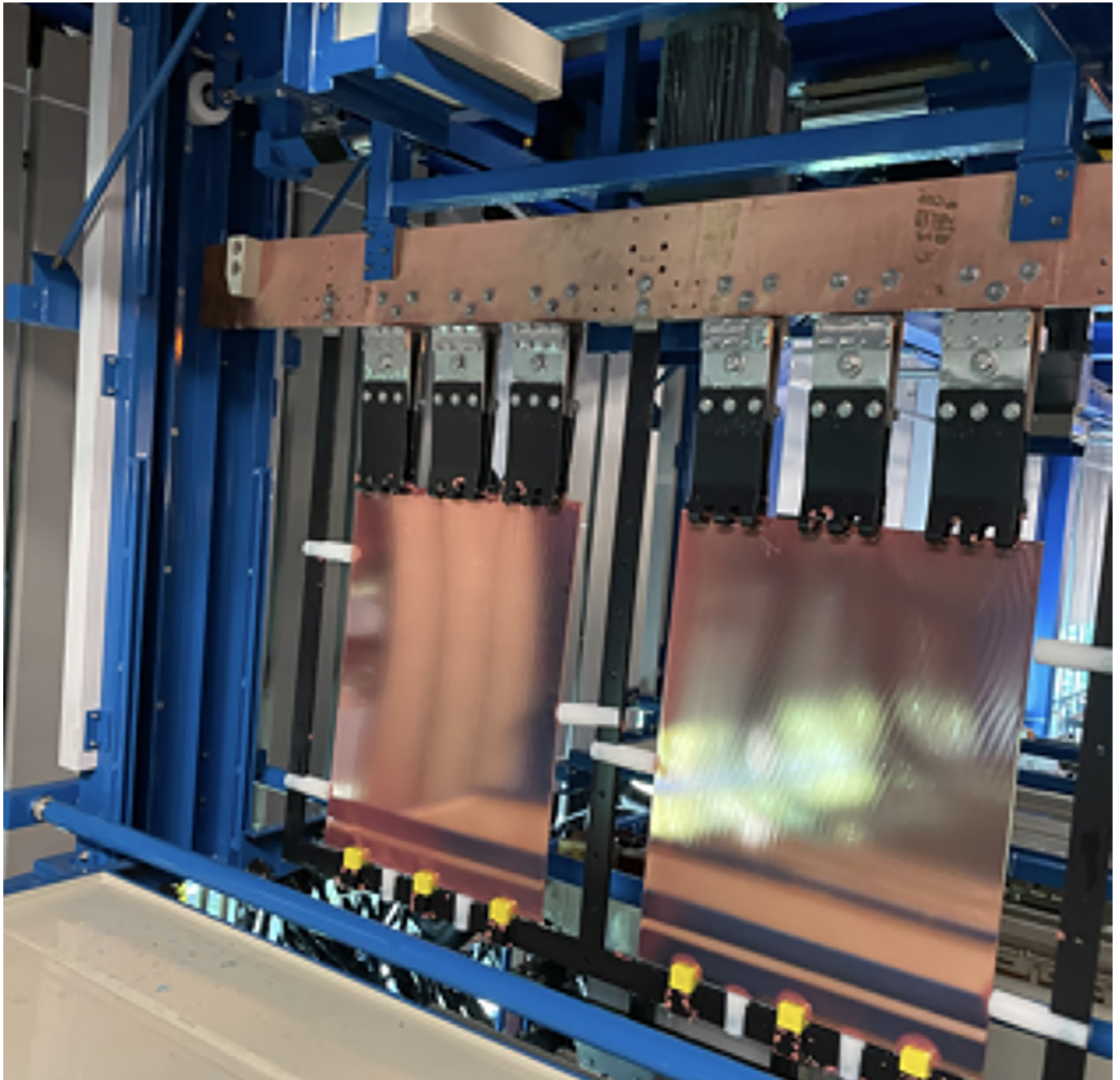


Figure 5: An actual representation of the plating equipment with finished panels.

For manufacturers installing new plating equipment, that could translate into shorter qualification cycles and fewer hardware iterations during startup.

For existing production lines, understanding how agitation and electrolyte delivery influence distribution may open additional opportunities for process improvement without major equipment modifications.

The work also highlights the importance of considering electroplating as an integrated system

rather than a collection of independent variables. Fluid dynamics, panel motion, current density, chemistry, and tooling all interact to determine the final plating result. Optimizing one variable while ignoring the others may not produce the best overall outcome.

Looking Ahead

Although the study focused specifically on copper

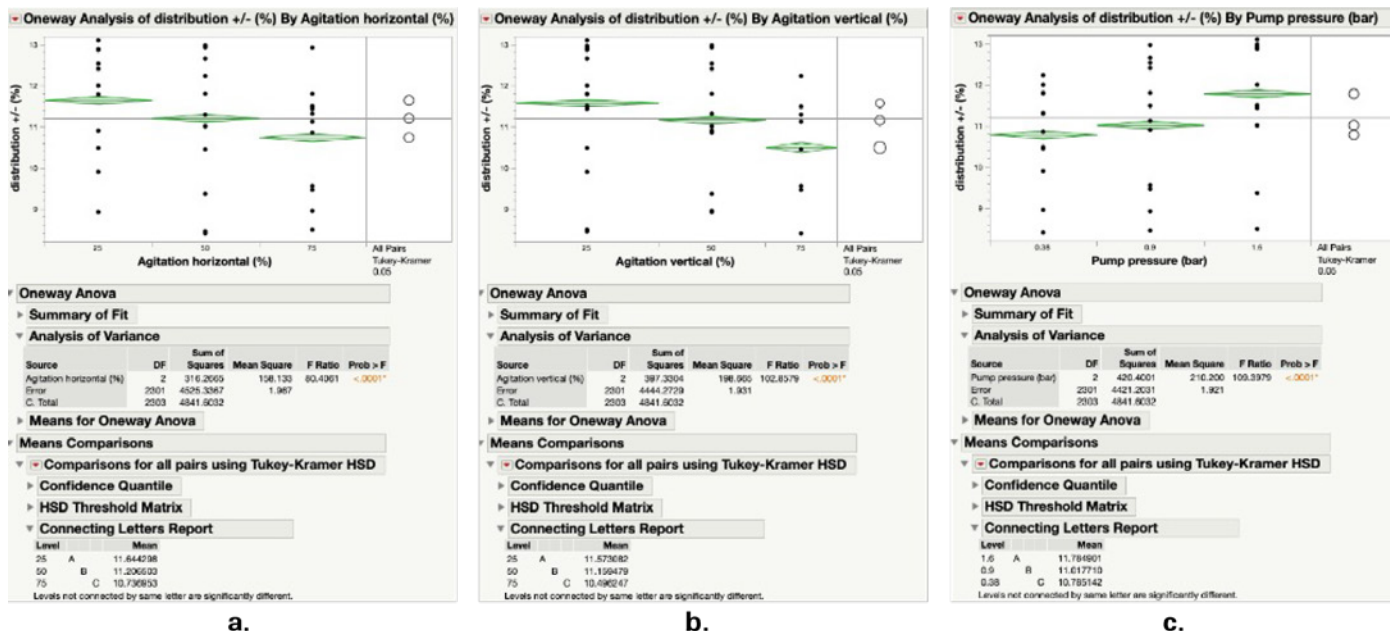


Figure 6: The final ANOVA summary supports the three principal conclusions: a) Higher horizontal agitation improves distribution; b) Higher vertical agitation improves distribution; and c) Higher pump pressure reduces distribution.

distribution, the broader implications become more relevant as PCB technology evolves.

Advanced packaging, heavy copper designs, high-power electronics, and next-generation power conversion systems all demand tighter process control than previous generations of printed circuit boards. As conductor geometries shrink while copper thickness requirements increase, maintaining consistent plating becomes more challenging.

The authors acknowledge that this work represents only the beginning of the optimization process. Future studies incorporating four-sided panel contact, shielding, and additional electrochemical refinements will likely further improve distribution.

Nevertheless, the results establish an important benchmark. Acceptable plating uniformity was achieved before those conventional optimization techniques were introduced.

That finding alone challenges the assumption that hardware modifications must always be the starting point for improving plating performance. Instead, it suggests that understanding the physical behavior of the plating process itself may offer one of the most effective, and often overlooked,

paths toward better copper distribution.

As PCB manufacturing pushes toward tighter tolerances and more demanding applications, studies like this remind us that sometimes meaningful improvements come not from reinventing the chemistry, but from a better understanding of the physics already at work inside the plating cell.

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Richard Nichols is technical marketing director, and Marko Mirkovic is the technical support and application director at GreenSource Engineering.



More Solutions to *Common PCB Etching Questions*

BY DON BALL, CHEMCUT

This month's subject is VeCS (vertical conductive structure), about which I must confess that I know absolutely nothing, since my career has mostly been focused on removing copper from the substrate rather than putting it on. To be honest, I had never even heard of VeCS until I received an email about this month's theme.

So, rather than pontificating at great length on a subject I know nothing about, although I have been known to do this on occasion (the scientific term for this is "baffling them with bull****"), I decided to

comment on some basic questions and problems that keep popping up in spite of them having been around forever and having known solutions.

Most of the inquiries come from the new process engineers who are being promoted as the older, more experienced process engineers retire. They're so basic that the older people don't even think about them anymore, let alone pass the knowledge on, so when these questions or problems arise, the new people are unaware that there are explanations and/or solutions.

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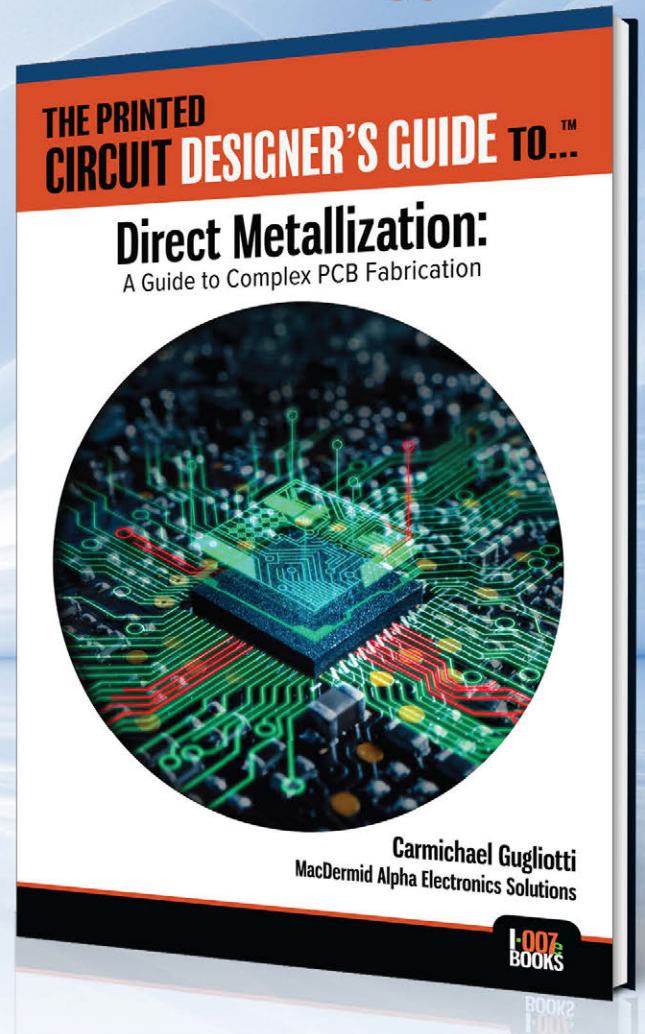
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A Sticky Situation

Here's a recent one I hadn't heard of in several years: a black, tar-like substance that builds up in the sump of a cupric chloride etcher. It coats the walls of the sump and plumbing, leaving an oily surface in the etchant sump, and eventually plugging the spray nozzles. Neither acid nor alkaline washes would get rid of this stuff.

Many years ago, this was diagnosed as organic residue leaching from the dry film etch resist as it passed through the etcher. However, the problem diminished over the years as dry film manufacturers responded by improving the product such that leaching rarely occurred. I assumed this was no longer a problem, but apparently it can still happen.



Fortunately, the solution is a simple carbon filter that removes unwanted organics and can be retrofitted as a closed-loop system on most etchers.”

Fortunately, the solution is a simple carbon filter that removes unwanted organics and can be retrofitted as a closed-loop system on most etchers. It's a good example of an old problem and an easy solution that has been forgotten because it rarely happens anymore. The main concern has been that people tend to forget the activated charcoal in the filter needs to be changed occasionally, or the problem will re-emerge. Keeping the organics out of the etch bath is simple. Cleaning it off the walls and plumbing in the etch sump after it forms is not.

Fan Fiction

One question that continually arises, especially as line and space tolerances get tighter, is “Can I get better etch uniformity and quality if I switch the etcher from cone nozzles to fan nozzles (or vice versa)?” Sadly, probably not. Nozzle dynamics is a lot more complicated than it appears on the surface.

For instance, one common misconception is that fan nozzles have better undercut performance (less undercut) than cone nozzles and therefore should give better etch quality as circuit traces and spaces get smaller because the spray is coming straight down rather than being spread out as with a cone nozzle.

However, a massive design of experiment done in conjunction with a large computer company (not IBM) showed that there was no difference under the right conditions. The experiment showed that the undercut performance of fan nozzles improved as the nozzle was moved further from the surface, and that cone nozzles performed better as they were moved closer to the surface. When each nozzle was at its optimum distance from the surface to be etched there was no difference in undercut.

The misconception probably comes from putting cone nozzles in an etcher optimized for fan nozzles and observing an increase in undercut. Another misconception is that if you have a smaller space to etch out, a nozzle with a smaller droplet size would do a better job of penetrating it. The truth is that, even with the smallest practical nozzle, the droplet diameters are still in the 500 μm range, which is still huge compared to a 50 μm space.

Also, reducing the droplet diameter by half reduces the droplet volume and therefore mass by a factor of eight. Since impact force is mass $\times$ acceleration, decreasing the droplet size reduces the impact of the droplet on the surface and results in a decrease in etch performance.

Perhaps the next time we have a monthly theme that I know nothing about (something that seems to be happening more frequently as I get older and the PCB industry gets more complicated and sophisticated) I'll go a little deeper into nozzle dynamics. By all means, feel free to experiment with spray nozzles, but don't get your hopes up too high.

That Etchy Feeling

Here's another popular and recurring question, especially for newcomers to the etch process: "Can I get better etch uniformity and etch quality by changing which etchant I use (most commonly from cupric chloride to alkaline etch)?" For etch uniformity, the answer is an unequivocal, absolutely not.

Etch chemistry has nothing to do with why a panel etches faster or slower on different areas of the board, to the point where you can no longer meet etched line width uniformity specifications for that product. These things are usually due to misadjusted etching equipment and could go as far back in the process as imaging or even panel preparation. (Plugged spray nozzles are popular, and you'd be surprised at how many people never check their nozzles.) Check these things first before wasting time on trying different etch chemistries.

As far as improvement in etch quality is concerned, the answer is a qualified maybe. Alkaline etch will definitely give you a faster etch rate and, under the proper operating parameters, will improve undercut performance, giving straighter sidewalls on the

etched line traces. This comes at the expense of more difficult etchant control and environmental discomfort (ammonia in the air is unpleasant, and the ammonia/copper complex is much harder to waste-treat). There is also a lingering misconception that ferric chloride etch gives better etch factor performance than cupric. This is not true, as discovered in the massive design of experiment mentioned above. Again, don't waste your time.

Talk about pontificating at great length. Once again, I am approaching my word count limit (I start these things thinking I can't possibly fill the space with the word count I am given and always end up having to edit for length). Anyway, I hope this has given you something to think about and maybe save you some time. **I-CONNECT007**



Don Ball is a process engineer at Chemcut. To read past columns or contact Ball, [click here](#).

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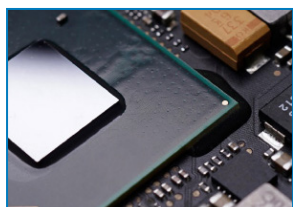


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