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INTERCONNECTING THE GLOBAL ELECTRONICS INDUSTRY



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Addressing Future Manufacturing Speed and Need



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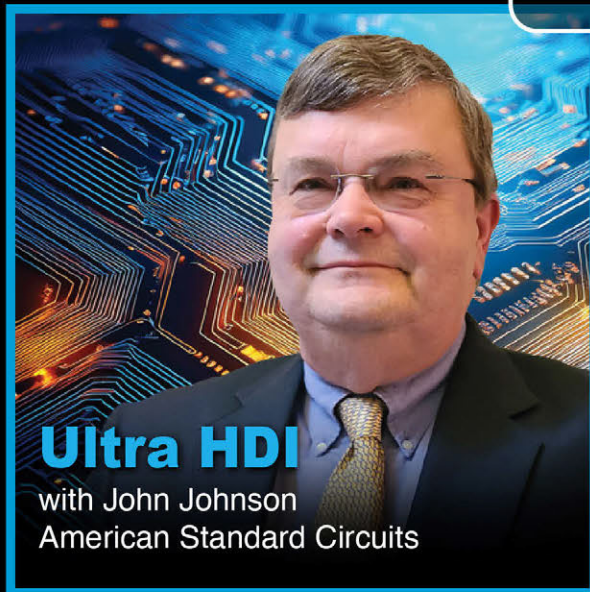
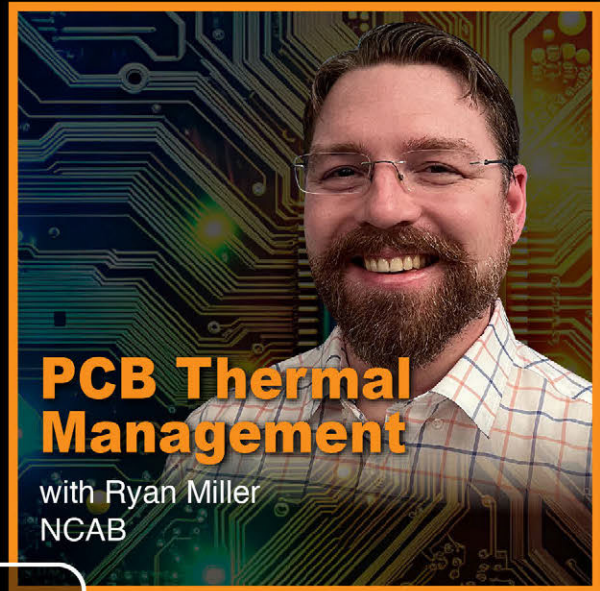
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Old School Vs. New School

Innovation rarely arrives without resistance. As PCB and systems technologies advance, engineers must decide which established practices still deliver results and which require a new approach. This issue explores the intersection of proven design principles and emerging methodologies, from AI and co-design to advanced packaging and ELIC technology.

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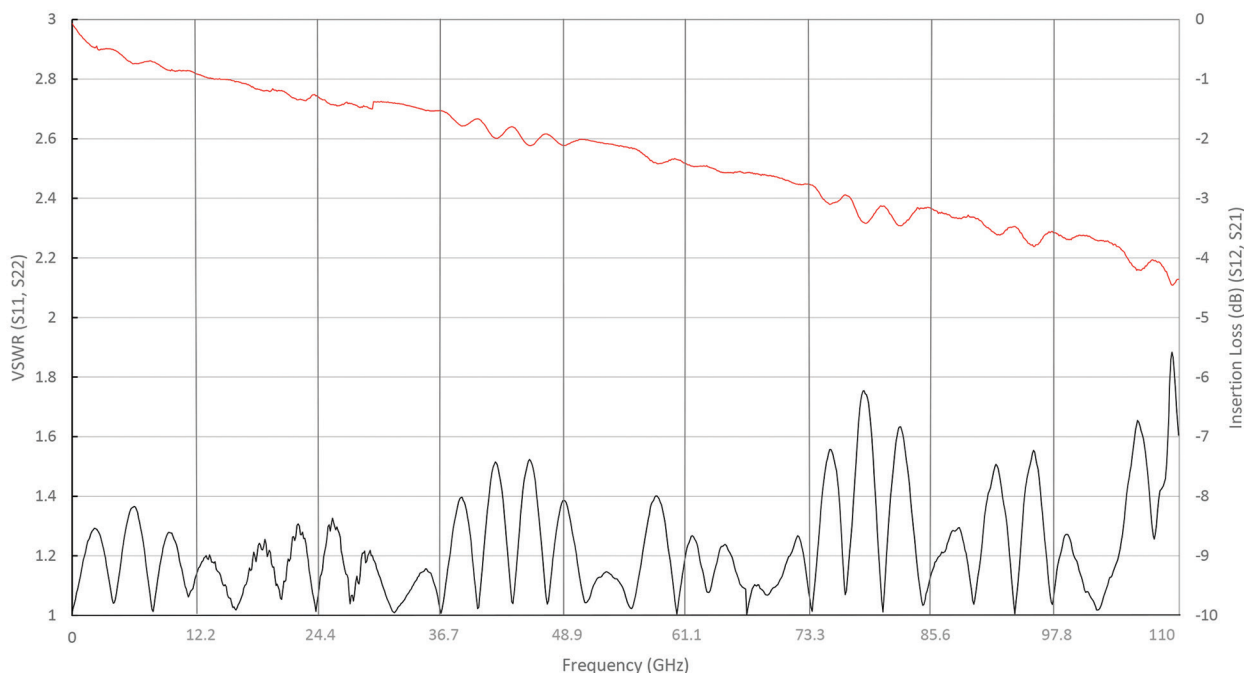
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Test Data: VSWR/ Insertion Loss



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OLD SCHOOL VS. NEW SCHOOL



BY MARCY LARONT, I-CONNECT007

The battle between old and new is nothing new. Throughout history, technological progress has faced skepticism, resistance, and at times, outright hostility. Yet progress tends to win. In his book, *RenAIssance*, author and APEX EXPO 2026 keynote Zack Kass illustrates this point beautifully. From hand weaving to sewing machines, from scribes to the printing press, from horse-drawn carriages to automobiles, and now to artificial intelligence, each technological leap has ultimately made our lives more productive and expanded what was possible.

Of course, disruptive change is rarely comfortable. That's why it's important to separate genuine innovation from hype. This month, our contributors tackle that question as we explore old-school vs. new-school thinking in PCB and system design.

Several authors argue that new approaches are not simply preferable; they are becoming necessary. In his column, Barry Olney says that as data rates push beyond 112G PAM4 toward 224G PAM4 and beyond, traditional stripline and microstrip geometries are reaching their limits. In some cases, the physics simply no longer cooperate.

Columnist Matt Stevenson challenges traditional

supplier-selection methods with the concept of total value management (TVM). Rather than focusing primarily on cost, TVM emphasizes collaboration, innovation, agility, and long-term partnership. The best manufacturing partners, he says, help customers navigate increasingly complex prototyping and production decisions, whether domestic or offshore.

Likewise, new contributor Pentalogix argues that the long-standing practice of “throwing designs over the wall” to fabricators is no longer sustainable. Designers and manufacturers must communicate continuously for meaningful progress to occur.

Kristin Moyer explores another shift in thinking through a discussion of concurrent design vs. co-design. While concurrent design allows multiple disciplines to work in parallel, co-design leverages integrated data environments that enable electrical, mechanical, RF, thermal, and other engineers to collaborate simultaneously. The result can be shorter development cycles, fewer revisions, lower costs, and higher first-pass success rates.

Vern Solberg also lands firmly in the new-school camp by examining advanced packaging technologies and the expanding role PCB designers

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must play as electronic systems become increasingly integrated.

Not everyone is ready to abandon traditional thinking, however. John Watson opens his column with Jean-Baptiste Alphonse Karr's famous observation: "The more things change, the more they stay the same." While PCB design tools and technologies have evolved dramatically since the days of Mylar tape, Watson reminds us that the fundamental principles of good design remain remarkably consistent. Watson also expanded on this theme in a recent edition of *Design007 Week*, where he took a critical look at how to educate designers for the future.

Stephen Chavez examines using digital twin in design. Kelly Dack continues his exploration of signal integrity influencers in the second part of his series on "Signal Integrity Without Borders," reinforcing that while technologies change, the underlying engineering disciplines remain essential.

On the fabrication side, we explore one of the industry's newest frontiers: every layer interconnect (ELIC), sometimes called every layer microvia (ELMV). The technology is so new that the industry has yet to settle on a single name.

Anaya Vardya of ASC introduces ELIC technology, explaining its capabilities, density advantages, and manufacturing challenges. Ralph Jacobo of all4-PCB discusses the critical role equipment technology plays in supporting the multiple lamination cycles required for these advanced stackups. Materials expert Ed Kelley rounds out the conversation by examining material selection, high-speed performance, and microvia reliability considerations in staggered and stacked microvia designs.

Our PCB columnists cover a diverse set of topics. Don Ball tackles common etching questions and challenges the long-held assumption that faster is

always better. Mike Carano examines insertion loss and signal distortion associated with final surface finishes, including the impact of roughness and nickel thickness on signal performance. Meanwhile, Shane Whiteside provides an update on the Printed Circuit Board and Substrates Act as it advances through Congress.

Additional features include Richard Nichols' case study on achieving extremely high aspect ratios, Anaya Vardya looking at flex in medical technology and PCBs, and Sean Patterson has a practical roadmap for AI adoption within PCB manufacturing operations.

We also celebrate EPTAC's new headquarters and long-standing contributions to industry training, and share highlights from my recent visit to Schneider Electric in Buffalo, New York, where I learned more about the AI-driven data center infrastructure reshaping the electronics supply chain.

As you read through this issue, I encourage you to consider which ideas truly represent the future and which enduring principles still deserve a place in our toolbox. After all, progress is rarely about replacing everything that came before. More often, it's about knowing what to keep, what to improve, and what to leave behind. **I-CONNECT007**



Marcy LaRont is the managing editor of *I-Connect007 Magazine* and executive director of IPC Publishing Group. Marcy started her career in PCBs in 1993 and brings a wide array of business experience and perspective to *I-Connect007*. To contact Marcy, [click here](#).

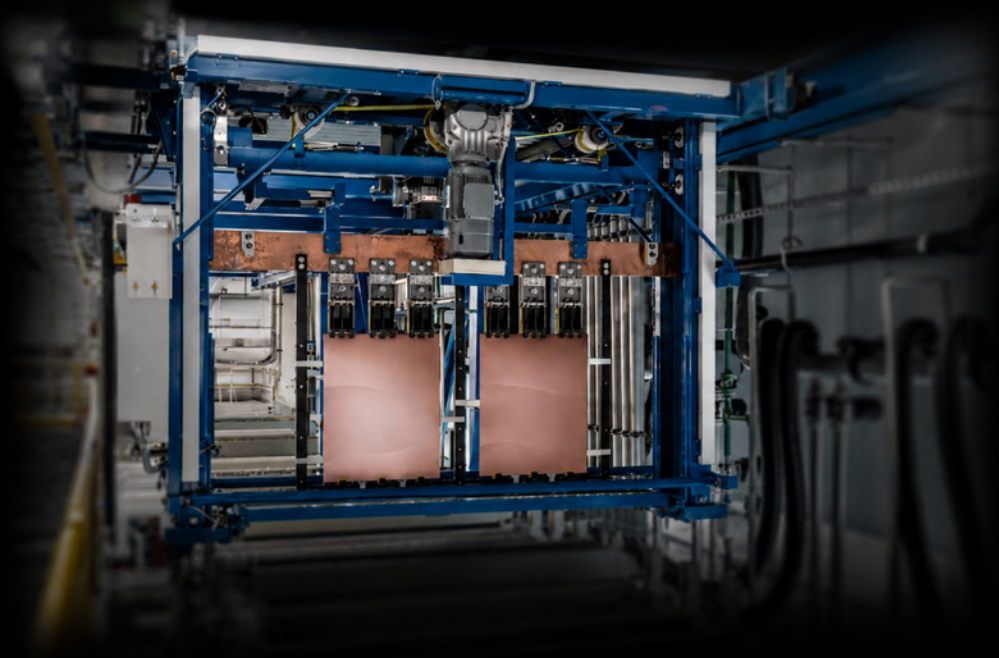
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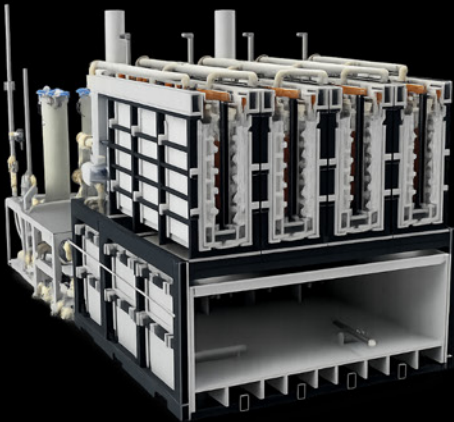
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Every Layer Interconnect

The Promise, the Pain, and the Practical Limits

Every layer interconnect (ELIC) is an architectural statement about how a PCB is built, signaling a fundamental shift in how we think about routing density, vertical interconnect, and the relationship between design and fabrication.

To understand what ELIC solves, you have to understand what it replaces. Traditional HDI construction uses a rigid core with sequential build-up layers on one or both sides: configurations such as 2-4-2 or 3-2-3. In those designs, microvias connect only

adjacent build-up layers. Through-holes serve the core. The result is a predictable, well-characterized architecture, but one that is fundamentally limited in how tightly you can pack interconnects, because the through-hole barrel consumes real estate from one side of the board to the other regardless of whether the signal needs to traverse every layer.

ELIC eliminates the through-hole as the primary vertical interconnect. In a true every-layer interconnect architecture, each layer connects to the adja-



Figure 1: ELIC architecture (left) eliminates through-hole barrels and makes every layer available for routing. Traditional 2-4-2 HDI (right) requires a mechanical through-hole barrel that consumes board space across all layers regardless of signal routing need.

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What is ELIC?

Every layer interconnect (ELIC) is a PCB fabrication architecture in which every layer connects exclusively to adjacent layers through laser-drilled microvias, eliminating mechanical through-holes as the primary vertical interconnect. Unlike traditional HDI constructions such as 2-4-2 or 3-2-3, where through-holes serve a rigid core and microvias only connect build-up layers, ELIC makes every layer a fully usable routing layer. The result is higher routing density, smaller pad footprints, fewer total layers, and elimination of via stubs, at the cost of significantly greater fabrication complexity and process discipline.

cent layer above and below exclusively through laser-drilled microvias. Every layer is a potential routing layer. Pads only occupy the layers where the net actually needs to be. The via stub disappears, and the annular ring footprint shrinks. The result is a board that can support the escape routing demands of the most aggressive sub-100-micron pitch BGAs and advanced packaging formats without sacrificing layers to plumbing that was never needed in the first place.

What’s driving this? Semiconductor packages are shrinking their pitch while increasing I/O count. SoCs, advanced memory stacks, and RF front-end modules are pushing designers into territory where traditional HDI construction cannot provide enough

routing channels in the available space. Board thickness envelopes are also tightening in wearables, implantables, and aerospace avionics. Every millimeter of Z-axis matters and ELIC addresses all of these simultaneously.

At ASC, we have been building HDI boards for over a decade and have expanded into UHDl fabrication with the SAP and thin-foil processes, enabling sub-25-micron line and space capability. What we see clearly from the fabricator’s seat is that ELIC is not simply an upgrade to HDI. It is a different manufacturing philosophy, much closer in process complexity to semiconductor packaging than to traditional multilayer PCB fabrication. That distinction shapes every conversation about design intent, material selection, registration tolerance, and yield. These are the variables that ultimately determine whether an ELIC program succeeds or struggles.

How Dense Can You Feasibly Get With ELIC?

The theoretical density ceiling for ELIC means that by eliminating the through-hole barrel and connecting every layer through microvias, designers can route signals through a much smaller pad footprint and recover routing channels that would otherwise be blocked. In practical terms, a well-executed ELIC stackup can support line-and-space geometries down to 25 microns in HDI territory, and sub-25 microns when combined with semi-additive processes like mSAP or SAP.

Counts that would require 20 or more layers in a

Table 1: Understanding this gap is foundational to ELIC design.
Minimum capability is a process boundary.

DESIGN CAPABILITY	PRODUCTION REALITY
Minimum geometry limits	Yield variability across production panels
Ideal material behavior	Material variation and CTE effects across cycles
Perfect layer-to-layer alignment	Registration tolerance that compounds with each cycle
Single successful build	Statistical process spread across volume production

conventional multilayer architecture can sometimes be achieved with ELIC in 12 to 14 layers, because every layer is genuinely usable for routing. That is a meaningful reduction as it affects board thickness, material cost, lamination cycle count, and the mechanical profile of the final assembly.

The most important perspective shift for ELIC designers is understanding the gap between design capability and production reality (Table 1).

From our production experience at ASC, ELIC becomes genuinely compelling when three conditions converge: component pitch below 0.35 mm, layer count demands beyond what a 2-4-2 or 3-2-3 configuration can support, and board real estate constraints that prevent spreading components to ease routing pressure. When all three are present, ELIC is often the only viable architecture.

The feasibility question is more nuanced than the theoretical ceiling suggests. Minimum capability is not the same as production capability. Designing at

the absolute process limit—minimum vias, minimum dielectrics, minimum mask clearances everywhere—is a reliable path to yield loss. The better question is what the fabricator’s comfortable production range is, not the theoretical minimum.

What Are the Biggest Manufacturing Challenges in ELIC?

When customers ask about the single biggest challenge in ELIC vs. traditional stacked or staggered microvia HDI, it’s not any one variable. It is the compounding relationship between variables that would be individually manageable in simpler architectures but become interdependent failure modes in ELIC. Small variations do not stay small; they stack.

Registration Across the Entire Stack

Registration is the ability to hold intended positional relationships between features during fabrication: copper layer to copper layer, drilled features to capture pads, and solder mask openings to copper.

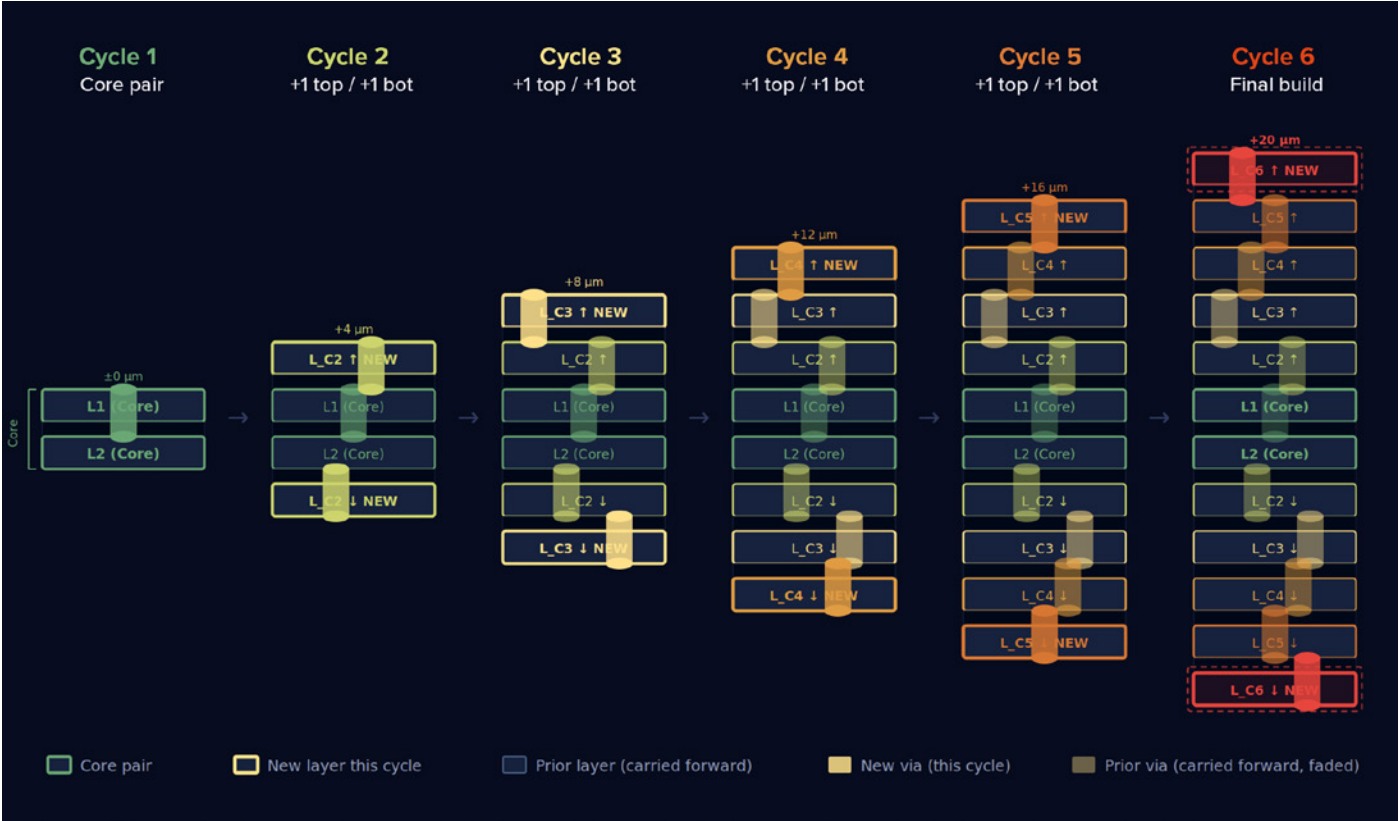


Figure 2: ELIC is built from the center outward; each cycle adds one layer to the top and one to the bottom. A ~4 μm positional shift introduced at any cycle propagates outward through every subsequent build. By Cycle 6, the outermost layers carry the full accumulated drift of ~20 μm, consuming most or all available capture pad margin in a 50–75 μm ELIC design.

Unlike HDI, which builds outward from a pre-drilled core, ELIC begins at the center with a core pair—L1 and L2—and adds one new layer to the top and one to the bottom with each sequential lamination cycle. This means registration errors do not simply accumulate from one end of the build to the other; they propagate symmetrically outward, and the outermost layers carry the greatest total positional uncertainty from the full history of the build.

A positional shift of $\pm 10\text{--}15\text{ }\mu\text{m}$ may be inconsequential on a forgiving HDI structure. On a UHDl design built around $50\text{--}75\text{ }\mu\text{m}$ microvias and reduced capture pads, that same shift can materially reduce the usable landing margin. In a six-cycle ELIC build, a registration error introduced in Cycle 2 persists in the final outer layers. It is never corrected, only added to. The designs that survive this are the ones that account for realistic process window behavior, not ideal alignment.

We have addressed this by investing significantly in imaging and lamination registration systems, specifically because ELIC tolerates less drift than any prior construction we have built. Process control around panel expansion coefficients, tooling

systems, and material conditioning before lamination matters equally: these are process disciplines, not equipment specifications.

Common registration-driven failure modes in ELIC include partial microvia capture, microvia breakout, stacked via misalignment accumulating through successive layers, solder mask encroachment onto exposed pads, insufficient mask dams leading to bridging risk, and trace exposure from shifted outer-layer relationships. None of these is a random event. They are predictable consequences of insufficient design margin in the presence of normal process variability.

Lamination Cycles and Cumulative Thermal Stress

Every sequential build-up cycle adds thermal exposure to the materials already built. This is manageable in a two-cycle HDI board. In ELIC with six, eight, or more sequential lamination events, each cycle exposes prior copper and dielectric to temperatures and pressures that induce stress and dimensional change. Materials must be specifically qualified for repeated thermal cycling without de-



Figure 3: A $15\text{ }\mu\text{m}$ registration shift reduces capture pad annular ring from $25\text{ }\mu\text{m}$ to $10\text{ }\mu\text{m}$, substantially increasing breakout risk. In ELIC, this condition exists at every level of the stack and compounds with each cycle.

lamination, Z-axis expansion, or degradation of dielectric properties.

Not all materials that perform well in a two-cycle HDI build will hold up in a six-cycle ELIC build. The materials that meet the required criteria—thin build-up films, select resin-coated foils with high dimensional stability and good laser drill response—are not commodity items. They are sourced from a limited set of suppliers, and material availability for qualified high-cycle laminates is a genuine operational constraint for North American fabricators.

Via Reliability: The Risk That Compounds With Every Layer

The PCB industry has been working through stacked microvia reliability issues for over a decade. IPC white paper IPC-WP-023, “Performance-Based Printed Board OEM Acceptance—Via Chain Continuity Reflow Test: The Hidden Reliability Threat,” documented field failures in HDI boards with stacked vias, traced to incomplete copper fill and electroplating conditions that created a weak interface at the microvia-to-target-pad junction. In ELIC, this problem multiplies with every additional stack level.

The most critical process control point in ELIC is copper fill quality at each microvia level before the next build-up layer is applied. An incompletely filled microvia creates a void, which becomes a stress concentration point under thermal cycling. In a two-level stack, a void may be caught by cross-section inspection. In a six-level stack, a void three layers deep may not be detectable by standard AOI and may only reveal itself after assembly or in the field.

Our process for ELIC at ASC requires 100% cross-section sampling at defined build intervals and electroplating chemistry management that is significantly tighter than what we apply to standard HDI builds. This is non-negotiable for production yield and reliability.

Material Cost and Cycle Time

ELIC builds differently from a cost and throughput standpoint. The unit cost of specialty dielectric layers is higher than commodity laminates. The lami-

“**ELIC is not simply an upgrade to HDI. It is a different manufacturing philosophy, much closer in process complexity to semiconductor packaging.**”

nation cycle count is higher. Per-panel throughput is lower because each sequential cycle requires the panel to move through imaging, laser drill, desmear, plating, and inspection before returning for the next cycle. Build time is measured in days per sequential cycle, not per board.

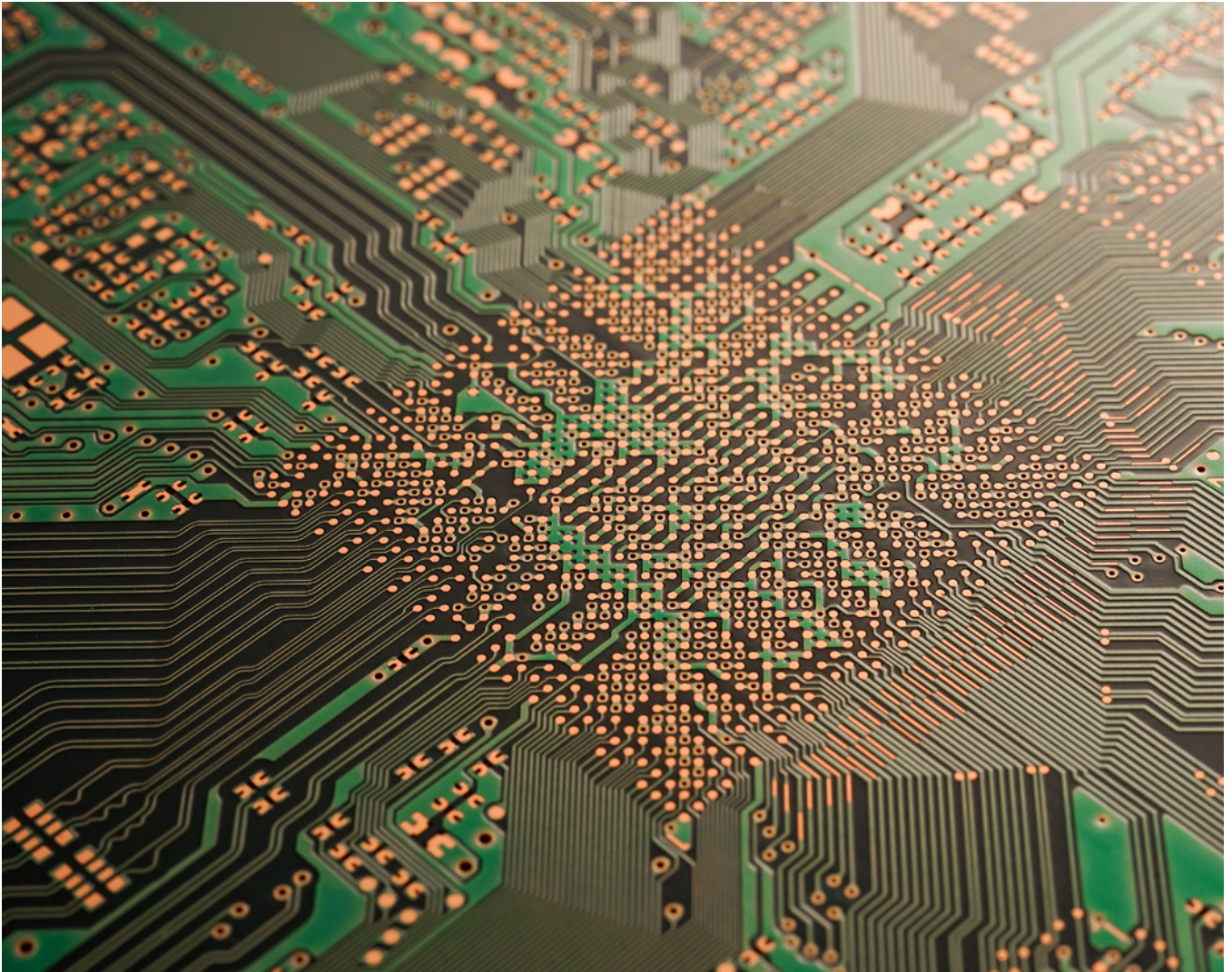
Customers accustomed to standard HDI lead times are often surprised by ELIC cycle time. For applications requiring short-turn prototypes, ELIC requires early commitment to a fabricator with dedicated capacity and the process infrastructure to support rapid sequential cycling without sacrificing process control at each step. **I-CONNECT007**

Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals*. He is the author of *Thermal Management: A Fabricator's Perspective*, *The Printed Circuit Designer's Guide to DFM Essentials*, and *The Companion*



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Base Material Properties *and Microvia Reliability*

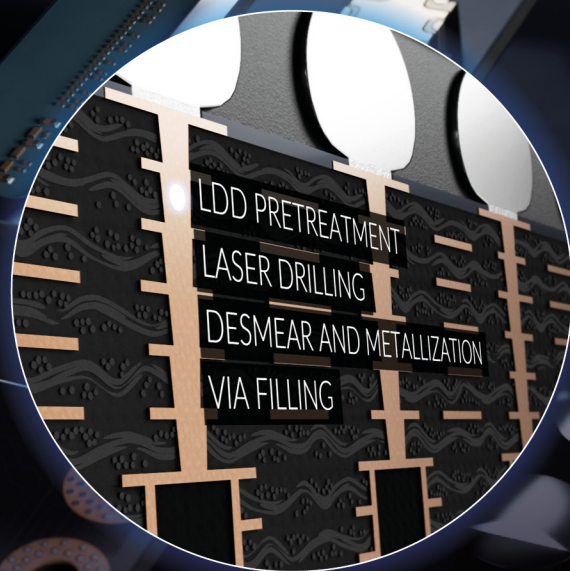


The drive toward higher circuit density is challenging PCB manufacturers and their supply chains alike, with base materials as a critical foundation for complex designs. HDI designs present specific challenges and requirements for these materials, but given the myriad possible designs and applications, there is no optimal “one size fits all” material. Perhaps the most challenging HDI designs

are those that use stacked vs. staggered microvias, with the number of layers of stacked microvias and the pitch between them as critical variables.

Staggered microvias are offset on adjacent layers with separate drill axes. They distribute mechanical stresses more evenly across a larger area and, therefore, are generally more reliable. Stacked microvia designs enable more dense circuit routing but carry

AI server PCBs and advanced packaging require highest copper reliability



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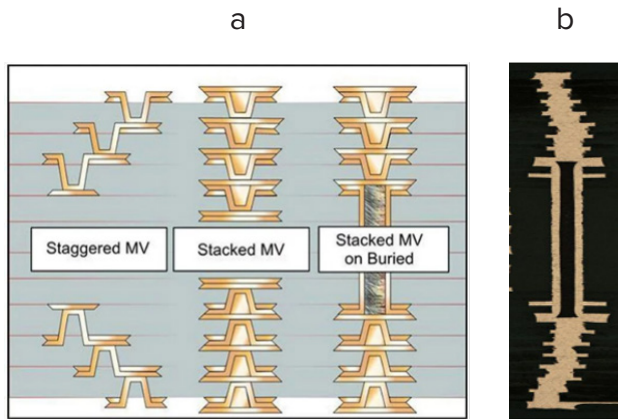


Figure 1: a) Illustration of staggered vs. stacked microvias; b) Seven stacked microvias on a buried multilayer sub-PCB.

higher reliability risks under thermal cycling.

Staggered designs offer better durability at the cost of board real estate, whereas stacked microvias, with an increasing number of layers, are required for high-performance applications, including AI, high-performance computing, and networking equipment. While PCB drilling and plating processes are critical to microvia reliability, base material properties will also determine whether these structures survive assembly processes and field operation for the expected service lifetime.

As a PCB undergoes thermal cycling, first with exposure to high temperatures in reflow assembly processes, and then in the operating environment, these microvias are subjected to various thermomechanical stresses. The actual level of these stresses will be affected by the specific PCB design features, including the number of layers of microvias, the individual dielectric thicknesses and resin contents, as well as the geometries of the micro-

vias, including whether staggered or stacked. A few types of microvia defects related to material properties are shown in Figure 2.

From a base material perspective, there are a few critical properties to consider.

Thermal Expansion Properties

Glass-reinforced thermoset laminate and prepreg materials will have different CTEs in the X-Y and Z directions. While X-Y CTEs are important, especially when considering large-format component packages, for microvia reliability, Z-axis thermal expansion is most critical.

Glass Transition Temperature (T_g)

The T_g of a material represents the temperature at which it transforms from a rigid, “glassy” state to a softer, more flexible state. While T_g is usually reported as a specific temperature, there is a temperature range over which this reversible process takes place (Figure 3a). The key point regarding microvia reliability is that CTE values above T_g will be much higher than those below T_g. This is why higher-T_g materials are generally preferred for the most complex designs. However, it is important to understand how the T_g and pre- and post-T_g CTEs combine to result in a total expansion over the temperature range of interest.

Figure 3a illustrates how T_g is determined by thermomechanical analysis (TMA). The benefit of using TMA to determine T_g is that it also provides pre- and post-T_g CTE values for a material. Figure 4 shows an actual TMA scan, including the T_g and pre- and post-T_g CTE values.

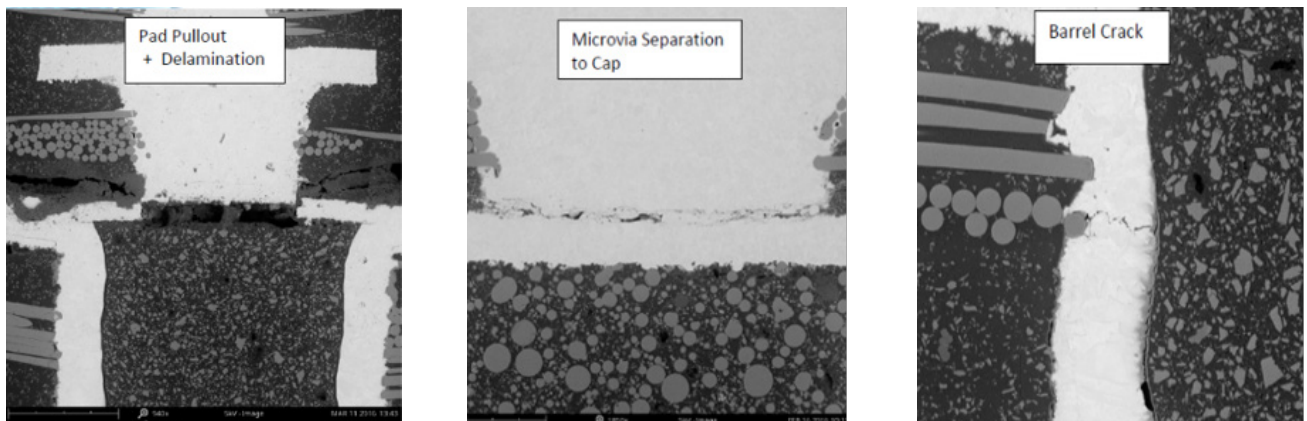


Figure 2: Examples of microvia defects.

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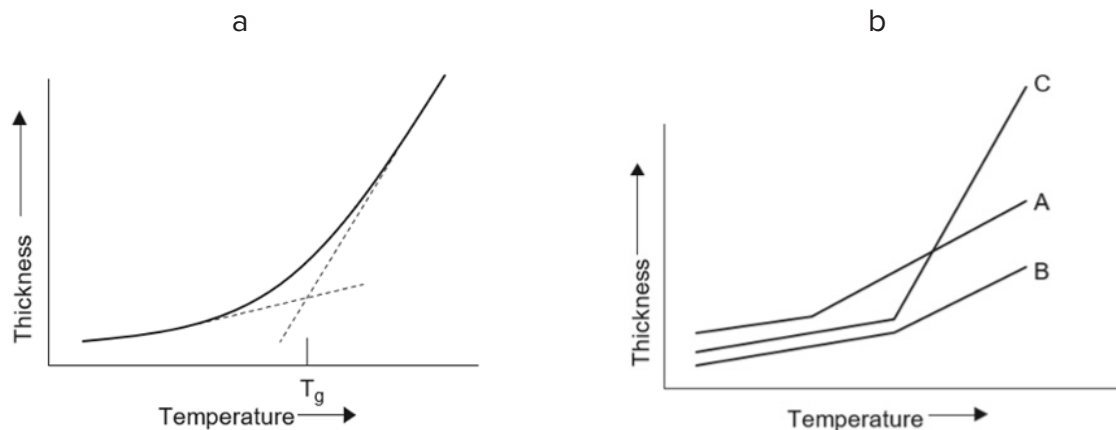


Figure 3: a) TMA measurement of T_g ; b) TMA T_g comparisons of materials.

But note the differences among the three materials, as illustrated in Figure 3b. Products B and C have the same T_g value, but Product C obviously expands much faster vs. temperature above the T_g than Product B, resulting in significantly more total thermal expansion. On the other hand, Product A has the lowest T_g , but exhibits less total expansion than Product C, because of a lower post- T_g expansion rate.

strain. So, a high-modulus material is very stiff, and a low-modulus material is more flexible or rubbery. “Storage Modulus” values determined through dynamic mechanical analysis (DMA) are often reported for base materials. For polymers below the T_g , Young’s modulus and storage modulus values are almost the same. Note, however, that as materials exceed the T_g , modulus values will decrease dramatically. Figure 5 illustrates how Young’s modulus is determined but note that different materials can have very different-shaped curves.

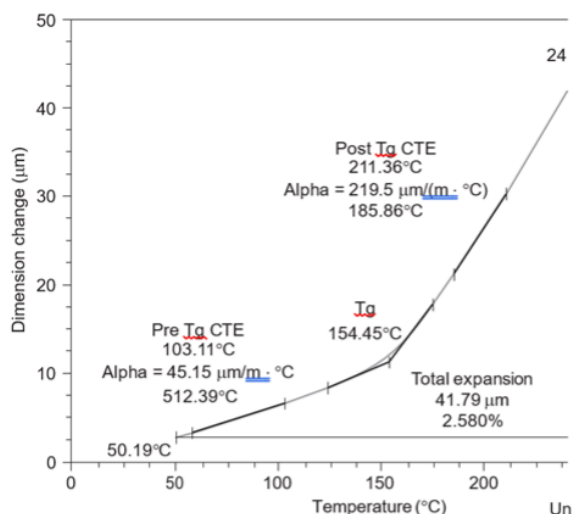


Figure 4: Example of an actual TMA scan.

Figure 4 is an actual TMA scan, showing the T_g at 154°C and pre- and post- T_g CTEs of $45 \text{ ppm}/^{\circ}\text{C}$ and $220 \text{ ppm}/^{\circ}\text{C}$, respectively.

Modulus

The modulus is usually thought of as a measure of a material’s stiffness, or how much it resists deformation under an applied stress. Specifically, Young’s Modulus is the ratio of tensile stress to tensile

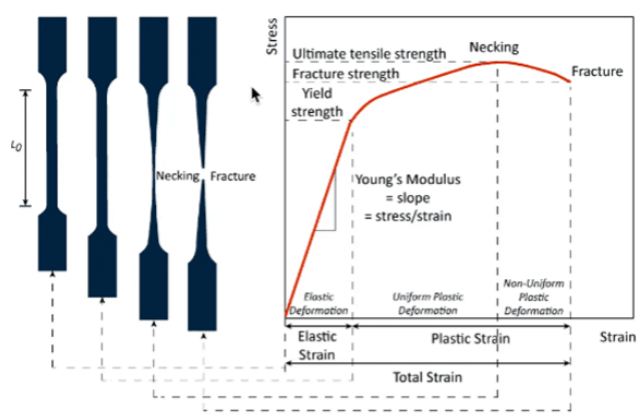


Figure 5: How Young’s modulus is determined.

Considerations for Microvia Reliability

In PCBs with multiple layers of microvias the primary failure mechanism is thermo-mechanical stress from CTE mismatch. Copper expands at approximately $17 \text{ ppm}/^{\circ}\text{C}$ while the dielectric layer expands at much higher rates. This exerts tensile and shear forces on via walls, pads, and interfaces. Cooling reverses this but potentially leads to fatigue crack-

Tips for High Reliability in “Many-layer” Stacked Microvia Designs

 Select materials with very low Z-axis thermal expansion in temperature ranges of interest. In practice, this is achieved by combining a high T_g with very low pre- and post-T_g CTE values.

 Note that selecting a material with a T_g above the expected operating temperature means that the pre-T_g CTE will be the most important property for long-term reliability. But given that assembly process temperatures typically exceed material T_gs, selecting materials with high T_gs, which delays the onset of rapid post-T_g CTE, is also beneficial. This helps prevent via damage during assembly that can also compromise long-term reliability.

 Understand how modulus values impact performance. High-modulus materials maintain dimensional stability and resist warpage, which is beneficial for flatness in multilayer builds, but they transfer more stress to microvias, increasing the risk of cracking.

 When multiple build-up layers are used (and therefore multiple lamination cycles), it is also important to understand whether the material properties change as they are exposed to these thermal cycles. While most high-performance materials will not exhibit significant changes in properties, some materials will exhibit slight increases in modulus vs. thermal cycle, for example. Most material suppliers should be able to provide this data.

 In glass-reinforced microvia dielectric layers, use of spread-glass fabrics can improve the distribution of the glass filaments within the dielectric, minimizing stress concentration due to glass-rich areas vs. resin-rich areas, as the glass will have a much lower CTE than the resin. In addition, spread-glass fabrics can improve the quality of the via wall.

 There are an increasing number of non-glass reinforced materials available for microvia build-up layers. By removing the glass fabric, more uniform via walls can be achieved and the stress concentrations caused by inhomogeneity of resin and glass in the dielectric can be eliminated. On the other hand, make sure that this does not lead to increases in CTEs that offset the benefit. The non-glass-reinforced material needs to be very low in CTE.

 Lower-modulus dielectrics provide compliance, absorbing some Z-expansion and reducing peak stresses at via interfaces. This can enhance reliability in complex designs. However, excessively low modulus may worsen warpage or reduce overall board rigidity. In PCB designs using a multilayer sub-PCB with many microvia layers added, one approach, when possible, is to use higher-modulus materials in the sub-PCB to provide rigidity and resistance to warping, and lower-modulus materials in the build-up layers, as long as those build-up layers also have low CTE values.

ing over many cycles. While the properties of the copper plating in microvias will interact with the dielectric materials, excessive mismatches in thermal expansion between copper and dielectric can result in the defects shown in Figure 2.

Staggered microvias can distribute stress across capture pads and the surrounding dielectric, reducing the localized strains. In stacked microvias, stresses accumulate along the vertical column. A single microvia may tolerate mismatch, but multiple levels amplify strain at joints and copper fill interfaces. Rough hole walls after via formation and glass-rich vs. resin-rich areas of the dielectric can also concentrate stresses in localized areas within the via (as shown in the barrel crack in Figure 2).

In an ideal world, there would be one material to recommend across various designs. But as engi-

neers and businesspeople, we want to select the most cost-effective material that meets the reliability requirements of various designs and applications. For high reliability in “many-layer” stacked microvia designs:

While beyond the scope of this article, finite element analysis (FEA) of specific designs can be very helpful, as long as the properties for the actual materials used are known. **I-CONNECT007**



Ed Kelley is vice president, materials technology, at Victory Giant Technology (Huizhou) Co. Ltd.

Building Better HDI Boards

Driving Quality Through Lamination



All4-PCB, a technology-focused supplier serving the PCB, IC substrate, chemical milling, and LTCC markets, works with manufacturers across North America to deliver equipment, materials, and process solutions that address the lamination challenges of HDI, advanced packaging, and complex multilayer designs. Under the leadership of Managing Director Ralph Jacobo, the company has continued expanding its support for advanced electronics manufacturing operations.

Among its key partnerships is Lauffer, the Germany-based press manufacturer founded in

1872 and widely recognized for its hydraulic and electric lamination press systems. Lauffer's technology is increasingly relevant as PCB fabricators confront the demands of higher layer counts, sequential lamination cycles, and every layer interconnect (ELIC) designs. Ralph discusses the role of lamination in advanced PCB fabrication, and how Lauffer's approach to automation, process control, and material handling is helping manufacturers improve quality, registration, and reliability in some of today's most demanding builds.

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Marcy LaRont: Ralph, when we met in April, all4-PCB had recently announced growth in the U.S. market with Laufer's lamination products. Tell me more about that.

Ralph Jacobo: Our partnership with Laufer in the U.S. goes back several years. Over that time, we have seen growing demand for lamination press technology. Much of that demand is driven by facility expansions, the need for increased production capacity, and the replacement of older press systems that cannot maintain the quality and consistency required for today's advanced PCB designs and higher-tech products.

Lamination is a key process, especially when multiple lamination cycles are involved. What defects arise when the lamination process is not well controlled?

PCB technology is demanding tighter lines and spaces, higher layer counts, and more sequential lamination cycles. In addition, manufacturers are increasingly using specialized high-speed, low-loss materials, which introduce even more complexity into the process.

Because of this, lamination has become one of the most critical, yet often overlooked, steps in PCB manufacturing. Problems during lamination can result in yield loss, delamination, voids or trapped air pockets, and insufficient adhesion between layers, all of which can significantly impact the reliability and performance of the final PCB.

Achieving a successful and repeatable lamination process requires a combination of factors, including the mechanical design and capabilities of the lamination press, as well as precise control of the lamination cycle and process parameters. When all of these elements work together, manufacturers can achieve the consistency and reliability needed for today's advanced PCB designs.

Laufer provides many types of presses, including very modern, fully automated lamination press systems. What is their most recent press technology? Laufer's RMV series of lamination presses has



been a staple in PCB lamination for many years and has undergone continuous development since its initial introduction. The RMV is a highly flexible platform that accommodates varying levels of automation and is suitable for different product and quality requirements. It is used specifically in highly demanding production processes such as HDI.

With the growth of ELIC for HDI boards, the multiple lamination cycles—sometimes four or more—create an extra challenge for all the normal lamination defects that can arise, especially registration. What might be some lamination or stackup strategies for optimizing registration with ELIC boards?

In the U.S., registration control has become one of the bigger challenges for PCB manufacturers, especially as designs move toward higher layer counts and more advanced HDI structures. To improve registration performance, the industry has adopted technologies such as X-ray drill-optimization systems, a broader shift toward pinless lamination over traditional pin lamination methods, and the use of lamination aids such as release films and press pads.

At the same time, lamination engineers are continually challenged to predict how laminates and prepreg materials will move during the lamination process. Understanding material movement is critical because many of today's advanced and low loss materials tend to exhibit more expansion, shrinkage, and skewing compared to traditional FR-4 materials.

This is where process knowledge and data collection become extremely important. The combination of understanding the product structure, monitoring material behavior, and collecting process data during lamination is essential to developing a stable, repeatable, and successful manufacturing process.

Different material behaviors and CTE mismatch or excessive Z-axis expansion are other challenges PCB fabricators face with advanced and HDI

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stackups. What type of on-the-ground customer care do suppliers, such as Laufer, provide their customers? What does that partnership look like when dealing with high-tech builds?

Understanding material behavior and flow characteristics in lamination is extremely important. A key factor is understanding the temperature profile throughout the product stack during the lamination cycle. While monitoring temperatures is not new, traditionally, it has required manual measurements and operator involvement within the press system.

Laufer has fully automated this process, eliminating the need for manual operations between lay-up and de-stacking. It allows manufacturers to capture a much larger amount of process data throughout the entire lamination cycle. The benefit is not only improved traceability and documentation for every product produced, but also the ability to better understand material behavior, resin flow, and copper distribution early in the product design phase.

In addition, Laufer's control systems use real-time process data, allowing lamination cycles to be dynamically optimized for improved consistency, efficiency, and overall process control.

Does cleanliness play into it significantly?

Yes, when producing complex PCB structures, maintaining process cleanliness and minimizing contamination during product handling and transport are

also important. Laufer's new transport solutions are gentler, faster, and significantly cleaner compared to conventional systems. These improvements help reduce handling-related contamination and ultimately contribute to better production yields and higher product reliability.

Ralph, what else would you like PCB fabricators to know about all4-PCB and Laufer as an equipment supplier-partner?

With the continued growth of the U.S. PCB market and the increasing number of lamination presses being installed in the field, we are investing in local spare parts inventory and expanding our service and support team. We understand that both of these are vital to providing the support our customers need when they need it.

In relation to our partnership with Laufer, we are excited to be working with such a technology-forward company focused on achieving continuous advancement in automation, process control, and the new technologies that will help manufacturers achieve higher quality, consistency, and overall production efficiency.

Lamination has always been an important factor in PCB fabrication quality and reliability, but in HDI, its importance is even greater. Ralph, thank you for your time.

Thank you, Marcy. I-CONNECT007

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PART 1



BY MICHAEL CARANO, GLOBAL ELECTRONICS ASSOCIATION

The electronics industry supply chain is moving very quickly with the explosion of AI servers, high-performance computing, ADAS, quantum computing, and 5G/6G. Signal integrity is under scrutiny in an entirely new role. With many factors influencing signal integrity, one area that contributes to signal distortion at high frequencies is the PCB's final finish layer deposits. Frequencies above 40 GHz are susceptible to such distortions, and

data transfer rates of 224 GB/s are driving changes in PCBs and IC substrates.

The insertion loss of a high-frequency PCB can decrease the usable signal levels of a system, whether in a receiver or a transmitter. Additional details on insertion loss can be found in a previously published paper.¹ Certainly, the particular conductors' loss and the conductors' attributes (surface roughness, surface profile, final finish topography, and

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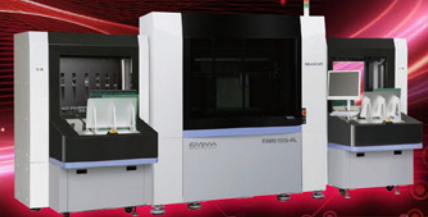
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particular metal) influence attenuation loss at higher frequencies. Metal finishes have different conductivity values as well and contribute to signal loss.²

A second concern for solderable finish circuits is the skin depth of the conductor. As frequency increases, skin depth decreases. This pushes the transmission more toward the surface of the circuit trace. Thus, the rougher the deposit and the varying conductivity of the metal itself, the more loss can be expected.

With the exception of silver, all other finishes, when plated over a copper conductor, will increase the loss compared to a copper conductor without the finish. This makes selecting nickel in the metal stack somewhat problematic for higher-frequency applications.

Alternative Finishes

As signal integrity becomes more critical at high frequencies, engineers are seeking final finishes that satisfy both electrical and assembly requirements, and several alternative finishes are now commercially available. Key considerations include:

- Lead-free assembly solderability
- Wire-bonding capability
- Reduced signal loss for product boards and advanced substrates

These needs are especially relevant in advanced packaging, where chips may be wire-bonded on one side of the substrate while solder balls are attached to the bottom side.

Over the past five to seven years, researchers have increasingly focused on final-finish metal stacks that eliminate electroless nickel, since nickel is significantly more lossy than silver or copper.

Except for silver, all other finishes listed in Table 1 will increase loss when plated over a copper conductor compared to a copper conductor without the finish. This makes the selection of nickel in the metal stack somewhat problematic.

Nickel's lower conductivity raises an important question for high-frequency design: Should solderable finishes such as Electroless Nickel-Immersion Gold (ENIG) or Electroless Nickel-Palladium-Immersion Gold (ENEPIG) still be used?

In practice, these finishes remain widely used because they offer proven benefits for demanding applications:

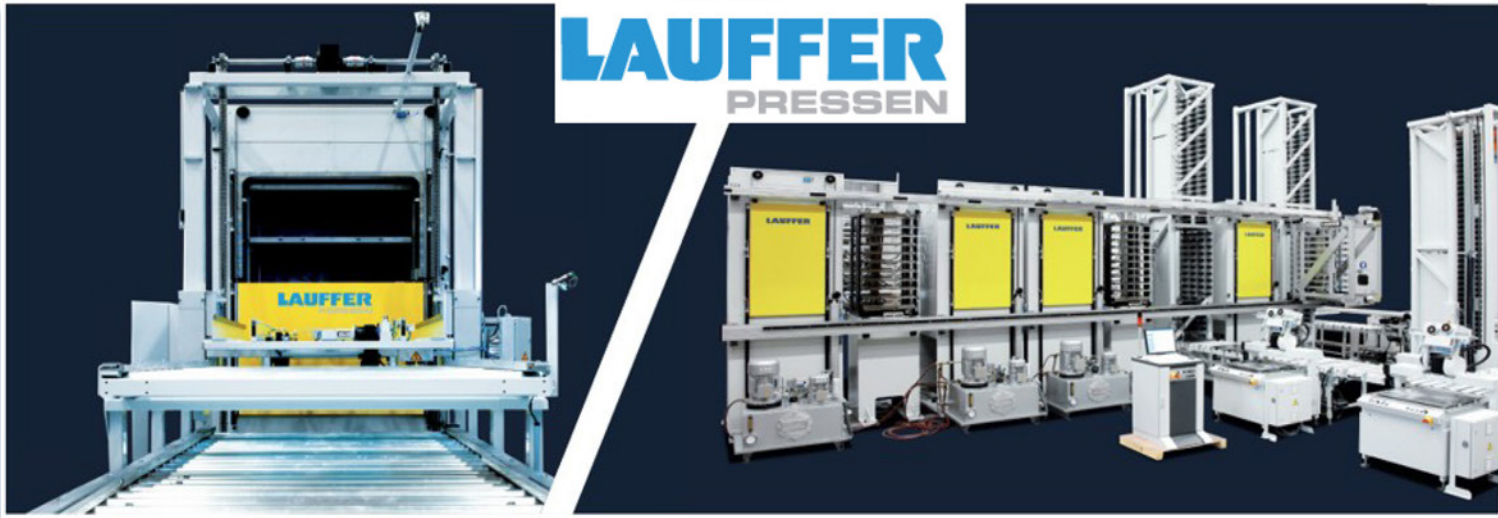
- They have a strong track record in advanced packaging
- They support the needs of high-reliability circuit designs
- They support wire bonding and solderability

Table 1: Approximate conductivity of metals

METAL	CONDUCTIVITY VALUE
Silver	$6.301 \times 10^7 \text{ S/m}$
Copper	$5.817 \times 10^7 \text{ S/m}$
Gold	$4.520 \times 10^7 \text{ S/m}$
Nickel	$1.500 \times 10^7 \text{ S/m}$
Tin	$0.870 \times 10^7 \text{ S/m}$

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Rather than eliminating nickel entirely from the solderable finish stack, a more practical alternative is to use a thinner electroless nickel deposit with a smoother topography.

Electroless Nickel-Immersion Gold (modified)

If one follows the IPC-4552 ENIG standard, the electroless nickel plating thickness is specified as 118.1–236.2 μin (3–6 microns).

There is a proven alternative to ENIG, with several commercially available final finish combinations designed to reduce signal loss. These include Direct Immersion Gold (DIG) over copper, Electroless Palladium-Autocatalytic Gold (EPAG), and Electroless Palladium-Immersion Gold (EPIG).

It's notable that these processes eliminate the nickel deposit from the stack. Electroless nickel is often considered a significant contributor to signal loss. Other considerations include the nickel thickness as required by IPC-4552 and the overall topography of the nickel deposit. However, the various processes described above have process complexity and cost issues.

So, simply eliminating the nickel deposit is not the answer. Nickel, plated from a specially formulated process, will provide a thinner deposit (which

is non-magnetic), a higher phosphorous content, and a near smooth topography. These three attributes improve conductivity and reduce skin effect signal loss due to the smooth topography. Figure 1 shows the comparison of the grain boundaries of the modified nickel formulation as compared to the conventional process. Note the roughness (often called cauliflower) of the conventional nickel.

As others have pointed out, nickel metal contributes to conductor signal loss due to its lower conductivity as compared to copper. However, the research hypothesis stated that if the nickel deposit morphology could be minimized and the magnetic effect eliminated, skin-effect signal loss at higher frequencies would be reduced.

A second hypothesis considered the overall plating thickness of the electroless nickel deposit. Previous experiments showed that a lower nickel thickness would improve the deposit's conductivity. Nickel plating uniformity across the circuit is also improved with a lower metal thickness. This adds further improvement in signal integrity,² and, in turn, reduces lossy characteristics to a manageable level.

Signal integrity testing showed that the modified electroless nickel deposit reduces signal attenuation loss. Figure 2 compares the signal loss of the

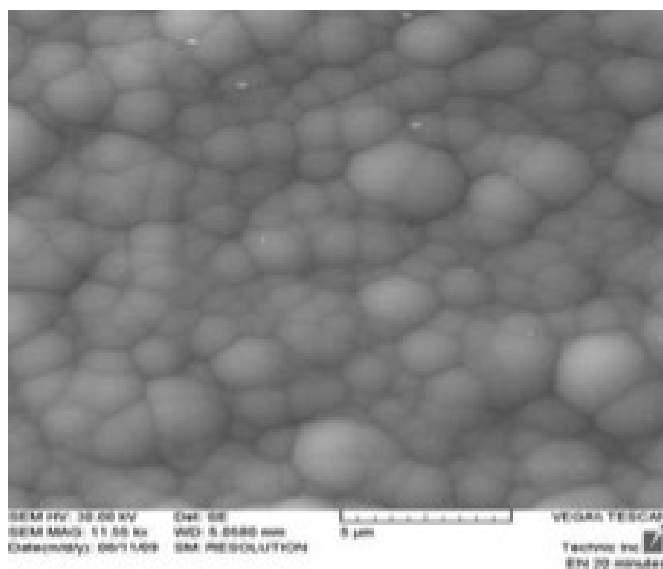
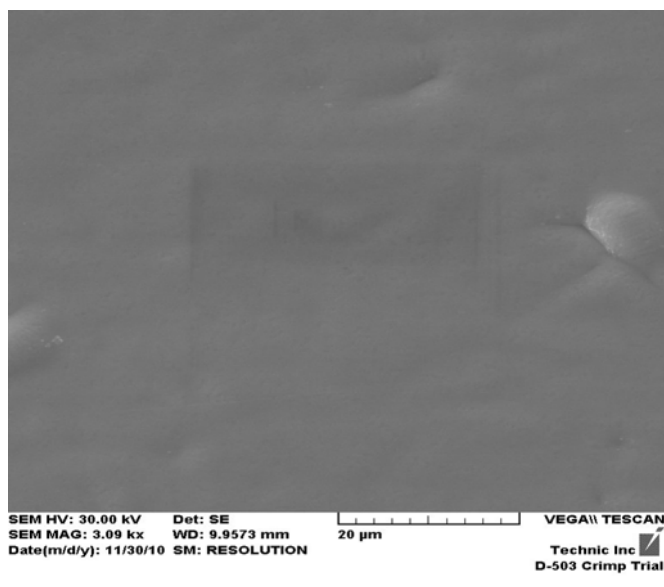


Figure 1: Smooth EN finish (left) vs. rougher topography EN, cauliflower (right).

Insertion Loss THP vs Typical EN

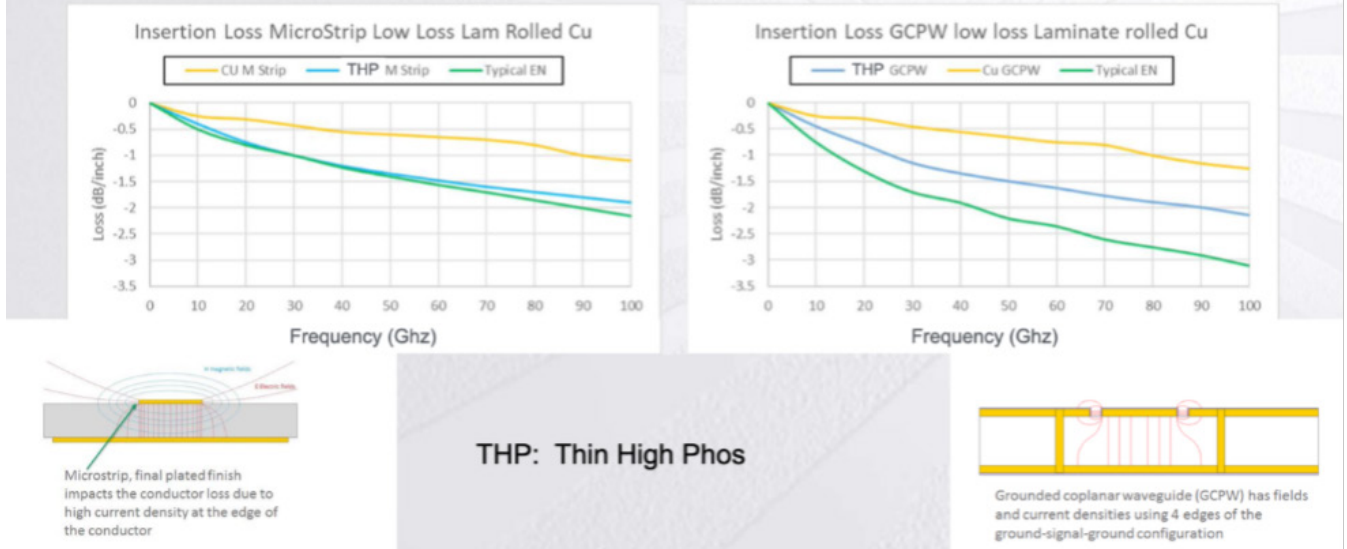


Figure 2: Insertion loss of thin high-phosphorous (modified) vs. conventional electroless nickel.

modified nickel deposit (THP) with that of conventional nickel and copper.

The modified ENIG (thinner deposit, smooth topography), while not as effective as immersion silver, nonetheless offers an alternative to conventional ENIG. This is due to the thinner nickel deposit, higher phosphorous content of the nickel deposit, and its non-magnetic properties. Another advantage is that the nickel deposit requires only 30–40 μ ins of plating thickness. That is much lower than conventional electroless nickel processes. The data compares insertion loss results on a microstrip test vehicle to a grounded coplanar waveguide (GCPW) designed test vehicle.

Summary

As AI and the Internet of Things (IoT) drive rapid technological change, processes and materials must keep pace. The electroless nickel-immersion gold process has served the industry well for many years, and a simple modification enables its continued use in higher-frequency applications. **I-CONNECT007**

In a future column, I will explore other final finish processes and materials for 40 GHz and beyond.

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Michael Carano brings over 40 years of electronics industry experience with special expertise in manufacturing, performance chemicals, metals, semiconductors, medical devices, and advanced packaging. To read past columns, [click here](#).

Part 2



Don't Buy AI, Learn It

A Fabricator's Guide to Getting Started

In Part 1, I covered common challenges encountered on a PCB shop floor, the missteps companies make when attempting to implement AI, and best practices to start that journey with a significantly higher likelihood of success. I identified six areas where AI's strength in aggregating data can make the shop floor run more smoothly, create better process documentation across departments and between shifts, and even help capture tribal knowledge. I also provided four prompts for you to experiment with in those areas, following a CRIT (context, role, interview, task) structure.

Hopefully, you're already more adept at using AI. Now, how do these new skills translate to your job and your organization?

What Does This Mean for the Whole Company?

If your people learn to use AI well, three things begin to happen: First, communication gets stron-

ger, customer questions get answered more clearly, internal summaries improve, and handoffs tighten up. Second, knowledge starts to move. A veteran engineer's rough explanation can become a cleaner draft. A quality manager's investigation structure can become teachable. Third, you begin building a capability that is hard to copy.

The practical payoff is better communication, cleaner first drafts, and faster comparisons, which reduce friction around quoting, handoffs, supplier communication, and investigations, which is usually where the first return shows up.

What Should I Do Now?

If you are wondering where to start, keep it simple. Pick one real task (not a demo) that already happens in your role every week. This could include document cleanup, comparison work, draft writing, handoffs, and investigation structure.

Then run this short checklist:



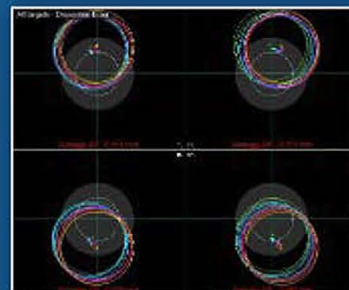
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- Choose a low-risk task with visible value
- Give the AI enough context to understand your situation
- Tell it what role to play
- Ask it to interview you before answering
- Ask for a specific output
- Review the result carefully
- Edit it like a professional
- Save the prompt if it was useful

The Invitation

If you followed my prompts in Part 1, I said you don't have to become an AI expert right now. Just be a regular user. Don't buy AI and assume the job is done. Learn AI so you can use it in real work. Use it humbly, visibly, and carefully.

Over the coming months, we'll talk about how to get better outputs, make AI part of your routine, use it in workflows that matter, and how shops begin turning their everyday use into something more durable. So, start simple and build capability.

Your Monthly Challenge: Start Small and Real

The following exercises are designed for Months 1–2: low-barrier, practical, and grounded in the kind of work PCB fabricators already do every day. The goal is to build your own capability. Good luck, and don't forget to have some fun with this.

Note: If an AI response touches IPC criteria, customer requirements, process parameters, chemistry limits, equipment settings, or accept/reject decisions, treat it as a draft for human review. AI is not the authority, so verify against your actual standards, specs, procedures, and shop knowledge before acting. I-CONNECT007



Sean Patterson is the founder of CrossGen AI. He previously served as COO & CTO at Summit Interconnect, held senior multisite roles at TTM Technologies, and was CRO of

Nano Dimension, a former Amazon executive and U.S. Navy Submarine Veteran.

Quick Win: Your First AI Conversation About PCB Fabrication

Time: 5 minutes

What to Do

Open your AI tool of choice and start with this prompt:

"I work in PCB fabrication. Explain, in simple terms, the basic steps of manufacturing a multilayer PCB, from incoming artwork to final electrical test. Then tell me which of those steps commonly creates the most scrap, delay, rework, or confusion in many shops. Be clear that this can vary a lot by product mix, equipment, and process control. Keep it practical, not theoretical. If you are unsure about anything shop-specific, say so instead of pretending there is one universal answer."

Ask one follow-up question tied to your own reality:

"In my shop, the step I worry about most is [fill in the blank]. Give me three reasons that step creates trouble and three questions I should ask my team this week."

What Success Looks Like

You finish with one saved conversation and at least one moment where you think, "That was useful," or "That is where this thing is weak." Both will count. Months 1 and 2 are about beginning the conversation and comparing AI's generic understanding to your fab's reality.

PROMPT 2

Practice: Multi-Turn Conversation Practice on Real Work

Time: 15–30 minutes

What to Do

This is one of the best exercises of Months 1–2 because it teaches the real skill: follow-up. Pick one real work scenario, summarizing a customer requirement package before quote review, drafting clarification questions for a new job, cleaning up a shift handoff, turning defect investigation notes into a cleaner summary, or comparing two supplier options.

Start with a prompt like this:

“I work in PCB fabrication, and I want to use you as a thought partner. Here is the situation: [paste notes or describe the task]. First, summarize what you think is going on. Then ask me one question at a time so we can improve the result before you draft anything final.”

During the conversation, force yourself to ask at least five follow-up questions, such as: “Why do you think that matters most? What assumptions are you making? What would change your recommendation? Give me an alternative interpretation. What important question have we not asked yet? Rewrite that for a shift supervisor, customer, or plant manager.”

What Success Looks Like

You save a 6+ turn conversation that is visibly better than the first answer. That is the lesson. In Months 1–2, you are not learning how to “prompt like a genius.” You are learning how to stay in the conversation until the output becomes useful.

Best for: Everyone

PROMPT 3

Stretch—Original Exercise: Build Your “Follow-Me” Shop Context Block

Time: 30+ minutes

What to Do

This one goes beyond the previous exercises and sets up the next stage of the journey. Write a short reusable context block about your plant and your role, keeping it to 150–250 words. Include your role, what your shop makes, typical technologies or product mix, your biggest operational constraints, the kind of decisions you personally make, and anything the AI should avoid assuming.

Then use that same block at the top of three different AI conversations this month. Here is a starter template:

I work at a PCB fabrication shop as a [role]. We primarily build [product types/customer mix]. Our operation includes [relevant process areas or capabilities]. The constraints that matter most in my work are [yield/lead time/customer specs/equipment uptime /documentation/material availability/staffing/certifications]. I am using AI to help me think, summarize, draft, and prepare questions, not to replace engineering judgment or shop procedures. If you make a technical claim about standards, process limits, or customer requirements, flag it for verification.

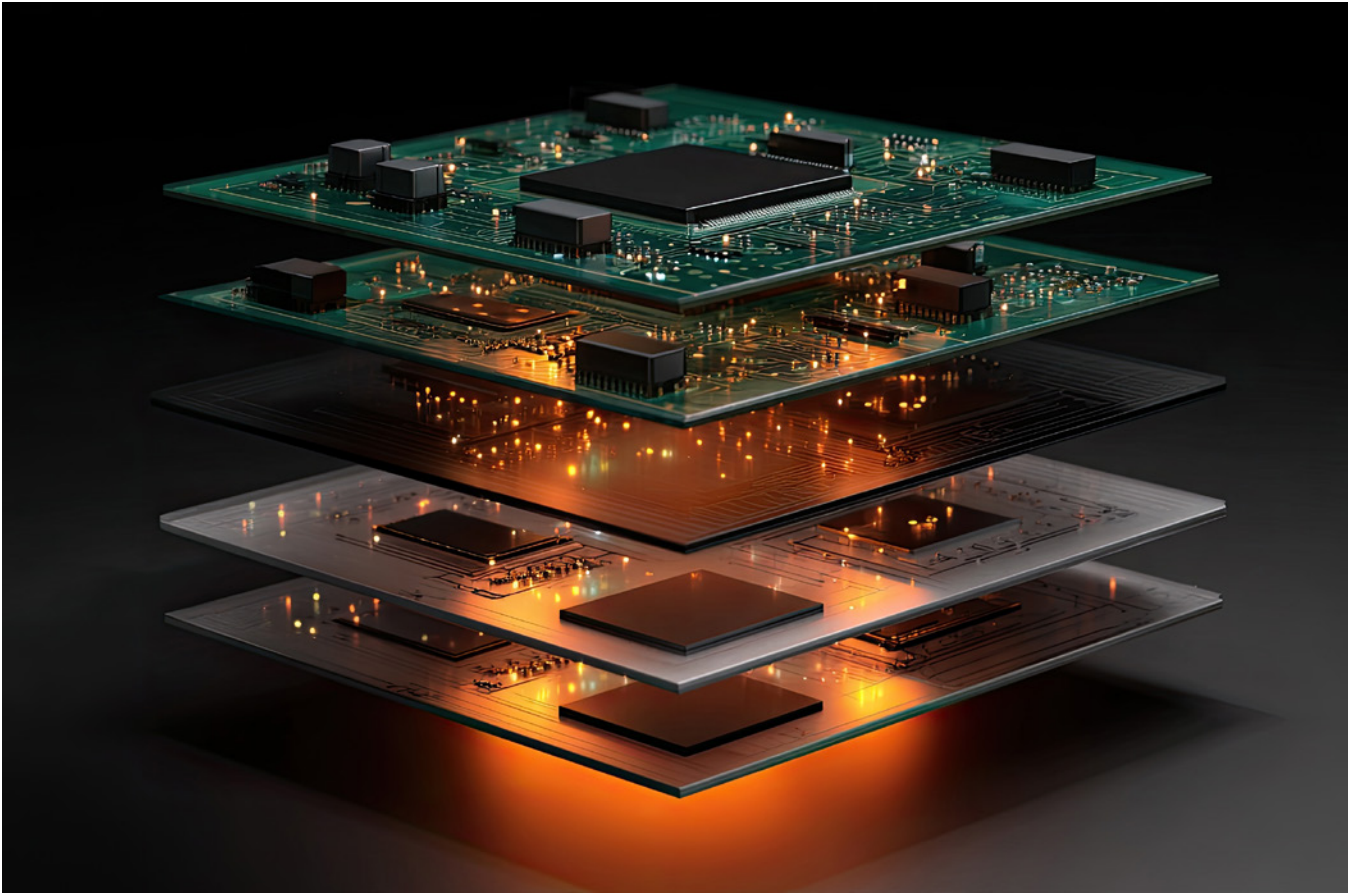
After using it three times, ask the AI:

Compare the quality of your answers with and without this context. What got better? What still needs human judgment?

What Success Looks Like

You create one reusable block that makes your AI conversations more relevant to your actual world. Just as important, you begin seeing that better inputs usually create better outputs. That will matter a lot in the months ahead.

Best for: Everyone, especially leaders who want to model a practical “follow me” approach for their team.



A CASE STUDY in Conquering High Aspect Ratio Features

As the demand for high-performance electronics is further driven by advances in AI and machine learning, the importance of high-aspect-ratio (HAR) through-holes in PCBs and IC substrates has become increasingly apparent. These vias play a vital role in enabling vertical interconnections in complex circuit architectures, especially within HDI structures, where maximizing space and enhancing electrical performance are crucial.

HAR through-holes help reduce signal path lengths and minimize parasitic inductance and capacitance. This is particularly essential for AI applications that demand high input/output (I/O) counts and low-latency communications across multilayer interconnects. Beyond their electrical advantages, HAR structures also contribute to

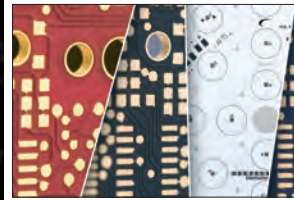
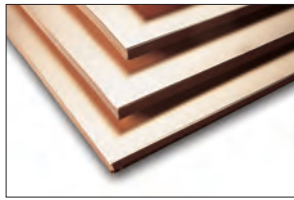
mechanical integrity, providing stability during thermal cycling, which is an important factor as substrates become more layered.

The increasing complexity of heterogeneous integration, which involves closely stacking logic, memory, and AI-specific systems-on-chip (SoCs), further drives the need for reliable vertical interconnect solutions. Technologies like 2.5D and 3D IC packaging rely heavily on precise HAR via structures for efficient signal routing within compact designs.

To examine the fabrication capabilities for HAR through-holes, this article evaluates a modular vertical electrolytic copper plating system developed by GreenSource Engineering (GSE), which merges features of both horizontal and

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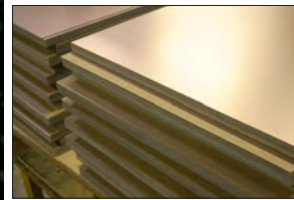


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Electro-deposited
Copper Foils



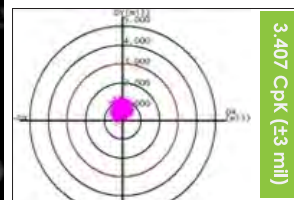
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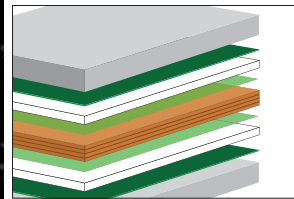
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vertical plating lines, offering flexibility and optimal process control.

This case study examines the throwing power (TP) results from recent sample plating at a customer facility employing GSE's modular vertical electrolytic copper plating tool. Included in the results are aspect ratios of between 16:1 and approximately 50:1, hole diameters of 0.1 mm, 0.2 mm, and 0.3 mm, and panel thicknesses of 3.2 mm, 3.8 mm, 4.5 mm, and 7.4 mm. The results are taken from pre-trials prior to plating the champion panel for the potential customer's internal evaluation.

Testing activities conducted on the customer's production plating line are significantly constrained by operational and process qualification limitations. The GSE team was unable to utilize the optimum plating parameters required for effective evaluation of the sample work panels because the line was operating under active production conditions. Since the process chemistry and operating windows had already been qualified for customer manufacturing, chemical concentrations, current density, and additive balance could not be adjusted to levels considered technically optimal for the trial work.

As a result, the testing was performed using production-approved settings rather than the preferred development parameters identified by the GSE team. This introduced substantial limitations in the ability to fully assess plating performance, process capability, and defect sensitivity under ideal operating conditions. Any deviation from the qualified process settings would have

Table 1: Pre-processing conditions for champion test panels

Panel ID	Panel Thickness (mm)	Via Diameter (mm)	A/R-1:	ASD	Bar	Mean TP (IPC)
RD1	7.4	0.1	49.5	1ASD	2	86%
RD2	7.4	0.2	37	1ASD	2	88%
RD3	7.4	0.2	29.8	1ASD	2	96%
RD4	7.4	0.3	24.7	1ASD	2	97%
A1	3.2	0.2	16	2ASD	2	140%
A2	3.2	0.2	16	2ASD	2	127%
A3	3.2	0.2	16	2ASD	2	125%
A4	3.2	0.2	16	2ASD	2	127%
A5	3.8	0.2	16	2ASD	2	91%
A6	4.5	0.2	22.5	2ASD	2	89%

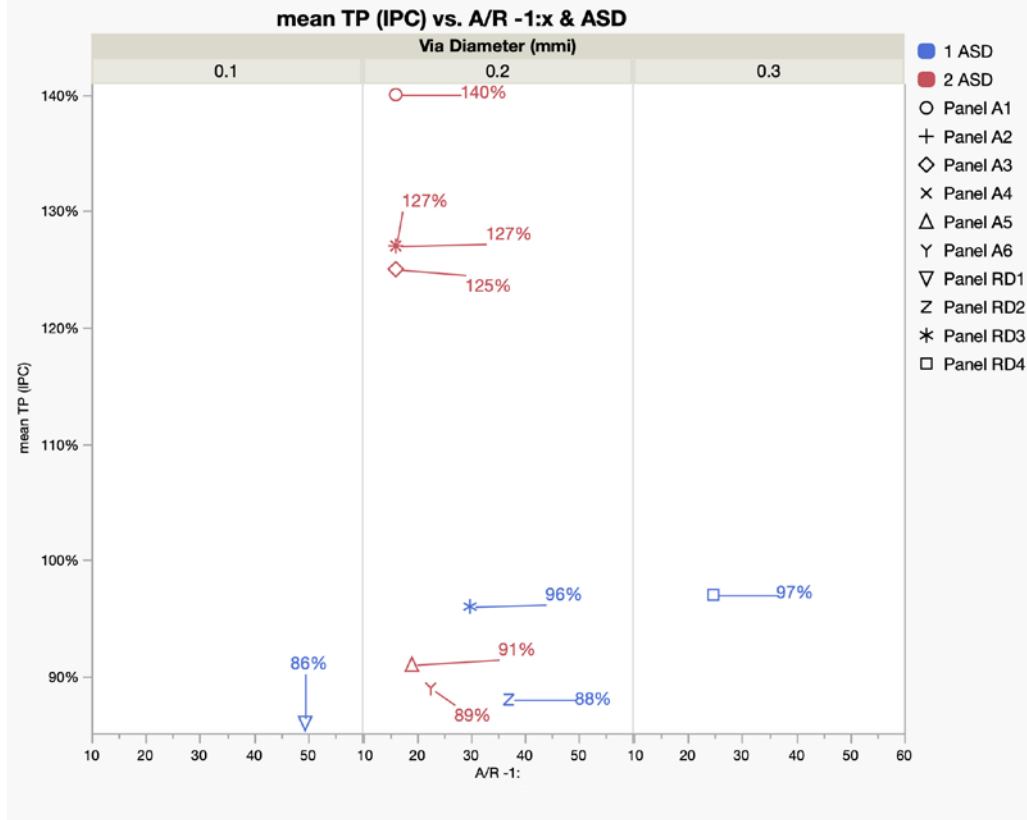
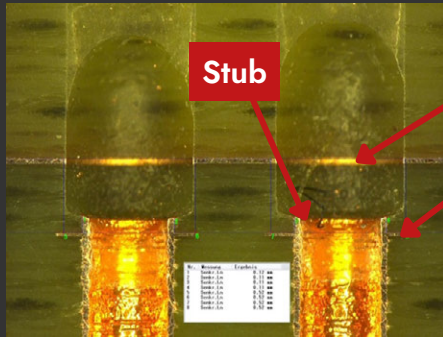


Figure 1: The mean throwing power results from the sample.

EAGLE EXY

HIGH-END EQUIPMENT FOR **BACKDRILLING**
AND **DEPTH DRILLING** APPLICATIONS

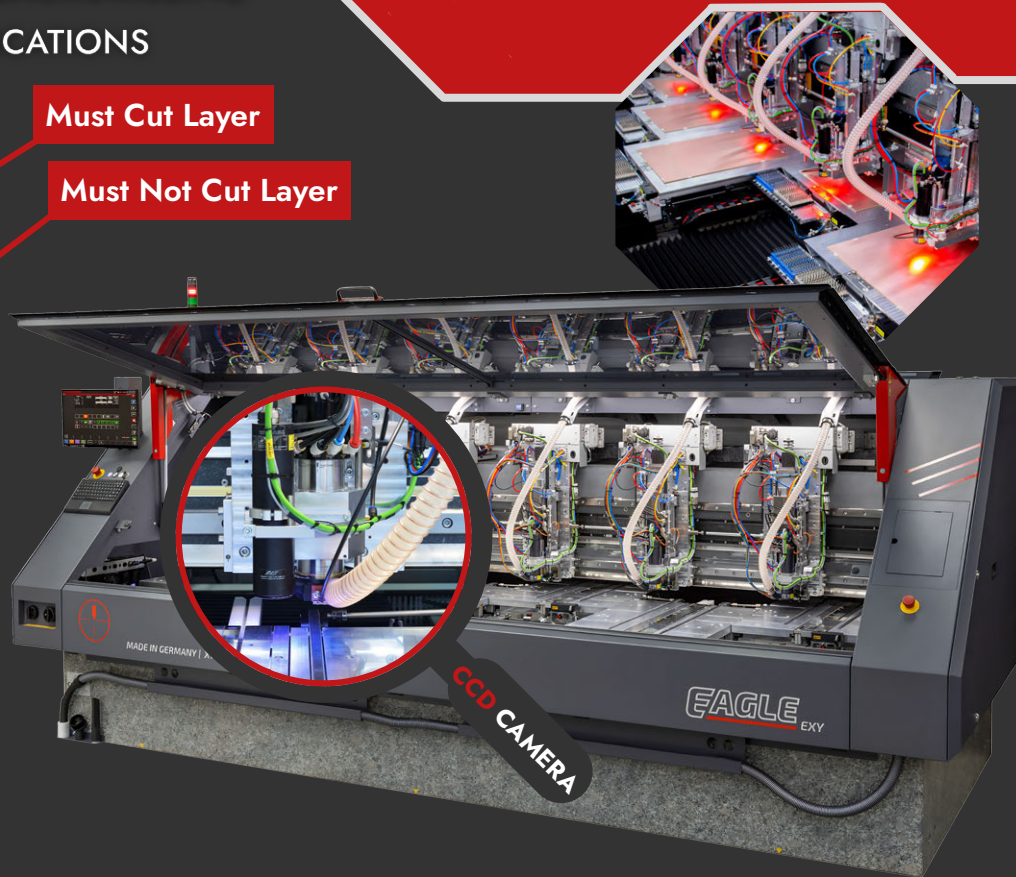


Back Drilling: stop of depth drilled hole before must-not cut layer within stub length tolerance

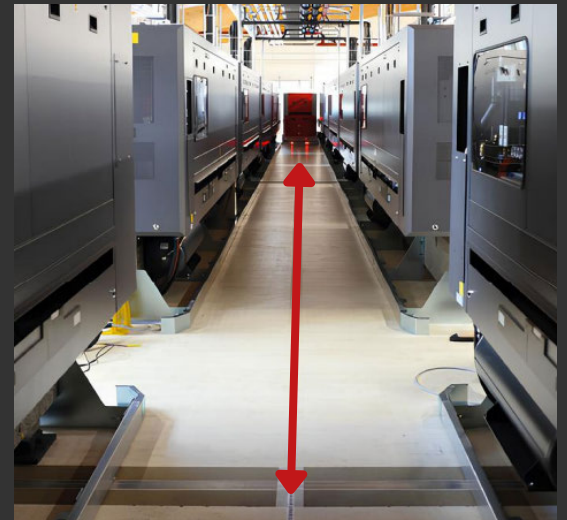


Depth Drilling: precise and reliable drilling to defined inner layers, enabling high-quality blind vias.

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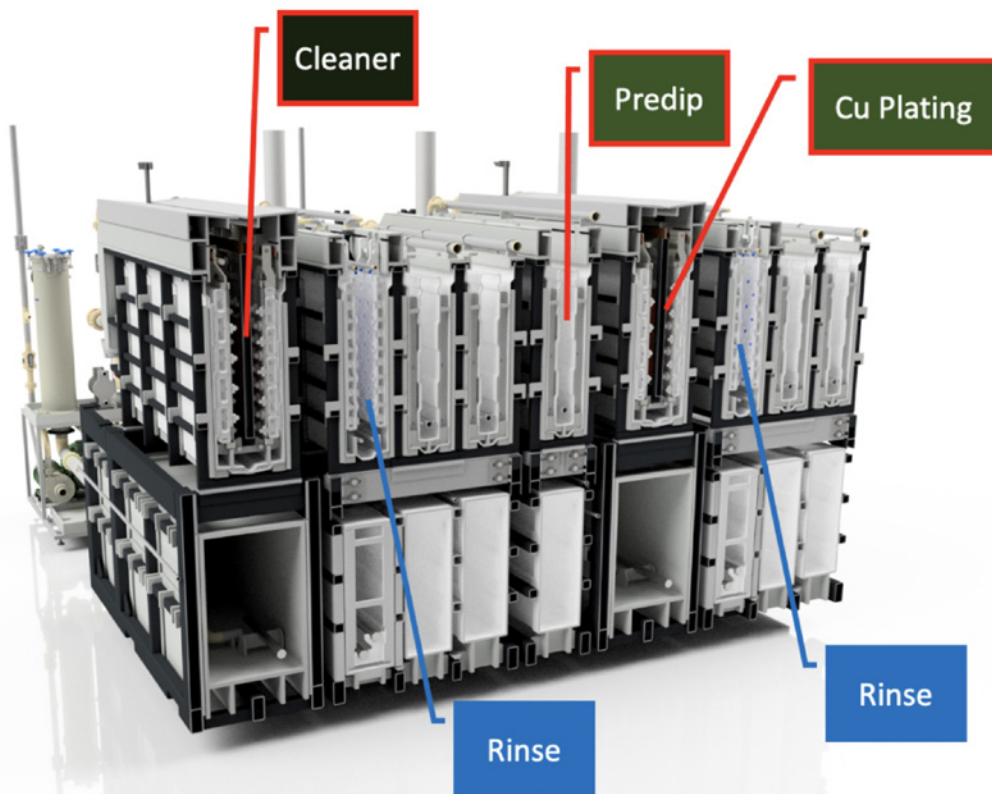


Figure 2: A cross-section of the test/R&D tool being honed to perfect an already robust equipment solution for HAR production.

TP, the mean values were well over 100% at the lower ARs and approached 90% across all features.

Overall, the outcomes indicate a strong robustness in the plating process. The findings showed that exceptional TP values could be achieved.

In conclusion, this study effectively demonstrates the potential for superior throwing power performance using this system, indicating that effective metallization of HAR through-holes is achievable even at higher current densities.

The unique design of the

created unacceptable risk to production material and potentially triggered requalification requirements, making parameter optimization impractical within the customer environment.

It is noteworthy that in this case study, only a very limited amount of testing was conducted due to ongoing production pressure and limited machine availability. Trial opportunities were confined to short production gaps, preventing the execution of statistically meaningful test runs or iterative parameter adjustments. Consequently, the overall evaluation scope was limited, and the ability to generate comprehensive process validation data was significantly reduced.

The TP evaluation was carried out using assessments that adhered to IPC-TM-650 standards.

Despite the limited evaluation scope, the study's results revealed several key insights. Although only three main variables were considered, the examination of TP across multiple microsections revealed an important finding: Higher aspect ratios require careful control of current density to ensure adequate plating quality. The results showed that while increasing the aspect ratio tended to decrease

plating tool, which is compatible with GSE's closed-loop water recycling system, enhances sustainability while meeting the demands of modern production.

To further optimize performance, the study's authors recommend refining both chemical parameters and physical settings to enhance throwing power. These results demonstrate the importance of advanced equipment and precise process control as the industry pushes the limits of high-performance electronics, particularly in AI and HDI technology.

To test using controlled, symmetrically constructed DOEs, GSE is working on setting up a pilot line for customer use going forward. **I-CONNECT007**

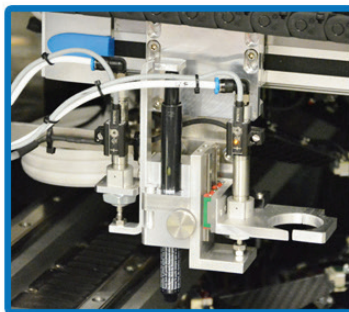


Richard Nichols is technical marketing director at GreenSource Engineering.

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PCBs in the National Spotlight



BY SHANE WHITESIDE, PCBAA

After decades of being overshadowed by the semiconductor industry, PCBs are now in the spotlight. Legislators, policymakers, and the media are paying attention, and the Printed Circuit Board Association of America (PCBAA) and our growing list of member companies have helped make it happen.

Legislation

In May, through PCBAA-led efforts, Sens. Ruben Gallego (D-AZ) and Jim Justice (R-WV) introduced S.4569, the Protecting Circuit Boards and Substrates Act, to incentivize domestic manufacturing of PCBs. The bill provides a 25% tax credit for the purchase or acquisition of American-made PCBs. This bill is a companion to H.R. 3597, the Protecting Circuit Boards and Substrates Act, which also pro-

vides for a tax credit and a \$3 billion grant program to support American PCB manufacturers.

Media Attention

The news media has discovered the critical role PCBs play in the technology stack in electronic devices powering everything from Apple devices to AI data centers. Reuters and Fox Business ran stories on PCBs in May, highlighting our reliance on foreign sources and how long, fragile supply chains can disrupt American manufacturing.

Also in May, CNBC produced a documentary and filmed a TTM PCB facility in Santa Ana. The story includes interviews with TTM and Sanmina executives, PCBAA's executive director, past and present Pentagon officials, a Harvard Business School professor, and other subject matter experts.

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This resulted in a 15-minute broadcast segment and online story seen around the world and, most importantly, in Washington.

Membership

PCBAA started out with five members five years ago. The association is now approaching 100 members, has achieved solid recognition in Washington D.C., and has a strong social media following. Our members will gather in Washington, D.C., June 16-18, for the fifth PCBAA annual meeting. A record number of attendees will hear an impressive lineup of speakers from Congress, the Pentagon, aerospace and defense companies, the Commerce Department, and engage in networking and discussions about the PCB industry. Attendees will also spend a day on Capitol Hill meeting with legislators and their staff to

educate, advocate and champion legislation that will help reshore and restore our industry.

Next month, I will report on what we heard from speakers at the Annual Meeting, as well as the challenges and opportunities we see for the second half of the year. If you are in the PCB industry and not yet a member, sign up today, and help us reshore and restore the American PCB industry. **I-CONNECT007**



Shane Whiteside is president and CEO of Summit Interconnect and current chair of the Printed Circuit Board Association of America. To read past columns, [click here](#).

The European PCB and Electronics Industries Score a Major Win in Chips 2.0 Milestone

BY MARCY LARONT, I-CONNECT007

Anyone in the PCB industry knows the frustration: Electronics policy discussions often begin and end with semiconductors. Yet chips don't function in a vacuum, and policymakers are increasingly recognizing that reality. For years, the PCB industry has argued that electronics manufacturing is about far more than chips alone. Now, the European Union appears to be listening. In a milestone development for the electronics ecosystem, the EU's proposed Chips Act 2.0 expands its focus beyond semiconductors to include electronics manufacturing, explicitly naming PCBs, PCB integration, IC substrates, advanced packaging, and system integration as strategic technologies.

Following a recent announcement in Brussels, I visited with Alison James, senior director of government relations in Europe for the Global Electronics Association, to discuss what this achievement means, why it matters, and how years of advocacy have helped elevate PCB manufacturing from an overlooked supply-chain component to a recognized pillar of Europe's industrial and defense strategy.

***Marcy LaRont:** Alison, tell me more about the EU's announcement on the Chips Act 2.0. Why is it important to the electronics industry?*

Alison James: The announcement was that the new Chips Act 2.0 takes a broader ecosystem approach beyond semiconductors, which is something we've been advocating for. Under the First of a Kind provision that enables Member States to support production capacity, the legislation now includes electronics manufacturing. That explicitly includes PCB manufacturing and integration, IC substrates, advanced packaging, and system integration.

Having PCBs explicitly named in major legislation is a significant development.

It is. PCB manufacturing and integration are specifically included in the European Chips Act, and that represents an important recognition of the role the broader electronics ecosystem plays in technology and industrial competitiveness.

[Read the rest of the interview here.](#)



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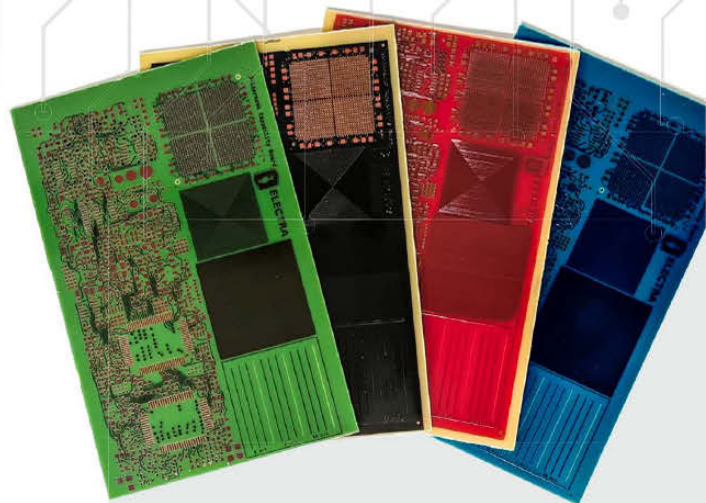
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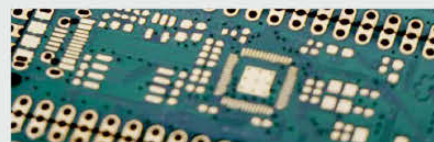
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Northrop Grumman to Demonstrate Space-Based Interceptor Capabilities with Apex for U.S. Space Force ►

Northrop Grumman Corporation announced one of its industry collaborators, Apex, will support Northrop Grumman's leading role in the Nation's historic drive to make space-based interceptors (SBI) a reality by the end of the decade. As part of the service's competition to demonstrate space-based missile defense and field a network of SBIs to protect the homeland soon after, Northrop Grumman is driving a culture of success with first-of-a-kind missile defense systems to build a new layer of homeland defense with an agile, nation-spanning workforce and industry partners including Apex.

Indium, Ames National Laboratory Team Up to Establish U.S. Gallium Supply Chain ►

Indium Corporation® and Ames National Laboratory have announced a research and development partnership to expand U.S. production of gallium, a critical material used in semiconductors and electronics, including smartphones, LED lighting, and optoelectronics. The new alliance will focus on developing the technologies needed to establish a domestic supply chain for an element that currently relies almost exclusively on imported sources.

MDA Space Tapped for U.S. MEO Epoch 2 Constellation ►

MDA Space Ltd., a leading provider of advanced technology and services to the rapidly expanding global space industry, has been selected by BAE Systems, Inc. as part of the U.S. Space Systems Command (SSC) MEO EPOCH 2 Constellation program. A key component of the U.S. multi-orbit missile defence architecture, Epoch 2 is focused on warning and tracking of advanced ballistic and hypersonic weapons.

How to Classify Your Product: Is It Defence, Dual-Use, or Civil? ►

Sooner or later, every company operating within technology, electronics, aerospace, drones, telecommunications, software, or defence-related manufacturing will face a question that sounds

simple, yet it is often difficult to answer: Is your product defence, dual-use, or civil?

RTX's Collins Aerospace Opens Expanded Manufacturing Facility in Tąęcina, Poland ►

Collins Aerospace, an RTX business, has opened its newly expanded, 22,000 square-meter manufacturing facility in Tąęcina, Poland. The \$69 million expansion will support an increase in landing gear system production capacity by nearly 25% for both commercial and defense aircraft programs. The site will create approximately 190 new jobs this year.

Boeing Validates MQ-28 Stealth Performance ►

Boeing has validated another advanced capability for the MQ-28 collaborative combat aircraft, which gives customers a decisive edge in combat: stealth performance. The MQ-28 Ghost Bat is designed to complement existing crewed aircraft by performing a variety of roles, including surveillance, electronic warfare, and force multiplication, all while maintaining a low radar profile.

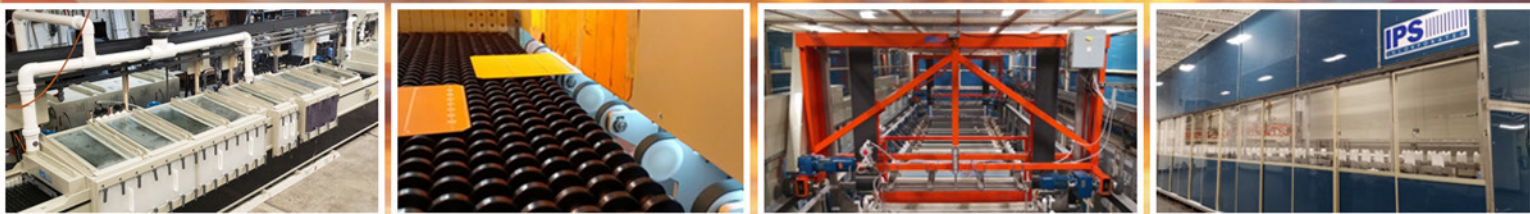
Lockheed Martin Delivers First Integrated Combat System Baseline for the U.S. Navy ►

Lockheed Martin has successfully delivered the first Integrated Combat System (ICS)-enabled baseline to the U.S. Navy. ICS-enabled baselines combine heritage combat system capability with modern infrastructure, driving rapid proliferation of capability through a singular development effort at scale.

Mission-Critical Timing Authority Safran Federal Systems Marks Milestone SecureSync Delivery ►

Safran Federal Systems, a trusted DoD mission partner and industry leader in Assured Positioning, Navigation, and Timing (A-PNT), together with Safran Electronics and Defense, announced the delivery of its 50,000th SecureSync™ time synchronization system, a milestone that reflects the platform's reliable track record. For over 50 years, precision timing has been at the core of Safran's mission. With more than 50,000 SecureSync units delivered globally across civil and defense networks, SecureSync is one of the most widely deployed precision timing systems in the market.

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EPTAC

The 'Ivy League' of High-tech Training

It's been an exciting time for EPTAC, an IPC training and certification center based in Salem, New Hampshire, which recently opened a new state-of-the-art training facility to much fanfare. To help celebrate this accomplishment, we spoke with some key individuals who tell the story of what truly makes EPTAC successful.

For over 35 years, EPTAC has built a reputation as a leading provider of IPC training and certification for the electronics manufacturing industry. It began in 1987 as a focused effort to deliver hands-on solder training and process expertise, and has evolved into a broad network of 24 training centers serving companies across North America.

What may surprise many is that EPTAC also offers professional services to manufacturers, including on-the-floor process audits and problem-solving. The opening of a new training facility in New Hampshire reflects the company's continued growth and ongoing investment in workforce development and high-reliability electronics education.

"We train the industry," said Jonathan Gilman, senior business development manager, who came to EPTAC nearly a year ago. He was a business owner and entrepreneur for over 30 years, during which time he did much of his own training. "That's one of the reasons this resonated with me."

He's impressed by EPTAC's "ridiculously high



Jonathan Gilman

standards. We are constantly looking for more people who meet our standards. We turn away more trainers than we accept. Our worst trainer rating is a 4.6 out of 5. To say we are the Ivy League of training excellence is not an overstatement.”

Gilman is obviously proud of his employer. “When someone comes in for training with us, it is important that they understand it is about more than the PowerPoint,” he said. “We have customers who come away from our training and say that they learned a lot about how to train, in addition to the course material that brought them in. That’s quite a compliment.”

He is primarily responsible for EPTAC Professional Services Group, a long-offered service that is now formalizing and expanding to meet the growing industry need. Solving “micro-problems” is a big value-add for manufacturers, he said, and broader than the standards to which they train and certify. “There is nothing we’ve said no to if it touches, at all, on IPC (standards).”

Helena Pasquito has been a trainer with EPTAC for 16 years but is a “legacy” in the industry. “I tell people I grew up in the industry, you know, back when dinosaurs roamed the Earth,” she said. “In the 1970s, there was a push in electronics. Things were changing by the minute. It was truly the place to be.” This was a time when electronics became big, not just for large companies and the government, but for everyone. Pasquito worked for Digital Equipment Corporation (DEC) while still in high school. “If you look at the archives of where the computer began, it was DEC and IBM.”

DEC helped Pasquito earn her electronics technician certification, and she’s cognizant that it was less common for women to earn degrees in electronics at that



Helena Pasquito

time. “DEC sent me to school as an 18-year-old, and I was pushing it forward,” she said. “The education that I got at the beginning was just incredible. Who would have thought I’d still be soldering eons later?”

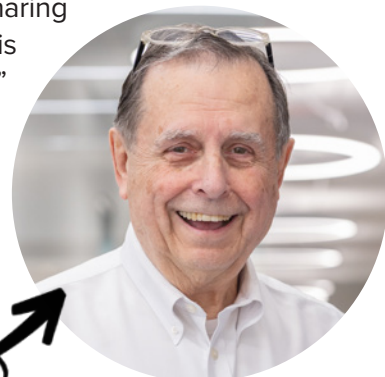
Her first turn at training came while working at MACOM Tyco, where she became an internal trainer and earned the Certified IPC Trainer (CIT) designation. MACOM touched all product classes, including aerospace and defense. “I was coming to EPTAC to get my certifications,” Pasquito said. “You could be working on the beginning of cell phone technology in the morning, and then you could be talking to NASA in the afternoon. Boeing was also a big partner for us, both aircraft and satellite systems. On the third floor, we had DARPA, all the secret military applications. We were also one of the first companies to have dancing robots—Spot. It was so varied, and it was such a cool business.”

MACOM sent her back to school for her second and third college degrees, in business and education, perhaps foreshadowing that training would become an even bigger part of her professional life.

After 16 years at EPTAC, the passion and enthusiasm have not diminished. “EPTAC is a great organization,” Pasquito said. “I love working here. We have grown leaps and bounds over my 16 years. We’re now, of course, in this beautiful space here in Salem, New Hampshire, with 14,000 square feet.” She teaches almost everything that EPTAC offers, and is excited about the new, large classrooms. I teach IPC-A-600 for bare PCBs, 6012 for rigid boards, A-620 for cable wire harness, J-STD-001 soldering requirements and A-610 for assemblies, which is still my favorite, and something I was training others in long before coming to EPTAC.”

Additionally, EPTAC does non-IPC training, custom training programs, and a five-day hand-soldering certificate, one of Pasquito’s favorites. “I’m still soldering my heart out and sharing my wisdom and love for this technology in the process,” she said.

Finally, I spoke with industry veteran and firecracker Leo Lambert. Though all EPTAC



Leo Lambert



trainers are superstars in their own right, Lambert brings it home with an abundance of passion and wise words for all. He's been with EPTAC since 1996 and is the face of the company, according to his colleagues. In fact, he may be the face of IPC standards and certification training in North America. He's also the author of "Learning with Leo," a popular *I-Connect007* column.

Lambert also started his career at DEC, getting involved in specifications when his boss asked him to attend some IPC committee meetings in his place. "Initially, the OEMs (chiefly DEC and IBM) wanted to get rid of their quality manuals, so it was decided to put all of that information into IPC specifications," he said. This first brought IPC manufacturing specifications into true prominence. "In 1994, the Department of Defense (DoD) under Secretary William Perry announced a shift from using exclusively military specifications to commercial," which upleveled the importance of IPC manufacturing specifications yet again.

In 1976, there were three big standards: IPC-J-STD-001, IPC-A-600, and IPC-A-610. Lambert said it was a lot easier to get consensus back then, with only 10–20 participants in a group meeting vs. more than 100 today. He's proud that, despite what may seem like constant change, the standards have held up well over time, and that 50 years later, he's still active in both creating new IPC standards and modifying existing ones.

Training is where it all began. "Industry volunteers wrote the first training program for IPC-A-600, folks like Dieter Bergman, Ralph Hersey, and me," Lambert said. "Training back in the day was an engineer doing a presentation or workshop, and someone saying, 'We need to do a training around that.' What started out as a workshop was broken down into steps to create a training

program, and if you presented the paper, you were on the hook. That's how it started."

While it seems that technology is accelerating at an unprecedented pace, Lambert offers grounded and wise counsel. "The technology is not changing as fast as people think," he said. "What's changing is the density; the methodology is the same at the core. We have two cultures that are coming head-to-head: the semiconductor business on one side and PCBs on the other. Will we need new tools? Will we need new (manufacturing) methods? How do we manage them coming together?"

No matter how it plays out, Lambert said it's essential to stay involved in the standards process. "You have to be involved in standards!" he said.

Training at EPTAC has been so effective and has allowed for tremendous growth for over 35 years because of its focus on how they teach and train, and on how they deliver the content to the audience in front of them to ensure they get what they need, Lambert said.

"People don't learn today the way they learned 30 years ago," he said of each new generation. "We always need to be taking a look at different (training) methodologies, and we need to talk to, not only the industry companies that make the products, but also the educators. This needs to happen in late grammar school to early high school."

Even all these years later, what he enjoys most about training is seeing that aha moment with his students, when they really understand the concepts. He ended our conversation with a big Leo Lambert smile, encouraging everyone, "Enjoy what you are doing. Keep studying. Keep learning and share your knowledge."

EPTAC and its dynamic and talented training team are certainly doing that. **I-CONNECT007**

EPTAC Celebrates

New Expansive Training Center in New Hampshire

BY MARCY LARONT, I-CONNECT007

On a picture-perfect spring day in Salem, New Hampshire, on April 23, EPTAC marked a major milestone with the opening of its new 14,000-square-foot training facility and headquarters on 7 Stiles Road. EPTAC welcomed state and local officials, industry partners, business leaders, and customers for a ribbon-cutting celebration that felt equal parts ceremonial and personal. Remarks from President and CEO Burak Gokmen, along with good food and easy conversation, set the tone for an event defined by both growth and gratitude.

With 24 training locations in the U.S. and Canada, the expansion underscores EPTAC's continued momentum and its sharpened focus on serving high-reliability sectors including defense, aerospace, and medical devices.

"This expansion strengthens our ability to deliver the hands-on training that today's manufacturers require," Gokmen said to the crowd of visitors. He emphasized the broader ecosystem behind workforce development and added that EPTAC will continue to deepen its "collaboration with industry, government, and education partners to help build a more resilient and highly skilled workforce."

As states compete for advanced manufacturing investment, that message resonated with policymakers as well. U.S. Sen. Jeanne Shaheen (D-N.H.) pointed to EPTAC's long-standing impact. "Today marks an important step forward for EPTAC as you continue to grow and innovate within the electronics

manufacturing industry," she said. "For more than 35 years, EPTAC has played a vital role in training and certifying professionals across critical sectors, helping to ensure quality, reliability, and advancement in fields ranging from medical technology to aerospace. Your decision to expand here in New Hampshire reflects the strength of our state's workforce and our shared commitment to fostering economic growth and innovation. I commend the entire EPTAC team for your dedication and vision.

Your investment in both your industry and our state's workforce will have lasting benefits for the region."

David Hernandez, vice president of education and workforce training at the Global Electronics Association, traveled to the event and echoed that sentiment. "EPTAC has a long and distinguished legacy of training for the electronics manufacturing industry," Hernandez said after the event.

"They are a critical partner to the Global Electronics Association in addressing workforce challenges and ensuring the industry has access to a skilled workforce. Congratulations to them on their new building and expansion, and our great appreciation goes out to them for all the essential training work they do."

The new facility features four large classrooms, two lecture halls, and two fully equipped training areas designed for hands-on instruction. Across all its sites, EPTAC offers a flexible mix of in-person, on-site, and online training, working closely with customers to tailor programs for maximum impact.



From left to right, David Hernandez of the Global Electronics Association with Burak Gokmen, EPTAC President and CEO.





Back to Basic Cupric Chloride Etching



BY DON BALL, CHEMCUT

This month's theme is every layer interconnect (ELIC) or every layer microvias (ELMV), a subject that, I must confess, I have little practical knowledge of. The process problems here are mostly related to registration during multiple lamination steps and how to minimize or correct any misalignment. I know this is very difficult, but I suspect that if you are already doing this or considering it, you've probably figured it out on your own.

So, when casting about for an alternative subject, it occurred to me that we have received several

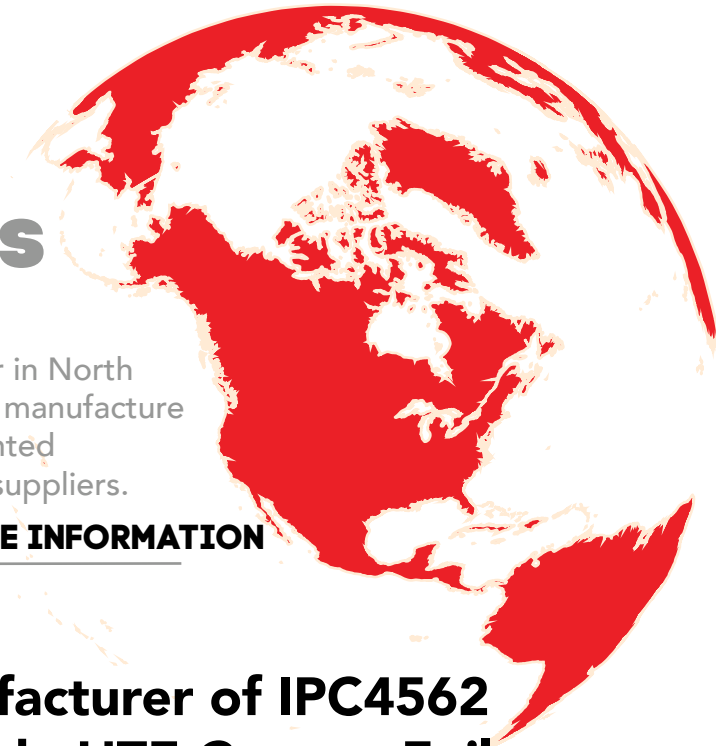
calls in the past few months from younger process people who have been thrust into more senior process positions as their older colleagues retire. They've realized they lack the practical knowledge their predecessors have accumulated over the years. They know what their various process parameters are, but not why those particular parameters were in place.

I thought that writing a Frequently Asked Questions (FAQ) column would be a good idea, where I could cover some of the simple practical process

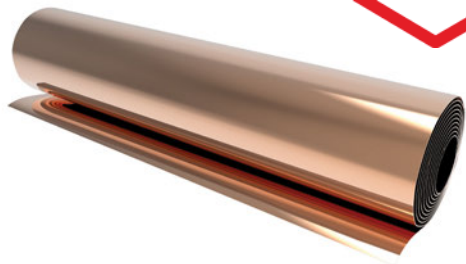
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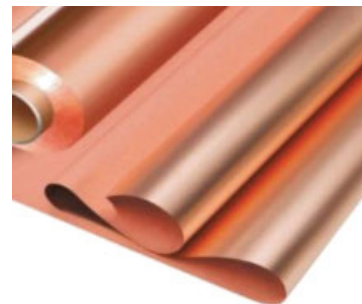


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questions that some of us lofty personages with decades of experience forget to put in our tutorials.

However, when I checked with our field service team and others in contact with customers, I found that the most frequently asked questions have been about cupric chloride etch chemistries. Therefore, I will cover the very basics of cupric chloride etching; not so much the technical facts but why we give the advice we do.



At the end of the day, there is no magic chemistry that eliminates the tradeoff between etch speed and etch quality.”

The Old Need for Speed

Back in the almost prehistoric days when I started in the industry, the mantra was speed, speed, speed. Get as many square feet through etching per hour as possible, because all those TVs, refrigerators, stereos, newfangled micro-computers, etc., needed circuit boards. State-of-the-art line and width spacings for circuit traces were 0.010" (10 mil or 254 μm) for densely packed circuits, and most of the production circuit designs were most likely double this. A sophisticated PCB would be double-sided with plated through-holes on 0.064" (1.65 mm) thick epoxy fiberglass laminate.

There were no such things as multilayers, other than a gleam in a PCB engineer's eye. Components (resistors, capacitors, etc.) were much larger than today (you could actually see a resistor with the naked eye), so a circuit board had to be quite large

to fit all the components. Hence, the need to cram as many panels per hour as possible through the etcher to meet the demand for boards. Nowadays, of course, with multilayer boards, chip-on-board, and many other miniaturization technologies, modern boards can be much, much smaller in area to accomplish the same tasks as early boards.

The need for raw etch speed has diminished since boards are now much smaller and multi-functional, and we don't need as many square feet per month to meet demand, even though extra square feet are needed for multilayer production. I have to admit, however, that I still hesitate to suggest or try new things that might improve etch quality at the expense of etch speed, so ingrained is the need for speed from my early career.

The Quality Factor

A major concern today is etch quality, which, in the case of using cupric chloride to etch copper circuit lines, means the rate of sideways etch to the rate of downward etch (etch factor) as the line is formed, or how straight we can make the sides of the circuit trace. Ideally, the sides of the trace would be straight up and down, but in reality, they are slanted, with the trace being wider at the bottom.

When the space between traces is 0.020" (500 μm), the shape of the sidewall doesn't matter, but when the space is 0.002" (50 μm) or less, as they tend to be these days, the shape of the sidewall is extremely important to avoid shorts and crosstalk. The main contributors to both etch speed and etch quality are the concentration of cupric chloride in the solution (specific gravity) and the amount of free acid (hydrochloric acid or HCl) in the mix.

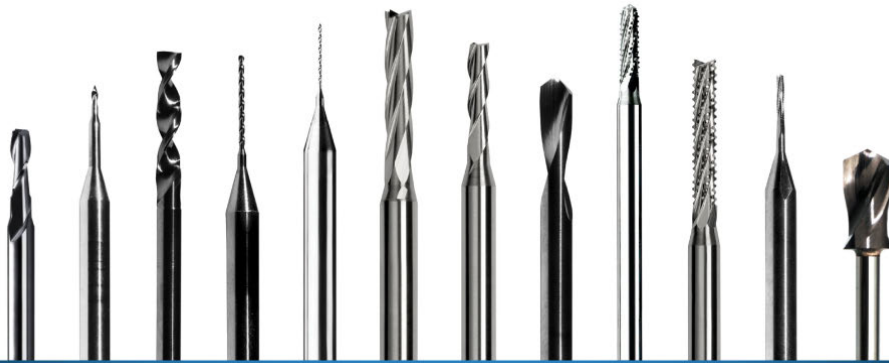
The best range of concentrations for cupric chloride etching copper is between 275 grams per liter (specific gravity at 1.2501 or 29°Be) and 370 gpl (sg at 1.3302 or 36°Be). We use specific gravity to define the concentration of cupric chloride as it is easier to measure and control. Degrees Beaume is an old French unit used since the 1600s to measure specific gravity, and it has somehow survived to describe the specific gravity of cupric chloride, ferric chloride, and alkaline etchants. So, the best range of specific gravity for cupric and etching copper is between 29 and 36°Be with 28°Be giving the fastest



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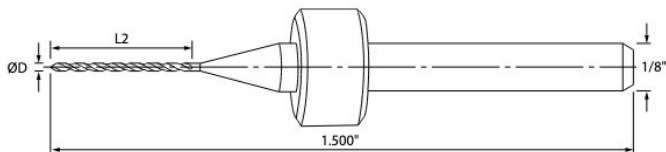


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4 Facet Point Geometry

REPOINTING will be a new service offered by Insulectro through Kyocera. The company has recently invested in automated, state-of-the-art equipment and all repointing will be done in Southern California.

etch rate downward, but also the fastest sideways etch. Running at an sg of 36°Be gives a slower etch rate but a much-reduced sideways etch.

Recommended free acid levels are between 1N and 3N where N is the normality of the acid in the cupric chloride solution and describes the concentration of the acid. A 1N solution is 36.5 gpl HCL. The free acid level is important for two reasons. One is to keep the cuprous chloride byproduct of the etch reaction in solution so an accurate reading of the ORP for regeneration can be made.

The second reason is that the free acid prevents the formation of oxides on the surface of the copper during etching. The etch rate would be halved without the free acid. Within the recommended range of free acid concentration, increasing the concentration gives faster downward etch rates but also faster sideways etch rates. The free acid level is important, and many smaller shops I have visited don't have the means to monitor it; they just estimate.

The equipment to measure it is not expensive, and it doesn't take a trained chemist to use it. I always recommend that a corner somewhere in the shop be cleared and a bench set up to measure free acid at least once a shift.

Running at the lowest recommended specific gravity and highest recommended free acid level will give the highest etch rate, at around 0.002"/min. (50 μ m) but a sideways-to-downwards etch ratio of about 1 to 1. Even in the old days this ratio was unacceptable. Running at the highest specific gravity and lowest free acid concentration drops the etch rate to about 0.001"/min (25 μ m), but the sideways-to-downward etch ratio improves to 1 to 4.

That etch rate was too slow for the old days, so a compromise was reached and the recommended specific gravity and free acid levels were stated as 32°Be and between 1N and 2N. This gave an etch rate of around 0.0015"/min. (38 μ m) at the higher acid concentration and an etch ratio of around 1 to 3 sideways to downward.

The 32°Be, 1N to 2N recommendation for cupric chloride operating parameters is what is recommended in most etching guides, but still favors etch speed over etch quality. I feel that nowadays

etch quality is at least as important, if not more so, than etch speed, so I run my cupric etcher at 36°Be specific gravity and 0.8N free acid and accept the lower etch rate in favor of the improved etch quality. This is what I recommend to those who ask. Higher specific gravities (40°Be is close to the saturation point) slow the etch rate without improving the etch ratio, while acid levels below 0.8N also slow the etch rate without improving etch ratios very much and, in addition, become harder to control.

In answer to the next anticipated question: Yes, alkaline etchant is reputed to have better etch ratios than cupric, and this is true if the etchant parameters are kept in the middle of the recommended range for pH, chloride concentration, and specific gravity. One can expect etch ratios of 1 to 4 and etch rates of around 0.0024"/min. (60 μ m).

By running at the lower end of the ranges for pH and chlorides and higher end for specific gravity you can get etch ratios of about 1 to 5 and a slower etch speed of 0.0018"/min (45 μ m). It should be noted, however, that etchant control gets very tricky at these settings.

At the end of the day, there is no magic chemistry that eliminates the tradeoff between etch speed and etch quality. The old mindset of "faster is better" worked well when circuit traces were large and throughput was everything. Today, with much finer features and tighter tolerances, quality deserves equal consideration.

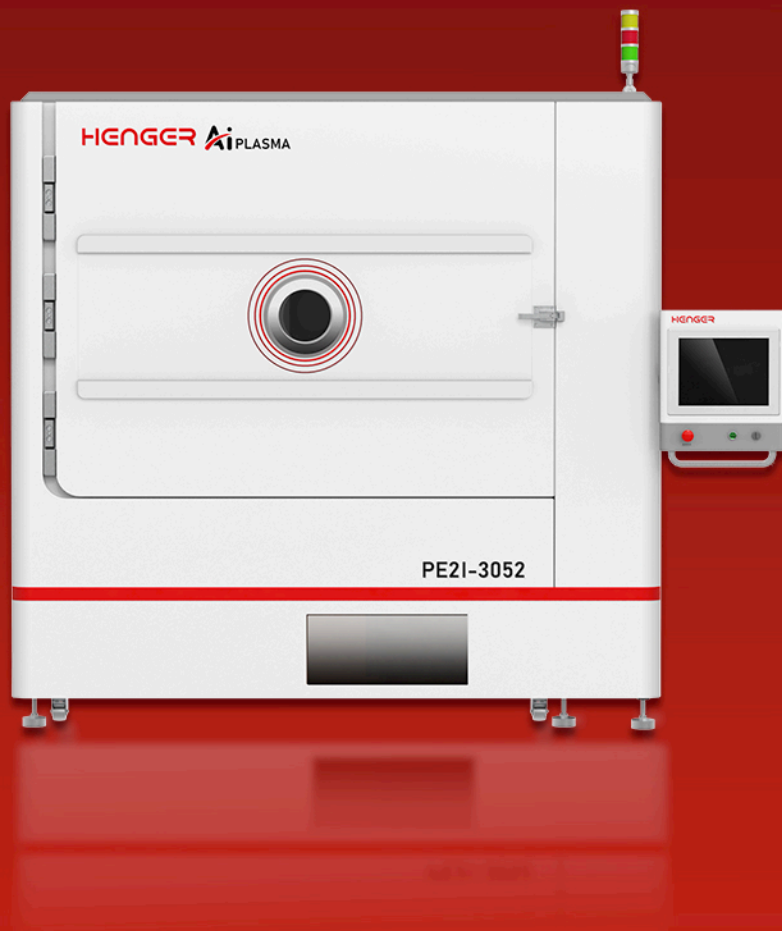
Careful control of specific gravity and free acid levels is not simply housekeeping; it directly affects the balance between productivity and circuit quality. Perhaps that is the real lesson from revisiting these older chemistries. Even with all the advances in PCB technology, the fundamentals still matter, probably more now than ever. **I-CONNECT007**



Don Ball is a process engineer at Chemcut. To read past columns or contact Ball, [click here](#).

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Material	Aspect Ratio	Avg. Desmear (μm)	TP Yield (%)
EM-892K (M8)	32:1	9.36 - 10.56	85 - 90
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Signal Integrity *Without Borders*

BY KELLY DACK, CIT CID+

I started my PCB design career in 1980, long before “signal integrity” became a formal discipline. Back then, we were trying to “connect the dots” on simple, two-sided PCB layouts using the new \$80,000 interactive graphics terminals we called a CAD system. By the time PCB design conferences emerged in the 1990s, signal integrity had begun to formalize into a discipline of its own.

Much of the early, visible thought leadership came from North America and parts of Europe. These were engineers who not only developed the fundamentals but also did the hard work of translating Maxwell’s equations into something the rest of us could apply without losing our minds. But signal integrity has never been geographically constrained.

Before going any further, I’m adding another North American master to those to whom our industry owes a considerable debt of gratitude: Dr. Todd Hubing. He is an American electrical engineer, educator, and consultant specializing in EMC. He is professor emeritus of electrical and computer engineering at Clemson University and president of LearnEMC, an organization dedicated to EMC education and electronic-system design support. Hubing is widely respected for advancing both the understanding and teaching of EMC principles in vehicular and electronic systems.

What sets Hubing apart is his ability to translate complex electromagnetic theory into practical engineering methods for PCB layout, grounding, shielding, filtering, return-current control, and EMC troubleshooting. His teaching philosophy emphasizes under-

standing current paths and field coupling rather than blindly following “design rules,” an approach that consistently shines through in his courses, publications, and industry presentations.

Zooming Out the Map

Last month, my column highlighted a dozen masters of signal integrity, most of whom reside in North America. Yet the global signal integrity community has been advancing high-speed design, power integrity, packaging, electromagnetic modeling, and measurement science for decades, often through conferences, universities, and publications less visible to North American audiences. The result has been a quieter parallel track of innovation that now underpins much of today’s AI hardware, hyperscale computing, and high-speed electronic systems.

Before AI completely takes over the world, I would like to pause that silence and continue acknowledging the many researchers, educators, and practitioners around the globe whose work has shaped our collective understanding of signal integrity. Their contributions—spanning PCB design, interconnect modeling, EMC, packaging, materials, simulation, and measurement—form much of the foundation upon which modern AI infrastructure now depends.

So, please join me in recognizing signal integrity pioneers from Europe, Asia, the Middle East, Australia, and beyond who have advanced our science. Several of them have trained generations of engineers, published seminal research, developed widely used methodologies, and influenced the tools and systems we now take for



Dr. Todd Hubing

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International Signal Integrity Pioneers

Japan: Dr. Kenichi Okada of the Tokyo Institute of Technology leads in RF and high-speed IC design, with work at the chip-to-package boundary in 5G and emerging 6G systems. Dr. Masayuki Fujita of the University of Tokyo has advanced EDA and system-level modeling, enabling earlier and more scalable signal-integrity-aware design.

Belgium: Dr. Eric Beyne of imec is a leading researcher whose work in 3D integration, chiplets, and advanced interconnects has shaped system-level signal integrity and modern high-speed system architecture through system-technology co-optimization of signal, power, and thermal effects.

Italy: Dr. Giovanni Ghione of Politecnico di Torino links device physics to system-level signal behavior in high-frequency systems.

Germany: Dr. Janusz Grzyb of Fraunhofer IAF works at terahertz and millimeter-wave frequencies, where SI becomes a fully electromagnetic problem.

Taiwan: Ruey-Beei Wu is a professor at National Taiwan University in Taipei, recog-



Dr. Kenichi Okada



Dr. Masayuki Fujita



Dr. Eric Beyne



Dr. Giovanni Ghione



Dr. Janusz Grzyb

nized for his contributions to SI, PI, and electromagnetic modeling of high-speed interconnects. His work is frequently published and cited in IEEE journals and conferences. He is also known for collaborating with industry and mentoring engineers in advanced SI/PI design methodologies.



Ruey-Beei Wu

Australia: Christophe Fumeaux is a professor at the University of Queensland, who has contributed to electromagnetics, antennas, and high-frequency modeling relevant to SI. He has published extensively in IEEE journals and conferences and is an IEEE Fellow. His research bridges theory and practical design, influencing RF systems, antennas, and high-speed electronic applications.



Christophe Fumeaux

Barry Olney is an Australian PCB design engineer, educator, and technical columnist best known for his long-running “Beyond Design” column at Design007. He is the managing director of In-Circuit Design Pty Ltd (iCD), a company specializing in high-speed PCB design, signal integrity simulation, stackup planning, and power distribution network (PDN) analysis software. Within the electronics industry, Olney is frequently regarded as a master of signal integrity because of his decades-long focus on high-speed digital behavior, impedance control, EMI/EMC mitigation, crosstalk, PDN analysis, and electromagnetic field behavior in multilayer PCBs. His writings consistently bridge theory and practical PCB implementation for working engineers.

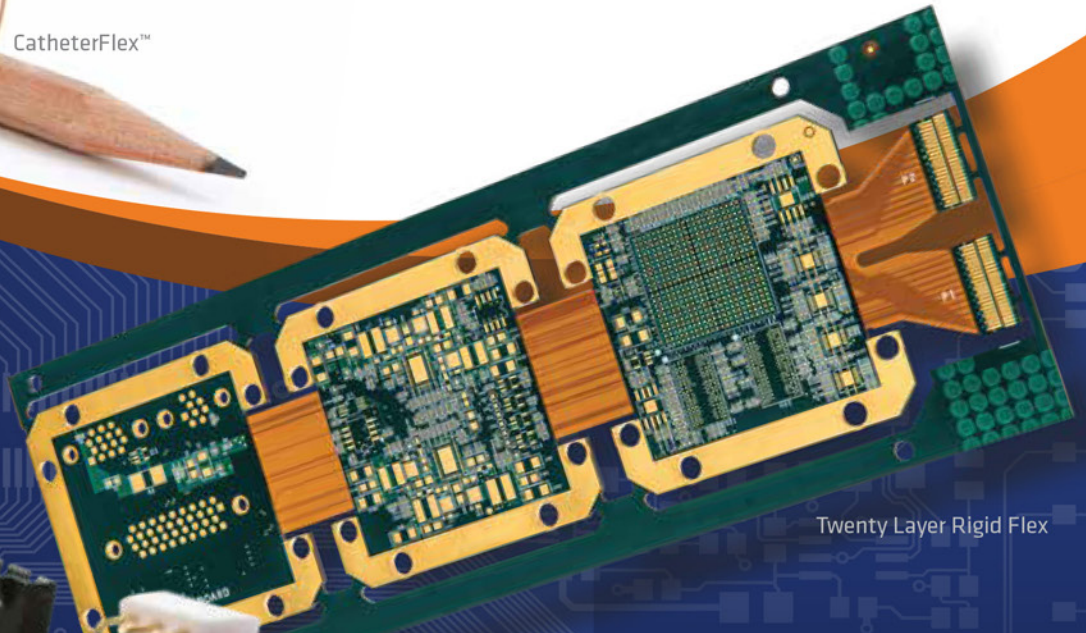


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granted. Their work reminds us that signal integrity has always been an international discipline.

And while AI may soon generate simulations, optimize layouts, suggest stackups, and probably critique our via fields with unsettling confidence, it still depends on the physical principles these masters spent decades researching, explaining, measuring, debating, and teaching the rest of us to respect. Return currents still follow the path of least impedance. Discontinuities still create reflections at the worst possible locations. Power planes still find creative new ways to resonate, and electromagnetic fields still stubbornly obey Maxwell instead of marketing slides.

The Human Layers Still Matter

Signal integrity is a story of accumulation, not replacement, moving from intuition to physics to measurement and now to intelligent automation. It is a global discipline shaped by engineers worldwide,

many of whom may never headline major conferences but continue to define the behavior of today's advanced systems. Signals do not care where the engineer is based; they only respond to whether the physics is respected.

Before SI becomes fully abstracted into systems that design faster than humans can follow, it is worth acknowledging the people who made that future possible. Because once the tools no longer need explanation, the industry may also forget who first taught the rest of us why the explanations mattered in the first place. **I-CONNECT007**



Kelly Dack, CIT CID+, specializes in DfX-driven PCB design and applications engineering at Pioneer Circuits, Inc. To read past columns, [click here](#).

BOOK EXCERPT

The Printed Circuit Designer's Guide to...UV Curable Conformal Coatings: Addressing Future Manufacturing Speed and Need

BY BRIAN J. CHISLEA AND CODY SCHOENER, PHD, DOW, INC.

Chapter 1: Options for Protecting Electronic Assemblies and a Deep Dive into UV Conformal Coatings

Electronics, depending on fit and function, have different protective options including conformal coatings, potting materials, encapsulants, protective enclosures, sealing and gaskets.

Conformal coatings: The most common method for protection involves applying thin, protective films to the surface of a printed circuit board (PCB) or printed circuit board assembly (PCBA) to shield it from moisture, dust, and other contaminants (Figure 1.1a). Conformal coatings can be made from various materials, including acrylics, silicones, urethanes, epoxies and more. Each type of coating offers different levels of protection and flexibility.

Potting and encapsulants: These materials encase the entire PCB or PCBA or specific components in a pro-

TECTIVE material creating a robust barrier against environmental factors while offering additional mechanical support, making it ideal for applications where the PCBA may be exposed to harsh conditions or physical stress (Figure 1.1b). The benefit, due to the thickness of the protective material, is that the chance of ingress is reduced; the drawback is that it adds weight to the final design, which could be detrimental.

Sealing and gasket enclosures: This method, commonly used for PCBAs, involves using seals or gaskets to create a combined barrier around the PCBA, thereby preventing the ingress of moisture, dust, and other contaminants (Figure 1.1c). These enclosures can be made of plastic, metal, or composite materials and further sealed with a polymer material between the joining parts.

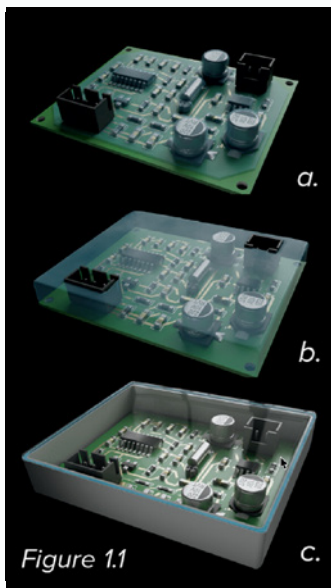


Figure 1.1

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One Design, Many Minds

From Concurrent to Co-design



For decades, hardware development has often looked like a relay race: Work is handed from the mechanical team to the electrical team to the RF team, and eventually back again, hopefully without too many expensive surprises waiting at the finish line. But as products become smaller, faster, smarter, and far more complex, that old-school “over-the-wall” workflow is starting to show its cracks.

Co-design is a more integrated, collaborative approach that promises to shrink design cycles,

improve first-pass success, and maybe even save engineers from a few stress-induced headaches along the way.

In this conversation, Kristin Moyer, a design instructor for the Global Electronics Association, explains the difference between concurrent and co-design, why the shift matters now, and how the future of hardware development may depend less on silos and more on everyone learning to work from the same digital playbook.

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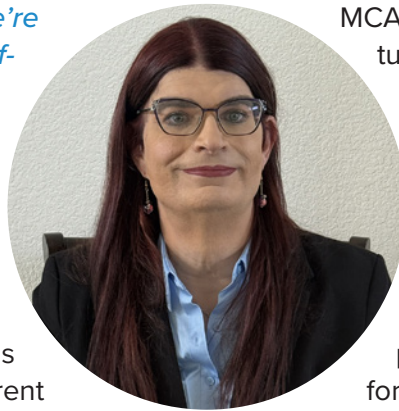


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Marcy LaRont: Kristin, this month we're focusing on potential substantive differences between old-school and new-school thinking. Specifically, let's talk here about concurrent vs. co-design. Can you define both and give an operational example of each approach being implemented?



Kristin Moyer: Concurrent design has always meant that the multiple different silos of design—mechanical design, electrical design, etc.—are happening simultaneously but in their own silos: The mechanical engineering team designs the enclosure, and in parallel, the electrical engineer does the circuit design and PCB layout with just a basic concept of the enclosure and the mounting.

Then, they get together at the end of each design phase to review how all the pieces fit together. If they don't fit, it's back to the drawing board for the affected design groups. This is one of the reasons for revision cycles in product development.

Isn't that a logistics challenge?

It is. A major drawback of concurrent design is time and flow issues. It requires that the different aspects or disciplines of design be carried out in order, which creates many start-stops for individual designers. For an RF product, for example, the regular PCB designer has to stop their work and hand the design over to the RF engineer, who can then continue laying out the board. Once it comes back, the designer continues from where the RF engineer left off.

Do the CAD data suites used to date for PCB and system design contribute to this dynamic?

Yes, historically, CAD tools have provided a single data file for each specific thing that is designed. Let's say your system has three PCBs. Each board has its own specific design engineer, yielding three individual data files.

Those data file formats were based on different design disciplines, especially MCAD vs. ECAD, which used data designed for electrical use, such as two-dimensional drawings. Whereas ECAD or

MCAD was designed for mechanical structures and contained a lot more definitions for mechanical parts and mechanisms that weren't supported in ECAD tools and vice versa.

Modern CAD, ECAD, and MCAD tools have become more tightly integrated. As software and operating systems have become far more powerful, we now have the capability for multiple tools to simultaneously read ECAD, MCAD, and thermal analysis data, and so on, back and forth. We can have a single live dataset that is acted upon simultaneously by the various disciplines.

Concurrent design isn't a perfect system, but until recently, it was the only way we could operate with many different moving parts. Primarily due to advances in our design software tools and their ability to integrate, co-design has become possible.

Yes, data system capabilities and formats have been a huge contributor to this operational dynamic in hardware and system design, and their advancements will support this shift in total system design.

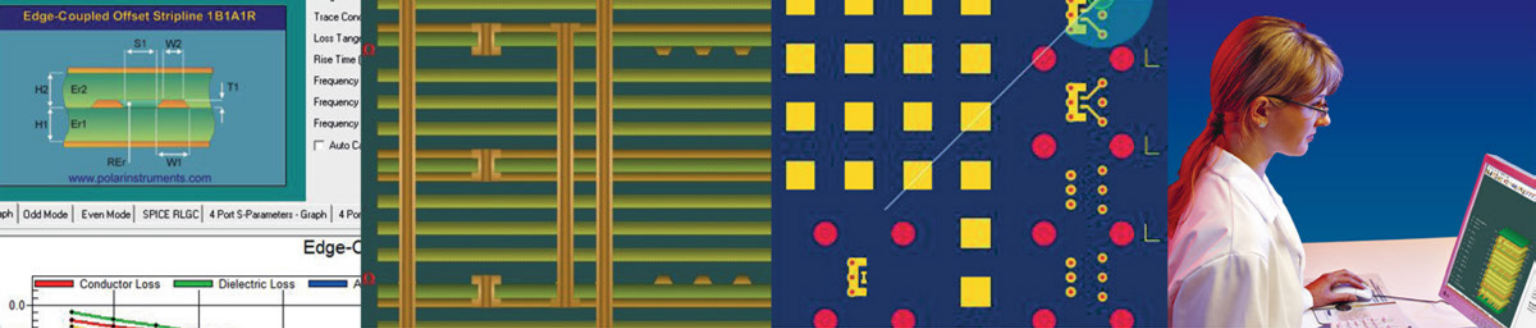
It sounds like you're now talking about co-design.

Yes, co-design, in contrast to concurrent, is where we integrate the different aspects or areas of a product or system design within a single design cycle from the beginning, both from mechatronics and operational points of view.

The data is integrated; there is a single dataset for the product or system being designed. It lives in all the tools simultaneously and can support multiple engineers across disciplines. Engineers can work on the same dataset simultaneously, significantly reducing design cycle time. The RF engineer from the previous example can be working on their section of the layout and routing at the same time as the PCB layout engineer is working on the digital and analog routing sections.

What are some other significant benefits of moving to a co-design operational model?

There are three. As I mentioned, there is a schedule or time benefit. I no longer have to delay the ECAD



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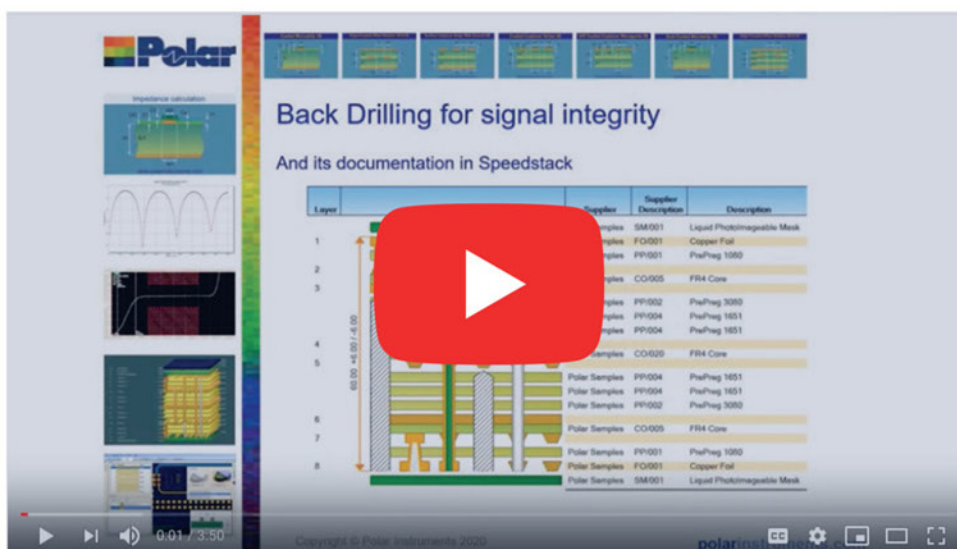
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layout to let the RF team do their thing, etc. It has the potential to significantly reduce design and product development cycle times.

The second benefit is higher reliability and higher first-pass yields. By having all the disciplines work on this design simultaneously, there's a much higher probability that we'll see better designs sooner in the total product development cycle. The constant feedback cycle allows for smaller change requests to be addressed in real time throughout the product development cycle.

Taking the RF example again, in co-design, the RF team does their thing, passes it back to PCB layout, which then passes it over to mechanical. Let's say that when it comes back to RF for review, they can see that the placement over in this one area with the housing has now interfered with the antenna signal path. That specific designer needs to go back in and change this part of their design. Issues are getting addressed as they are observed.

central data set. You can see in real time how small changes requested by one area affect another, so you get more timely feedback and responses.

Are these positive cost implications?

Yes, there's significant potential to reduce the raw or total cost to build. That's the third benefit. You reduce your development costs by reducing cycle time, the likelihood of failures, and the number of revisions needed, all of which mean a shorter time to market. That's huge for profitability.

So, why are we not doing co-design more widely? Is it something that sounds great theoretically, but isn't so easy practically?

Well, not all businesses have a full staff of engineers across multiple disciplines. If you rely on a third party for some of your design work, such as an RF expert, you still need the traditional concurrent design approach: reaching a certain point in the PCB layout before passing it off to the RF engineering firm to do their part, and then waiting for them to finish before you get that design back for further work.

Another barrier is data and cybersecurity. In military, aerospace, and defense designs, the sensitive nature of some information may include classified parameters, for which not all design engineers have the security clearance or authorization to see all aspects of a design. So, when certain parts of a system must be designed within a restricted environment, concurrent design is the logical way to work through a total system design workflow.

A third reason is that the CAD tools a company uses can't integrate data across systems and disciplines. That is still the case for many smaller companies. Contractors may not be privy to all their manufacturing partners for the total system. In those cases, investing in advanced CAD tools that enable the kind of integration co-design requires may not be feasible or practical.

Which tools support this level of co-design?

The Tier 1 tools, all the big, established names everyone knows. Many startups use Tier 2 tools that may or may not support co-design capability. They are just not yet at the point in their organiza-

This software can organize, control, and track product-related data throughout engineering, manufacturing, and operations processes."

Will co-design reduce the need for full design revisions?

Yes, it is likely to reduce design revisions. But more than that, it's likely to give better first pass yields for a higher first pass success rate.

Regardless of revisions, it will reduce your design cycle time by eliminating the built-in pauses to let the next team or engineer do their part, since engineers are all working simultaneously. Instead of working with multiple sets of data files, everyone's design work is now compiled into a single

tions where it makes financial sense to invest in a Tier 1, even if they plan to do so eventually.

Regarding security and cybersecurity, what do military contractors building defense products need to consider?

From a security standpoint, there is both cybersecurity and operational security (OPSEC). This is certainly germane for military contractors. But because co-design reduces overall development cycle time and time-to-market, increases reliability, and decreases total build cost, it will be a big driver for organizations like the military and medical OEMs. In fact, that's true for all high-reliability and Class 3 designs where co-design is the most beneficial. Even though they may not be built in high volumes, they have the greatest need to get designs right the first time.

The Global Electronics Association is known for creating and implementing standards for the industry. Do you see co-design requiring its own standard?

I don't believe that co-design necessarily needs its own separate standard. I think co-design will be most successful with more complete industry adoption of the existing standards tree, rather than just adopting the big three for design, fabrication, and assembly. The full standards tree includes the 2220 series for design, the 6010 series for fabrication, J-STD-001 for assembly, along with the 4000 series for materials, and the 2600 series for documentation, among others, as well as new standards being developed around HDI and packaging."

To have OEMs become familiar with, and adopt the entire spectrum of standards, is to really understand how the parts play together and interact with each other. That is where we will see the greatest benefit of the co-design approach to hardware and systems development.

If companies want to seriously consider co-design, but don't have the ideal environment or tools to support it, what are some appropriate first steps?

There are a couple of areas where a company can make some strides toward a more co-design-friendly ecosystem: technology and tactical business operations.

If you don't have the Tier 1 ECAD and MCAD tools and integration links, you can approach co-design operationally and procedurally. Implement an in-house manual process with much more frequent passing of data back and forth. Even without full co-design implementation through software tools, most businesses use some form of product data management system, such as Teamcenter, Windchill, Doors, or SAP. This software can organize, control, and track product-related data throughout engineering, manufacturing, and operations processes. It acts as a central repository for product information and helps teams collaborate while maintaining version control and process consistency. Such systems allow for checking data in and out.

You could implement a process, whether automated or procedural, requiring engineers to check their data in at the end of each day or shift. It can then be reviewed by and between the various design elements as the design moves through. Things will be caught and fixed more quickly.

From a technology point of view, even if you do not have a complete co-design environment through your CAD tools, make the most of the ECAD and MCAD tools you do have. They often have viewer versions or limited/light versions of their tools. You do need some cross-functional training in this scenario. But you can train your ECAD engineers on how to open, view, and do some measurements in the MCAD environment and vice versa, between all the different design tools and disciplines.

Not only are you checking data in and out and synchronizing between the two teams more frequently, but you'll have fewer instances needing your ECAD engineer to track down your MCAD engineer to ask why they set this spacing between these two ribs of the enclosure in this specific area, etc. They can perform their measurements, analyses, and fit checks simultaneously without taking design time away from the engineer doing the actual engineering work. They will be more independent, and this will help the design process move more quickly.

I like that. This has been really interesting and informational, Kristin. I look forward to watching this trend going forward.

Great talking with you, Marcy. **I-CONNECT007**



BUILDERS OF THE DREAM

BY JOHN WATSON, PALOMAR COLLEGE

In 1849, French writer, journalist, and satirist Jean-Baptiste Alphonse Karr wrote the famous line, “Plus ça change, plus c’est la même chose,” which translates as “The more things change, the more they stay the same.” He penned it in his satirical journal, *Les Guêpes* (*The Wasps*), during a period of great upheaval in France.

The February Revolution in 1848 had just shaken the country, the July Monarchy had fallen, and the French Second Republic had emerged. To many, it seemed as if everything was changing. But Karr’s insight suggested that while leaders, systems,

slogans, and structures may shift, beneath the surface, the same patterns of ambition, conflict, and repeated mistakes often remain. His words remind us to look past appearances and ask: Has something truly changed, or has it simply been given a new name, tool, or look?

That very question returned to me in an unexpected place: a small gift shop in Yosemite Valley, California, a few weeks back. Among the racks of nostalgic books by Sterling Publishing was a series called “The Year You Were Born.” I rotated the rack, flipping through the years, until the



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browsing became archaeology: 1990s, 1980s, 1970s. Finally, 1961, the year I was born, appeared. It's hard to believe that in 1961, we thought a slide rule was a supercomputer.

It was fun to flip through the pages, learning about the cost of gas, popular TV shows, who won the World Series, and the most popular songs of the day. Yet it also became clear that the book wasn't just showing how different the world was; it was really showing how much has stayed the same.

PCB design offers a similar lesson. On the surface, it has changed dramatically. The drafting tables, tape, Mylar, and light tables of old have been replaced by CAD tools, digital libraries, 3D models, cloud platforms, and automated rule checks. Old-school designers worked with physical artwork and a steady hand; new-school designers work with layers, constraints, simulations, and enough menus to make it feel like launching a satellite. I remember well those "good old days," coming home with sliced fingers, Mylar tape everywhere, and enough adhesive on your clothes to qualify as a walking PCB layout.

The speed has changed. What once took hours, days, or even a complete redo can now be revised, rerouted, checked, and regenerated almost instantly. That beautiful "undo" button is one of the greatest inventions in PCB design history, because nothing says progress like instantly erasing your own mistakes.

The complexity has changed. Modern boards are denser, faster, smaller, and far more demanding. Designers now handle fine-pitch parts, BGAs, controlled impedance, differential pairs, EMI/EMC issues, power integrity, rigid-flex, and manufacturing data that must survive the full path from design to fabrication to assembly.

But the designer's role has had some major changes as well. PCB design is no longer just about connecting pins. Designers must understand the circuit, the mechanical fit, the manufacturing and assembly processes, documentation, sourcing, reliability, and sometimes even why the engineer picked that impossible connector.

Even with all these changes, the core of good design remains completely unchanged. Careful

placement, thoughtful routing, proper spacing, respect for manufacturability, and understanding how every component, trace, and layer interacts have guided designers for decades. These principles are not just rules; they mean that every board works, survives testing, and powers our technology.

Working with university students brings this connection to life. New design students step into the class, nervous yet eager to learn, experiment, and push the limits of what they can create. Their energy is contagious. I know the fundamentals we teach—critical thinking, attention to detail, and problem-solving—are more than classroom lessons; they are the tools the next generation will use to shape the future.

Understanding the truth of what has stayed the same gives this work real meaning. The challenges may have changed, and the tools may be new, but the skills and mindset remain timeless. Every trace, connection, and thoughtful decision reminds us why this work matters.

Now imagine visiting that Yosemite gift shop in the future, where the racks once again spin with small books from Sterling Publishing. Among them, one title stands out: *Year 2026 in PCB Design*.

This book won't be filled with statistics, charts, or snapshots of the latest technology. Its focus will be on the people behind the boards: the designers, students, and teams who bring ideas to life through focus, creativity, and determination.

It will celebrate the timeless disciplines of PCB design, including attention to detail, respect for the process, critical thinking, and problem-solving. These fundamentals, combined with today's tools and technology, allow designers to create boards that power ideas no one has yet imagined.

We know this story is not really about the boards. The boards are only the result. The real story is about the minds and purpose behind them: the student who stays late in the lab to solve one more problem, the designer who refuses to compromise on quality, and the team that works together to turn an idea into something real, reliable, and meaningful.

Maybe if Karr were alive today, he would be smiling with a cheerful, "That's what I meant." Tools

and technology change, but the human side of the work still matters most. With each generation, it's clear that the future of PCB design is in capable, curious, and passionate hands.

Our future is bright. Not because PCB design will stay the same; I know it won't, and honestly, I hope it doesn't. Progress demands change. But what must remain is the mindset behind the work: curiosity, discipline, imagination, and the determination to turn ideas into something real.

As an instructor, I often remind my students that they are the builders of the dream. They carry forward the lessons of the past, use the tools of the present, and bring the courage to imagine what

comes next. Every schematic, layout, and solved problem becomes part of something larger than the board itself. In that, Karr was right. Fortunately, the more things change, the more they stay the same.

I-CONNECT007



John Watson is a professor at Palomar College, San Marcos, California. To read past columns, [click here](#).

BELOW THE SURFACE

From Nanometers to 10-Gauge: It's More Than Just a Wire

BY CHANDRA GUPTA, REMTEC

Modern life runs on printed circuits: Your phone, your car, satellites overhead, and even everyday appliances rely on carefully patterned pathways that guide electricity where it needs to go. From nanometer-scale traces integrated into semiconductor chips to thick film conductors printed onto ceramic substrates—and ultimately connected to heavy 10 gauge wires delivering power—it's easy to think of them all as the same thing and say, "It's just a wire."

But that simplicity hides the real story: In printed circuits, those "wires" are engineered materials and structures, designed across multiple scales to perform far more than just carrying current.

The real sophistication lies not in the conductor alone, but in the engineered materials and structures around it—the layers that insulate, protect, support, and interconnect printed paths while withstanding heat, voltage, vibration, and long-term use. Advanced packaging and substrate technologies make this possible, ensuring that the entire system operates reliably under demanding conditions.

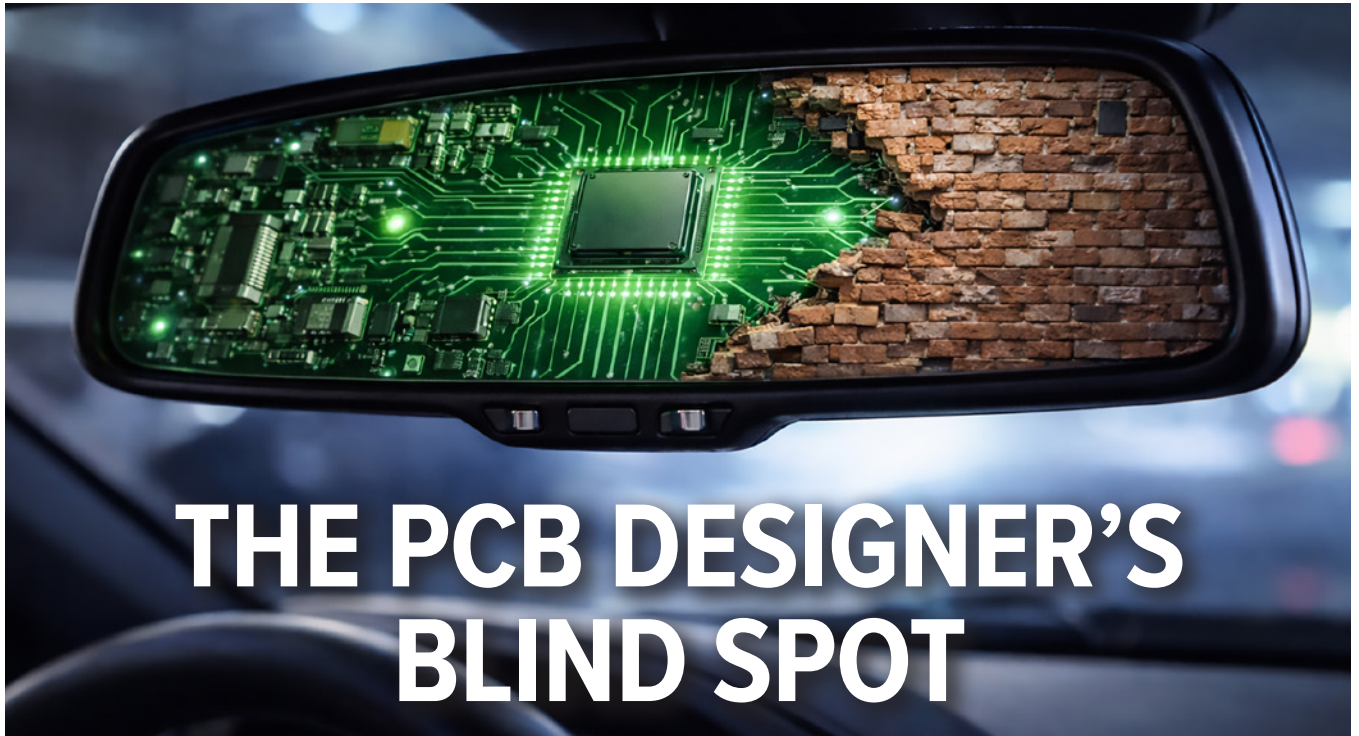
A Wire Is Easy, a Reliable Wire Is Not

At its simplest, a wire is a conductor, usually copper, that allows electrons to flow. If all we cared about was turning on a light for a few minutes, that might be enough. But in real systems, wires must:

- Carry precise amounts of current without overheating
- Maintain signal integrity at very high speeds
- Survive years or decades of thermal cycling
- Operate safely at thousands of volts
- Function in environments ranging from humid factories to space

When engineers design electronic systems, the wire is only the starting point. Everything around it matters just as much, if not more.

[Click here to read the full column](#)



THE PCB DESIGNER'S BLIND SPOT

No Feedback, No Progress

In PCB design, time and effort are everything. You've spent weeks perfecting your schematic, routing traces, and ensuring signal integrity. Finally, you generate those Gerber files and send them off to your preferred PCB fabricator. It's a moment of relief: The design is out of your hands, and production can begin. But what happens next?

For many PCB designers, the answer is surprisingly unclear. Fabricators often make manufacturability adjustments without providing detailed feedback, leaving designers unaware of recurring issues. The solution is not waiting for better communication from the fabricator. Designers can implement independent CAM validation tools that give them direct visibility into manufacturability problems before release.

This handoff is notoriously known as "throwing it over the wall," a term that vividly captures the abrupt, one-way transfer of files with minimal communication between designers and fabricators. Behind that wall lies a host of unknowns that could torpedo your production timeline, or worse, undermine your design's performance.

The "wall" isn't just a metaphor; it has, in fact, become a literal barrier erected by the hyper-competitive nature of global PCB fabrication. With razor-thin margins and instant online quoting systems, fabricators prioritize speed and customer retention above all else. They battle for volume in a market dominated by low-cost providers, with many of them being overseas, where a single delay could send a client jumping ship to a competitor.

As a result, when your unverified production files arrive, which could potentially contain issues such as undersized drills, misaligned layers, or missing board outlines, fabricators often choose not to object. Instead, they might quietly intervene, or they might not. The uncertainty leaves designers in the dark and perpetuates a cycle of inefficiency and missed opportunities to improve.

The Competitive Blind Spot

Imagine submitting a set of Gerber files with a subtle flaw: a solder mask opening that's too narrow, risking shorts during assembly. In an ideal world, the fabricator would flag the issue, explain it, and

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	Dk / Df @ 10 GHz	Dk / Df @ 20 GHz	Dk / Df @ 30 GHz
Industry Std Mid-Loss	3.40 / 0.0035	3.35 / 0.0035	3.33 / 0.0035
I-Tera MT40	3.30 / 0.0031	3.28 / 0.0031	3.27 / 0.0031
Industry Std Mid-Loss	3.18 / 0.0018	3.15 / 0.0018	3.12 / 0.0018
Tachyon 100G	3.10 / 0.0021	3.07 / 0.0021	3.04 / 0.0021
TerraGreen 400G	3.15 / 0.0017	3.10 / 0.0017	3.07 / 0.0017

Values shown are typical across 10-30 GHz and demonstrate comparable electrical performance.

request a revision, allowing you to refine your design process, perhaps by adjusting your CAD tool settings or incorporating better tolerances.

In reality, many fabricators opt for silence in favor of speed. Their in-house engineers might resize the opening, shift a layer, or add the missing outline without consulting the designer. The boards arrive on time, function (mostly), and you can move on to the next project. While such a “fix-and-forget” approach keeps the production line moving, it comes at a steep hidden cost to the designer.

First, there’s the unpredictability: Fabricators may or may not fix your errors. Some issues, like minor drill size discrepancies, are easy to correct in-house. Others, such as impedance mismatches or poor panelization, might slip through if they’re deemed non-critical to the fabricator or if the production engineer is rushed.

What if the fix introduces a new problem? A shifted layer could inadvertently create EMI issues in your high-speed design, leading to field failures you might attribute to assembly rather than to a silent alteration during board fabrication. Without communication, you’ll never know, and this Russian roulette with your files erodes trust in the supply chain and exposes your projects to unnecessary risks.

More critically, the lack of communication stifles



you and your team’s professional growth.

Every uncaught error reinforces bad habits. Maybe you’ve been routing traces too tightly, ignoring fabrication tolerances, or skipping basic design for manufacturing (DFM) checks in your CAD software. Over time, these oversights become ingrained.

You might produce functional boards, but they’re far from optimal and could be wasting materials, reducing yields, and potentially increasing costs downstream.

Industry data shows yield rates hovering at 85–90% when 98%+ is possible with proper DFM. That gap represents scrapped panels, excess material use, and environmental waste, all because the feedback loop is either broken or not in place at all.

Without dialogue across the “wall,” designers and fabricators operate in silos. You might not realize that your stackup lacks embedded impedance data, or that your panelization could be optimized for better efficiency, potentially cutting costs by 10–20% or more depending on volume and optimization.

This forces the fabricators to make assumptions, and they often take on these burdens to keep customers happy. However, they rarely share their insights. But why? Providing detailed reports could reveal trade secrets or slow down the PCB fabricators’ workflow. In rare instances, designers

might receive a generic email about a “minor adjustment,” but obtaining any substantial advice on enhancing their DFM process is extremely uncommon, if not nonexistent.

Unfortunately, this built-in opacity is slowing innovation in areas where precision is paramount to reach maximum performance.

The Real-World Impact on Designers

As a PCB designer, you’re at the forefront of electronics innovation. Whether you’re crafting boards for IoT devices, medical

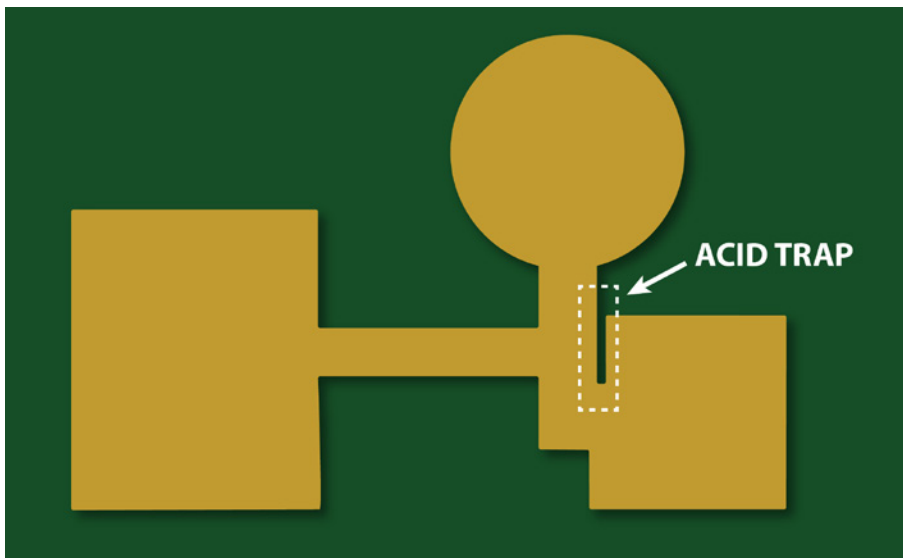


Illustration of an acid trap which can compromise a PCBs durability. Etching solution becomes trapped at the junctions where traces meet at sharp angles as shown.

DIRECT METALLIZATION

The Next Evolution in PCB Technology

As advanced PCB and IC substrate technologies continue to evolve, direct metallization is emerging as a critical process for improving reliability, enabling higher-density interconnects, and supporting sustainability goals.

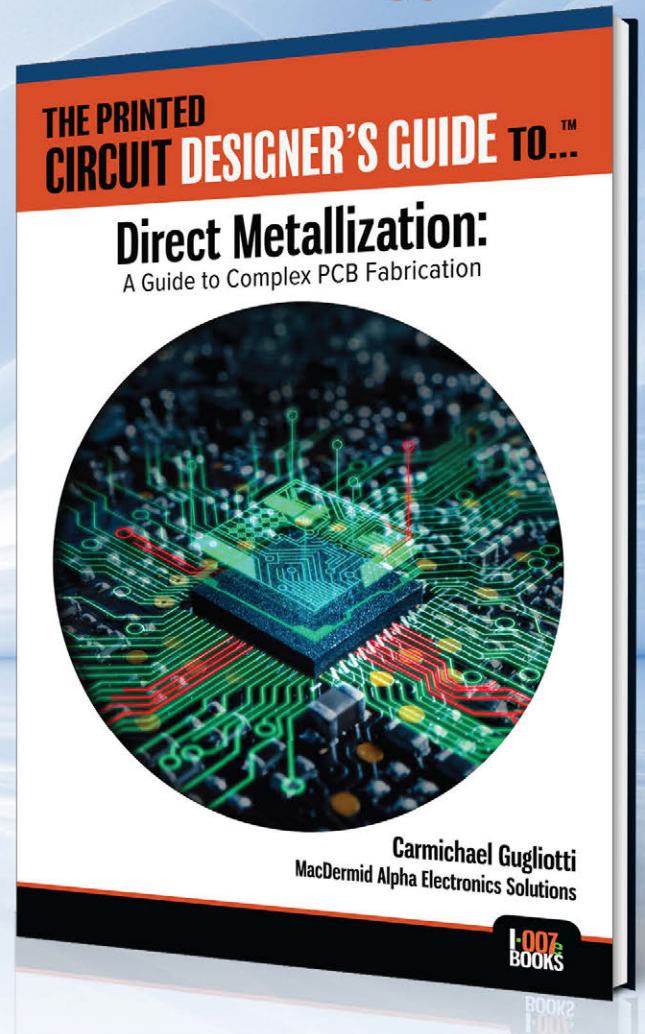
Featuring insights relevant to PCB designers, fabricators, OEMs, and process engineers, this book provides the technical foundation needed to understand, evaluate, and implement direct metallization technologies in next-generation manufacturing environments.

"An essential resource for fabricators and OEMs."

—Venkat Raja, Advint, Inc.

"A clear and practical perspective on direct metallization."

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"This book provides the definitive view on the use of direct metallization for advanced printed circuit boards and IC substrates."

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equipment, aerospace, communications, or automotive systems, your work demands reliability and efficiency. Yet, by throwing it over the wall with unverified files, you gamble on the outcome, betting that the fabricator will catch whatever potential DFM violations your CAD may have missed.

CAD tools are powerful for layout and simulation, but they're not infallible. They frequently overlook fabrication-specific pitfalls such as annular ring violations, acid trap formations, or silkscreen overlaps that could lead to production issues. DFM rules can vary from company to company, as they are based on the fabricator's experience, process flow, and technical capabilities.

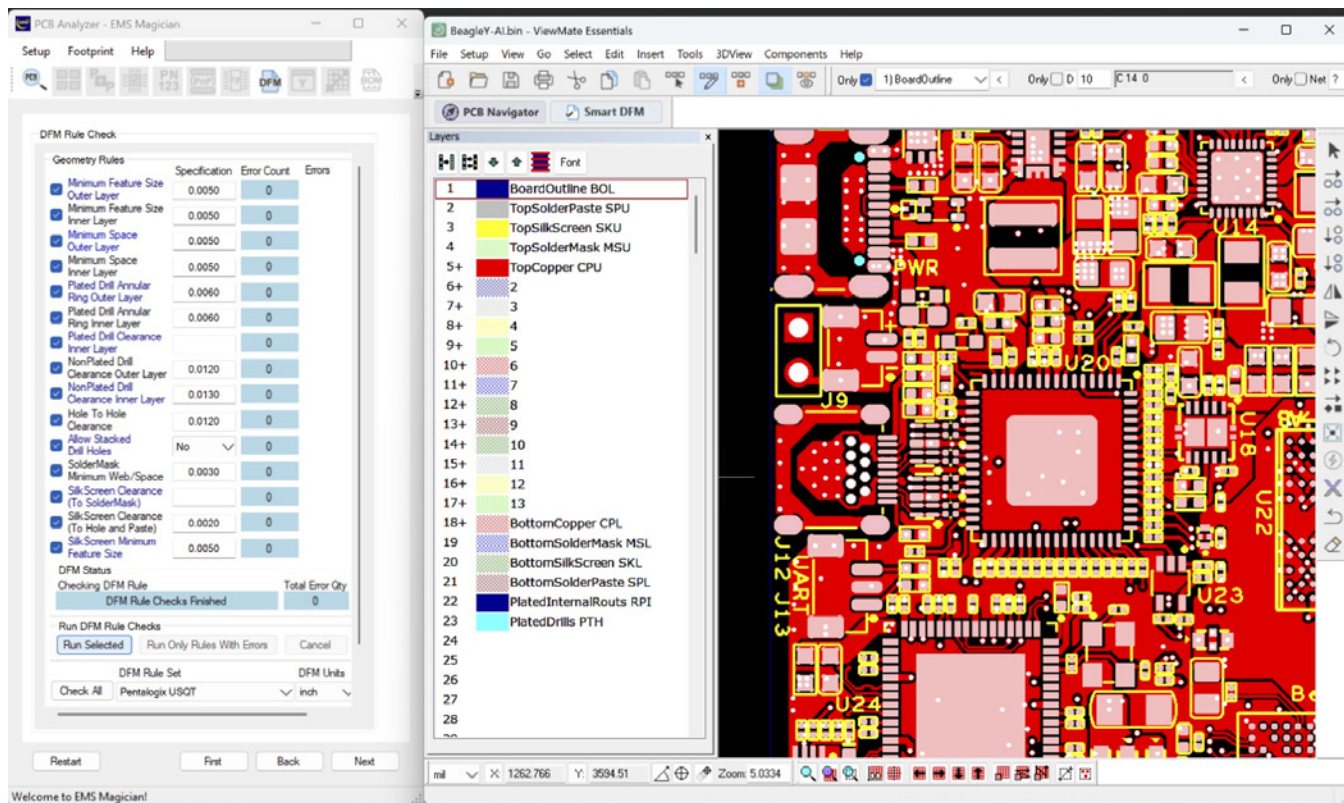
The consequences extend beyond individual projects. Repeatedly submitting flawed files without correction leads to stagnant skills. You miss out on learning best practices, such as adhering to IPC standards. Over time, this could make you less competitive in the job market, where more

employers value designers who prioritize DFM from the outset. Moreover, in high-stakes fields, undetected issues can lead to significant delays, product recalls, safety hazards, or even financial losses, all scenarios in which the design phase can quickly become the target of heightened scrutiny.

Breaking the Cycle

While the wall stifles communication, you don't have to wait for fabricators to tear it down. The solution lies in integrating independent CAM tools into the workflow, like Gerber viewers or Gerber editors. These add-ons to a CAD system are essential for detecting issues that CAD overlooks, so it's important that they be independent of CAD. Working with the same data that the fabricator sees allows you to prevent manufacturing errors and, more importantly, learn and improve your design process and foster a robust DFM culture.

Beyond detection, CAM empowers self-improve-



Professional Gerber viewers and Gerber editors allow you to validate your Gerber files before submission. They run comprehensive checks for drill tolerances, layer alignments, solder mask clearances, and more, generating detailed reports that highlight warnings in plain language. This catches errors early, reducing revisions and accelerating time-to-market.

ment. By reviewing reports, you learn to anticipate fabrication challenges, like optimizing trace widths for better yields or embedding stackup data to eliminate ambiguity. Some advanced CAM platforms even simulate panelization, helping you minimize waste and costs. With standards like ODB++ and IPC-2581 gaining traction, CAM facilitates seamless data exchange, turning your files into a blueprint for success rather than a puzzle for the fab.

Incorporating CAM isn't complicated. It can start with a simple Gerber viewer that integrates with the CAD environment to validate the production files. Beyond that, a more powerful Gerber editor can run validations after layout completion, addressing issues, and generating a DFM report to accompany your submission. Over time, CAM should be treated as a core review step, on par with schematic simulations. Training resources, online forums, and industry certifications can help designers master it quickly.

Building a Better Design Culture

PCB designers must recognize the perils of throwing it over the wall. The existing culture of silent fixes, or no fixes at all, denies PCB designers the insights needed to refine their workflows and elevate their DFM practices. Hoping for valuable input from across the wall is, in most cases, a losing strategy. It only perpetuates errors, wastes resources, and hampers innovation.

Instead of waiting for the fabricator to speak up, the design team should empower itself with the right tools and transform uncertainty into precision. Independent Gerber viewers and Gerber editors are an indispensable part of the process. By detecting errors before they become "production issues," these tools help produce cleaner designs, improve yields, and build a culture of continuous improvement. **I-CONNECT007**

My Trip to Schneider Electric AI, Data, and the Need for More Power

BY MARCY LARONT, I-CONNECT007

AI is pushing power infrastructure to its limits, and many of those same challenges, particularly around power delivery and heat management, parallel what the electronics industry faces in building and scaling advanced microelectronics. Yet when it comes to AI and hardware, we typically only see a small piece of the total picture. So, when Schneider Electric invited me to tour a modern AI data center still under construction, I jumped at the opportunity. This became a fascinating technical journey I'm excited to share.

Who Is Schneider Electric?

Schneider Electric is a French multinational company with nearly 200 years of history that began in steel production and heavy machinery. Today, it is a global leader in energy management, industrial automation, and digital infrastructure, operating in more than 100 countries. Its technologies sup-

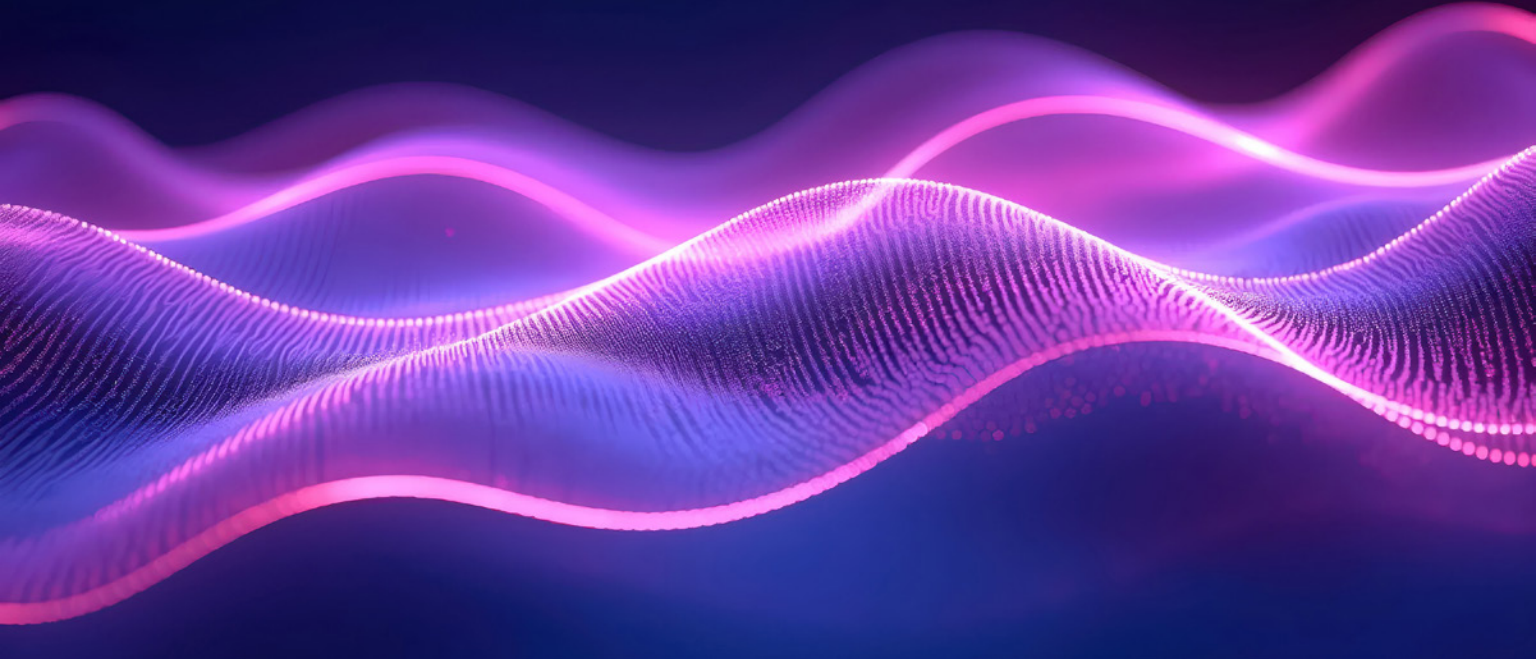
port factories, utilities, buildings, and data centers worldwide, with a growing emphasis on electrification, automation, and sustainability. Schneider Electric has also become a major player in the AI boom, investing heavily in power distribution, automation software, and advanced liquid cooling systems designed for high-performance computing.

While data centers themselves are not new, next-generation AI facilities present entirely new challenges. "AI factories are not traditional data centers; they're purpose-built to produce digital insight across the AI lifecycle," said Steve Carlini, chief advocate of data centers and AI. "With 60% of deployments moving to AI and power densities jumping from 20 to 150 kilowatts per rack, this is a fundamental shift in how we design and operate infrastructure."

[Click here to continue reading.](#)

SKIP-LAYER ROUTING

The Waveguide Structure That Makes 224G Possible



BY BARRY OLNEY, IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

As data rates climb from 112G PAM4 toward 224G PAM4 and beyond, electronics designers are discovering that traditional strip-line and microstrip geometries are no longer sufficient. The physics simply break. Rise times are now in the single digit picosecond range, loss budgets are measured in millimeters, and even tiny discontinuities can collapse a PAM4 eye.

Next-generation Ethernet is moving to 224G signaling, enabling the transition to 1.6 terabit Ethernet. As data complexity explodes and servers hit their physical density limits, the industry can no longer rely on simply adding more pluggable modules. The only viable path forward is faster SerDes, which converts parallel data into a high-speed serial stream for transmission and reconstructs the parallel data at the receiver. Beyond raw bandwidth,

224G delivers architectural advantages: fewer cables, fewer switches, and more efficient network fabrics. Its inherent backward compatibility ensures that operators can integrate 224G into existing Ethernet environments without disruption.

Higher data rates demand modulation schemes with greater spectral efficiency. For decades, non-return-to-zero (NRZ) has been the workhorse for standards like PCIe and Ethernet 802.3, but as bit rates surpassed 32 Gbps, PAM4 signaling has become the standard. This scheme uses multiple signal levels or phases to encode more bits per symbol, thereby increasing the channel's spectral efficiency and data rate. However, they also increase the complexity and sensitivity of the signal-processing and recovery circuits, requiring careful PCB design to ensure proper signal quality and synchronization.

NRZ is a modulation technique that has two



Hmm, what is recommended
**minimum distance for
copper to board edge?**

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

Every day we get questions like those. And we love it. We have more than 600 PCB experts on 3 continents speaking 19 languages at your service. **Regardless where you are or whenever you have a question**, contact us!

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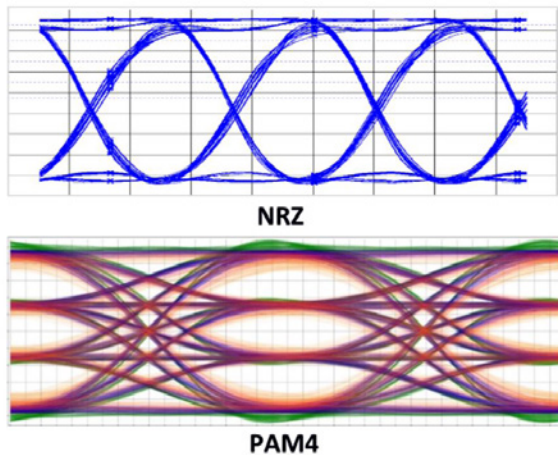


Figure 1: NRZ eye vs. PAM4 eye. (Source: Xilinx)

voltage levels to represent logic 0 and logic 1 and is limited to 28 Gbs per lane. PAM4 uses four voltage levels to represent the 2-bit logic combinations 11, 10, 01, and 00 (Figure 1). A 224G PAM4 lane requires approximately 56 GHz of usable channel bandwidth.

To survive at these speeds, routing must evolve from controlled impedance traces into engineered electromagnetic structures. One of the most promising of these structures is skip layer routing, a differential waveguide geometry originally developed for IC substrates now emerging as a practical solution for ultra high speed PCB channels. It involves a type of substrate-integrated waveguide structure for differential pairs. A differential stripline pair is essentially routed between two reference planes and surrounded with a fence of ground vias. This creates a differential coaxial-like waveguide within the substrate, commonly used to carry high-speed signals down to the BGA ball-out.

The limitation is bandwidth; PAM4 requires 56 GHz. At these frequencies:

- Traditional stripline excites higher-order modes
- Vias behave like resonant cavities
- Plane cavities radiate
- Crosstalk becomes unavoidable
- Copper roughness dominates loss
- Dielectric loss is no longer the limiting factor

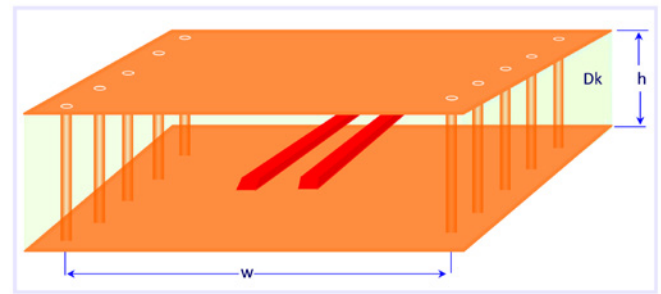


Figure 2: Skip-layer 224G differential waveguide structure.

The channel must keep the signal in the quasi-TEM mode. That is the clean, single-mode behavior where the fields stay tightly contained between the trace and its reference planes. Once a higher-order mode is triggered and the fields disperse, the fields spill into lossy paths, the waveform distorts, and the eye collapses.

This is where skip-layer routing comes into play. It is a coaxial-like waveguide formed by a differential pair sandwiched between two reference planes and surrounded by a via fence. This creates a rectangular cavity that behaves like a differential waveguide (Figure 2). The waveguide geometry pushes the first higher-order mode far above the operating frequency.

The cutoff is determined by the cavity width, height, via spacing, and trace separation. The via pitch must be $\leq \lambda/8$ (0.37 mm) at the highest frequency. If the cutoff is above 56 GHz, the channel remains clean with reduced EMI, minimal differential to common-mode conversion, and low lane-to-lane crosstalk.

Also, at 56 GHz for 112G PAM4 and 112 GHz for 224G PAM4, conductor loss becomes the dominant impairment in the channel. Rough copper dramatically increases skin-effect loss, introduces phase-delay variation, and drives additional mode conversion, all of which collapse PAM4 eye height. Using hyper-very-low-profile (HVLP) copper mitigates these effects, reducing conductor loss by roughly 1–2 dB per inch at 56 GHz compared to standard copper, a substantial improvement at these frequencies.

Skip-layer routing uses blind skip-vias to jump directly to the appropriate stripline layer, eliminating unnecessary layer transitions, via stubs, antipad discontinuities, and reference plane changes. Skip-layer routing aligns perfectly with the emerging

A person in a yellow shirt is sitting on a suspension bridge that spans a deep valley. The bridge is made of wooden planks and metal cables. Below the bridge is a calm lake reflecting the surrounding mountains. The mountains are covered in snow and have jagged peaks. The sky is a mix of blue and orange, suggesting sunset or sunrise. The foreground is a rocky, uneven path leading up to the bridge.

Hmm... If I have a **conductor width and isolation distance of 40 μm (1.5 mils)**, does that mean my **PCB is considered Ultra HDI?**

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

Every day we get questions like those. And we love it. We have more than 600 PCB experts on 3 continents speaking 19 languages at your service. **Regardless where you are or whenever you have a question**, contact us!

What's your PCB question?

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Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
1	8	Soldermask	Top	Dielectric	3.3	0.5								
2		Signal	Prepreg	Conductive	3.76	2.8	1.4	8	4	0.31	53.79	100.36		Tg=180C; Df=0.0274
3		Plane	GND	Conductive	3.39	3	1.4							
4		Signal	Inner 3	Conductive	3.16	3.5	0.7	7	3	0.15	50.18	98.35	1957.58	Tg=200C; Df=0.004
5		Plane	VCC	Conductive	4.1	16	1.4							Tg=200C; Df=0.002
6		Signal	Inner 3	Conductive	3.92	4.8	0.7	8	6	0.25	50.13	90.86	1957.58	Tg=180C; Df=0.022
7		Plane	GND	Conductive	3.3	0.5	1.4							Medium Speed Routin
8		Soldermask	Bottom	Dielectric										Tg=180C; Df=0.0250

Figure 3: 112G short-reach hybrid stackup. (Source: iCD Stackup Planner)

rules for ultra-high-speed stackups:

- Thin dielectrics (2–3 mil). Thin dielectrics confine the fields and raise the cutoff frequency.
 - Ultra-low loss materials. The waveguide reduces radiation and crosstalk, but dielectric loss still matters.
 - HDI-only via structures. Through-vias excite higher-order modes. Skip-vias and microvias do not.
 - Minimize transitions. Skip-layer routing reduces the number of via transitions dramatically.
 - Field containment is mandatory. Skip-layer routing is literally a field containment structure.
 - Crosstalk must be engineered. The via fence becomes the crosstalk control mechanism.
- Standard low-loss or mid-loss materials (e.g., Isola 370HR) for the rest of the board
 - HDI microvias and skip-vias for clean BGA escape
 - Conventional through-vias for slower signals and power distribution

A 112G short-reach hybrid stackup (chip-to-chip) is shown in Figure 3. It uses blind skip-vias from layers 1 to 3 to give a clean escape from the fine-pitch BGA, with the 112G lanes routed on layer 3 using Megtron 7, while medium-speed digital signals run on layer 5 in 370HR to reduce cost. The iCD Stackup Planner is set to HDI sequential-build mode to exclude resin flow.

The **224G long-reach ultra-low-loss stackup** (backplanes, etc.) in Figure 4 supports dual 224G waveguide layers on L3 and L5. Surface skip-layer vias drop directly into each waveguide layer, preserving quasi-TEM behavior, cutting transitions, and driving loss down. GND via fences are used to close the cavity. This is the architecture Intel and Synopsys are converging toward.

Figure 5 illustrates numerous differential pair grounded coplanar waveguides routed internally on the stripline layers. Via fences shield the pairs as they traverse the board to the RF connectors.

Skip-layer routing is not a fad, but a necessary evolution of PCB interconnects as we push toward 224G and beyond. It brings packaging-level electromagnetic engineering into the PCB domain, giving designers a practical way to maintain quasi-TEM propagation, suppress higher-order modes, and control crosstalk at frequencies where traditional stripline fails. As data rates double, the PCB will increasingly resemble a microwave structure, and skip-layer routing is one of the first signs of that future.

Suitable Dielectrics for 224G

For 224G PAM4, only ultra-low-loss dielectrics with $D_f = 0.002$ and tightly controlled D_k (3.2–3.4) are suitable. These materials use E-glass spread fiber to reduce skew and must support 56 GHz Nyquist bandwidth while minimizing loss, skew, and higher-order mode excitation.

Stackups Where Skip-layer Is Mandatory

- 112G short-reach hybrid stackup.** A short-reach hybrid stackup is a mixed-performance PCB structure designed to support 112G PAM4 on selected layers while keeping overall fabrication cost and layer count under control. It blends:
 - One or two ultra-low-loss stripline layers for the SerDes lanes

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Stackup Planner PDN Planner CPW Planner

2 Layer 4 Layer 224G Long-Reach Ultra Low loss 8 Layer 10 Layer 12 Layer 14 Layer 16 Layer 18 Layer

UNITS: mil 5/1/2026 Total Board Thickness: 22.1 mil

Differential Pairs > Pair 1

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
1	8 4 8	Soldermask	Top	Conductive	3.3	0.5	1.4	8	6	0.42	53.67	98.07		
2		Prepreg		Megtron 7, 1078, Rc=70% (34GHz)	3.16	3.5	1.4							Tg=200C, Df=0.002
3		Plane	GND	Conductive			1.4							
4		Core		Megtron 7, 1-1078, Rc=63% (34GHz)	3.39	3								Tg=200C, Df=0.004
5		Signal	Inner 3	Conductive			0.7	7	3	0.15	50.18	98.35	1957.58	224G Waveguide
6		Prepreg		Megtron 7, 1078, Rc=70% (34GHz)	3.16	3.5								Tg=200C, Df=0.002
7		Plane	VCC	Conductive			1.4							
8		Core		Megtron 7, 1-1078, Rc=63% (34GHz)	3.39	3								Tg=200C, Df=0.004
9		Signal	Inner 5	Conductive			0.7	7	3	0.15	50.18	98.35	1957.58	224G Waveguide
10		Prepreg		Megtron 7, 1078, Rc=70% (34GHz)	3.16	3.5								Tg=200C, Df=0.002
11		Plane	GND	Conductive			1.4							
12		Soldermask	Bottom	Conductive	3.3	0.5								

Figure 4: 224G long-reach ultra-low-loss stackup. (Source: iCD Stackup Planner)

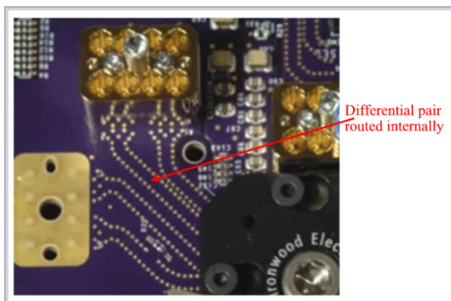


Figure 5: 224G PAM4 test platform. (Source: Synopsys)

Key Points

- Next-generation Ethernet is moving to 224G signaling, enabling the transition to 1.6 terabit Ethernet.
- Higher data rates demand modulation schemes with greater spectral efficiency.
- As bit rates surpassed 32 Gbps, PAM4 signaling has become the standard.
- At these speeds, routing must evolve from controlled impedance traces into engineered electromagnetic structures.
- Skip-layer routing is a coaxial-like waveguide formed by a differential pair sandwiched between two reference planes and surrounded by a via fence.
- The via pitch must be $\leq \lambda/8$ (0.37 mm) at the highest frequency.
- Rough copper dramatically increases skin-effect loss, introduces phase-delay variation, and drives additional mode conversion, all of which collapse PAM4 eye height.

- Skip-layer routing uses blind skip-vias to jump directly to the appropriate stripline layer, eliminating unnecessary layer transitions, via stubs, antipad discontinuities and reference plane changes.
- For 224G PAM4, only ultra low loss dielectrics with $Df = 0.002$ and tightly controlled Dk (3.2–3.4) are suitable. **I-CONNECT007**

Resources

- Beyond Design by Barry Olney: Balancing Trade-Offs for Optimal PCB Design, Substrate Integrated Waveguides
- Skip-Layer Routing for High Bandwidth Channels, Interference Technology
- Will Skip-Layer Routing Work Past 56 GHz?
- Accelerating Hyperscale Data Centers w/ 224G SerDes Ethernet, Synopsys Blog
- 224G Ethernet PHY IP, Synopsys
- 224 Gbps PAM4 end to end channel solutions, Intel



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, [click here](#).

Flip-Chip to Chiplets

The Evolution of System-Level Packaging

BY VERN SOLBERG, CONSULTANT

The electronics industry has experienced a renaissance in semiconductor package technology, driven by the need to maximize electronic product functionality while minimizing the area reserved for component mounting and interconnects.

Passive surface mount components are relatively small, while the packaged semiconductor die is significantly larger than the tiny die element it encases. The plastic-packaged semiconductor, although suitable for use on PCBs, is far too bulky for those developing electronics that require miniaturization: new product introduction systems for physically stressful operating conditions, such as aeronautics, military ordinance, and space missions.

For these applications, design engineers needed to abandon the plastic-encapsulated lead-frame-packaged semiconductor and use only bare, uncased die elements. So, companies began to quickly and economically develop modular hybrid system-level products with commercially available uncased die, implementing the same assembly methods used for packaged semiconductors and wire-bond technology. This category of products became known as a multi-chip module (MCM).

What is a Multi-chip Module?

This generic electronic assembly method integrates two or more bare (uncased) semiconductor die and

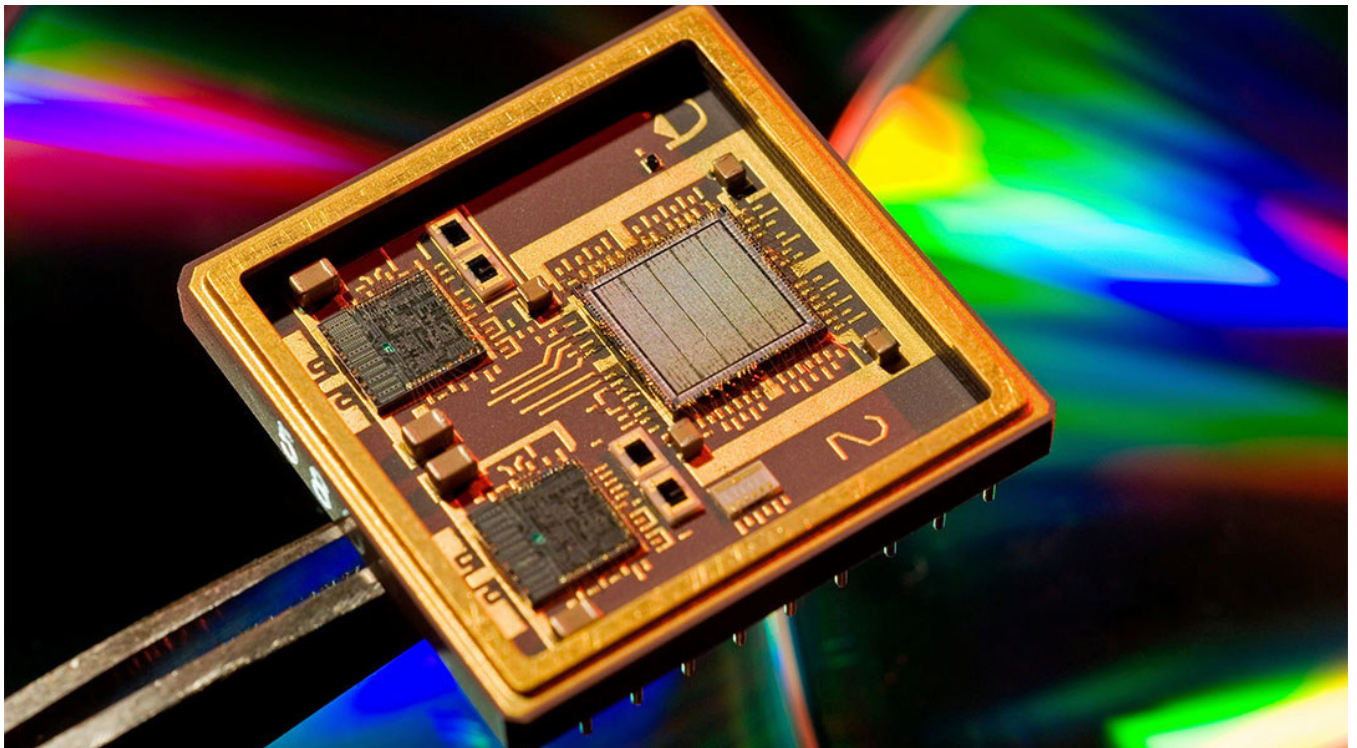
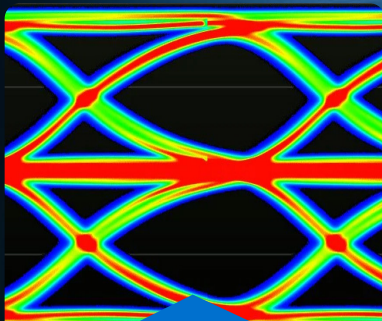


Figure 1: Ceramic-based multi-chip (system-in-package) module. (Source: PR Newswire)

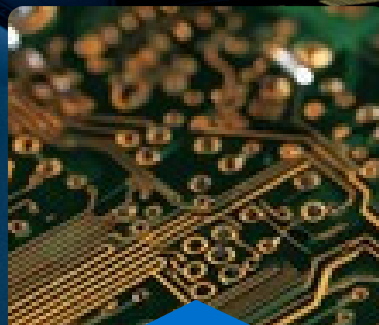
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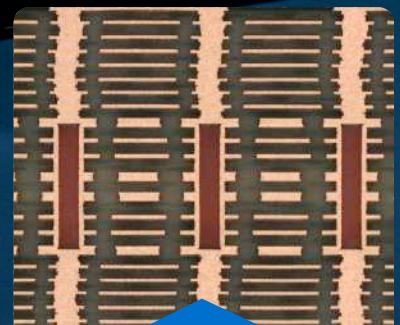
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Excellent Dk/Df
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Ultra-low
X/Y-axis CTE



Proven multi-
lamination reliability

related discrete components onto a common substrate or interposer platform to provide interconnect. The MCM wire-bond assembly sequence begins with die-attach, the placement of the die onto an adhesive deposited on the substrate's surface, with the active surface of the die facing up. Wire-bond processing follows, connecting the terminal sites on the die element to land pattern features located on the substrate's surface. Following wire-bond, the die and wire are coated with a liquid polymer material that, when cured, protects the die and delicate wire interconnects from physical disturbance.

The wire-bond process uses extremely fine-diameter wires (< 40 microns or 0.0015"), typically made of soft metals such as gold, silver, or aluminum.

The classic MCM variations are assembled onto a metallized, ceramic-based substrate (Figure 1), a dielectric material that closely matches the CTE of the silicon die elements and exhibits excellent thermal conductivity.

Other variations may use glass-reinforced FR-4 or polyimide dielectrics as a base platform. The fabrication processes for these materials enable multiple-layer construction and, when employing a semi-additive copper plating process, very high interconnect density at a moderate fabrication cost.

Flip-chip Packaging

As an alternative to wire-bond processing, many companies opted to adopt a process to terminate the die in a face-down orientation known as flip-chip. The face-down process was originally introduced commercially by IBM in the 1960s, using high-lead solder to form a raised terminal at each wire-bond site. The original IBM concept employed very small diameter solder-coated copper spheres placed on the lands originally furnished for wire-bond processing. In 1969, IBM replaced the copper-core spheres with solder-alloy bumps, as shown in Figure 2.

The solder material proved to be more economical, easy to deposit, and compatible with the SMT assembly process:

1. Print or deposit solder paste onto the land pattern.
2. Place components.
3. Employ a heating system to melt the solder to enable the joining of the component terminals to their respective land patterns on the substrate.

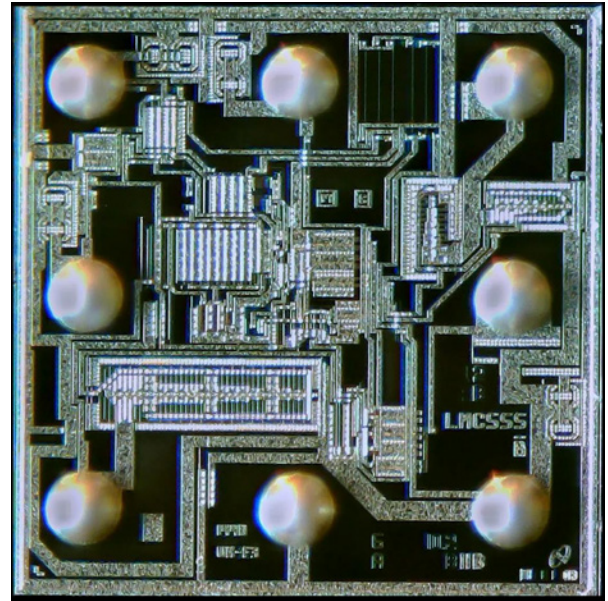


Figure 2: 0.5 mm terminal pitch, flip-chip configured LMC555 CMOS Timer. (Source: Texas Instruments)

As the molten alloy begins to cool during the joining process, the alloy bumps collapse slightly, reducing the standoff height between the die and substrate surface. For the initial solder-bumped die process, IBM adopted C4 (Controlled Collapse Chip Connection) technology.

The increased component density enabled by multiple uncased die elements on a single interposer can significantly reduce the complexity of the host PCB. Close coupling between active devices will minimize power consumption and improve functional performance. It's not uncommon to include discrete passive components (resistors and capacitors) on the same surface using the reflow solder processing for termination noted above.

In flip-chip packaging, the smallest possible package is always the size of the chip itself.

As the industry moved more toward miniaturizing semiconductor packaging in the mid-1990s, standards for chip-size and chip-scale packaging (CSP) began to evolve. Among the categories defined were fine-pitch BGA, die-size BGA, and wafer-level BGA (WLBGA), in which terminal forming occurs while die elements remain in wafer format.

Fan-in Wafer Level Packaging

The WLBGA is a type of BGA in which the finished component's outline is the individual die element. Terminal features required for attaching the semiconductor to a package substrate or circuit board

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are completed while the die elements remain in the wafer-level format. Developers may prepare the original wire-bond sites for direct chip attachment or use an additive copper plating process to redistribute the edge-located wire-bond sites to a more uniform array pattern. The additive metallization process (Figure 3) provides an electrically conductive interface from the wire-bond lands on the die element's perimeter to a wider spaced and more uniform array-configured terminal pattern.

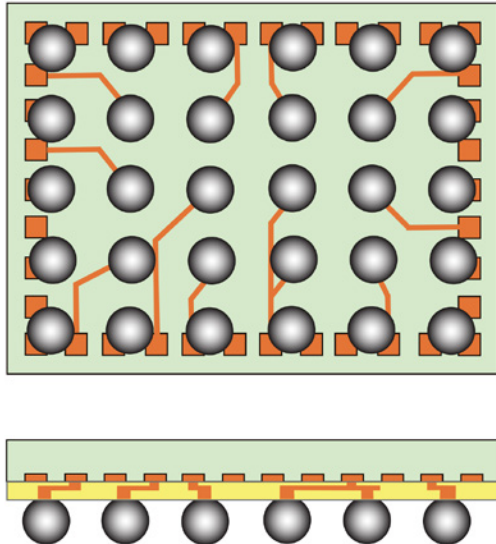


Figure 3: Fan-in wafer-level package terminal array example. (Source: I-Connect007)

Fan-out Wafer Level Package

Fan-out wafer-level BGA represents a major evolutionary direction in packaging technology when the die element is not capable of providing enough area to accommodate all the I/O terminals within the device outline. In preparation for the fan-out WLP, a silicon wafer is developed to redistribute the very fine-pitch bond sites of the die element outward to a wider-array terminal pattern that is more compatible with conventional circuit board fabrication. Microvia through-holes are formed in the silicon (TSV) and Cu-plated to transfer the interconnect on the upper surface to an identical array pattern on the opposite surface.

Individual die elements are then placed face-down onto and joined to the silicon wafer surface. While remaining in the wafer format, the developer will often encapsulate the die with a molding compound to reinforce and protect the die

elements, followed by the formation of terminals (solder balls, microbumps, or micropillars) on the wafer's bottom surface. Finally, marking is applied, and each section is separated (sawing, laser) from the wafer format.

2.5D Package Integration

As semiconductor dies became more functionally complex, and the bump size and pitch continued to shrink, developers needed to adopt higher-density interconnections, moving from the traditional C4 solder ball or bumped terminal to a smaller solid-copper micro-pillar terminal that can support finer pitches and better electrical performance and mechanical stability. A wide range of semiconductor package innovations has already been developed to meet the growing proliferation of ultra-fine-pitch multicore processors and related semiconductors.

System-in-package developers have realized that, instead of the traditional monolithic integration used for earlier, less complex applications, adopting mature, high-yield miniature semiconductor chiplet-configured die to meet system-level criteria is more economical and can significantly reduce development time.

"Chiplets" is where old-school flip-chip packaging reemerges to become new-school technology. A chiplet is an integrated circuit block specifically designed to work with other similar chiplets. That is, by clustering and interconnecting two or more associated heterogeneous or homogeneous semiconductor dies within the confines of a single package outline, closer coupling and the potential for enhanced electrical performance are enabled. By positioning these smaller, less complex functional chiplets in close proximity to the more advanced core processor die, as shown in Figure 4, interconnect distance is minimized and power and ground distribution are optimized.

Overall, the circuit density of the 2.5D interposer is significantly greater than that of the mainstream HDI circuit board. Commercial CAD tools are available to support most very high density (VHD) interposer development. The key enabler for success in chiplet packaging is the interposer. Acting as an intermediary, it furnishes a bridge for electrical signals and thermal management. While the upper surface of the 2.5D interposer accommodates a majority of the semiconductor redistribution and/or

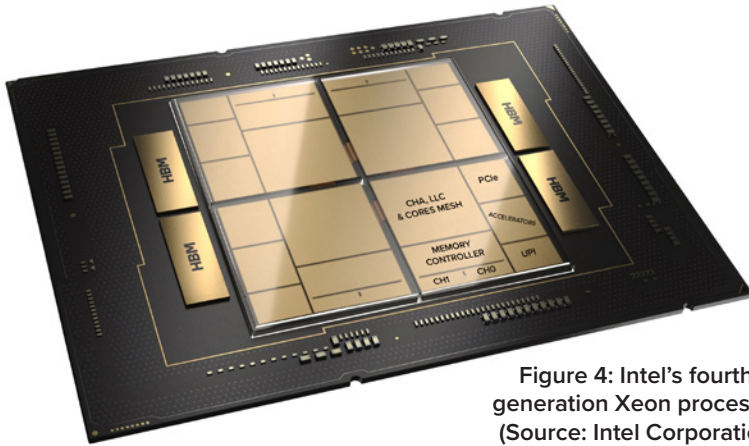


Figure 4: Intel's fourth-generation Xeon processor.
(Source: Intel Corporation)

die-to-die interface, the primary I/O channels and power and ground terminals are located on the bottom surface of the interposer.

Furthermore, separating the pre-tested chiplet support functions from the core processor has improved process efficiency and maximized overall end-product yields; however, the shrinking of terminal size and pitch has become extreme. As the terminal features become narrower, solder process defects increase: opens, shorts, and bridging. Ideally, traditional solder processing can be avoided.

Hybrid Bonding

Hybrid bonding is a heterogeneous or homogeneous direct-bond interconnect technology that enables vertical joining of very fine-pitch semiconductor die-on-die, die-on-wafer, and even wafer-on-wafer without the use of solder or other additive conductive materials between the attached die surfaces. This technology is increasingly used to vertically join a wide range of semiconductor devices, including sensors, memory, and logic die elements. Contrary to all traditional packaging technologies, where the interconnects are joined first, then an underfill is inserted to occupy the space between the interconnects, the direct bond interconnect¹ process (hybrid interconnect) does not use solder or flux and does not require underfill between opposing surfaces.

Die bond interconnect is an enabling low-temperature, low profile die-to-wafer and die-to-die hybrid bonding technology platform. By eliminating the need for copper pillars and underfill, the process enables a dramatically thinner stack as compared to conventional approaches, allowing the stacking of die that are the same or different sizes, processed on fine or

coarse wafer process technology nodes, or manufactured on the same or different wafer sizes while readily scaling down to 1 μm interconnect pitch. The opposing copper terminal surfaces are first aligned to one another and brought together. Alignment for this unique joining process is critical. The developer has stated that the current alignment accuracy of flip-chip bonders is in the 1–10 μm range.

Interconnection is completed using a moderate batch anneal, where the Cu bond pads expand to form a homogeneous metallic interconnect with grain growth across the

bond interface. The chemical bond between oxides is significantly strengthened, ensuring high reliability.

Note: From a historical perspective, integration of multiple functional elements onto a single monolithic platform has become commonplace, although they prove most practical for high-volume applications. Monolithic integrated circuits are electronic circuits that consist of transistors, resistors, and diodes, and their connections, formed on the surface of a single piece of silicon, resulting in a seamless system-level structure. Developing these ASIC products often requires a great deal of engineering resources, monetary commitment, and time. Although many hybrid circuits can be replicated and produced as monolithic integrated circuits, it may not be economically feasible unless large quantities are required in the long term. **I-CONNECT007**

References

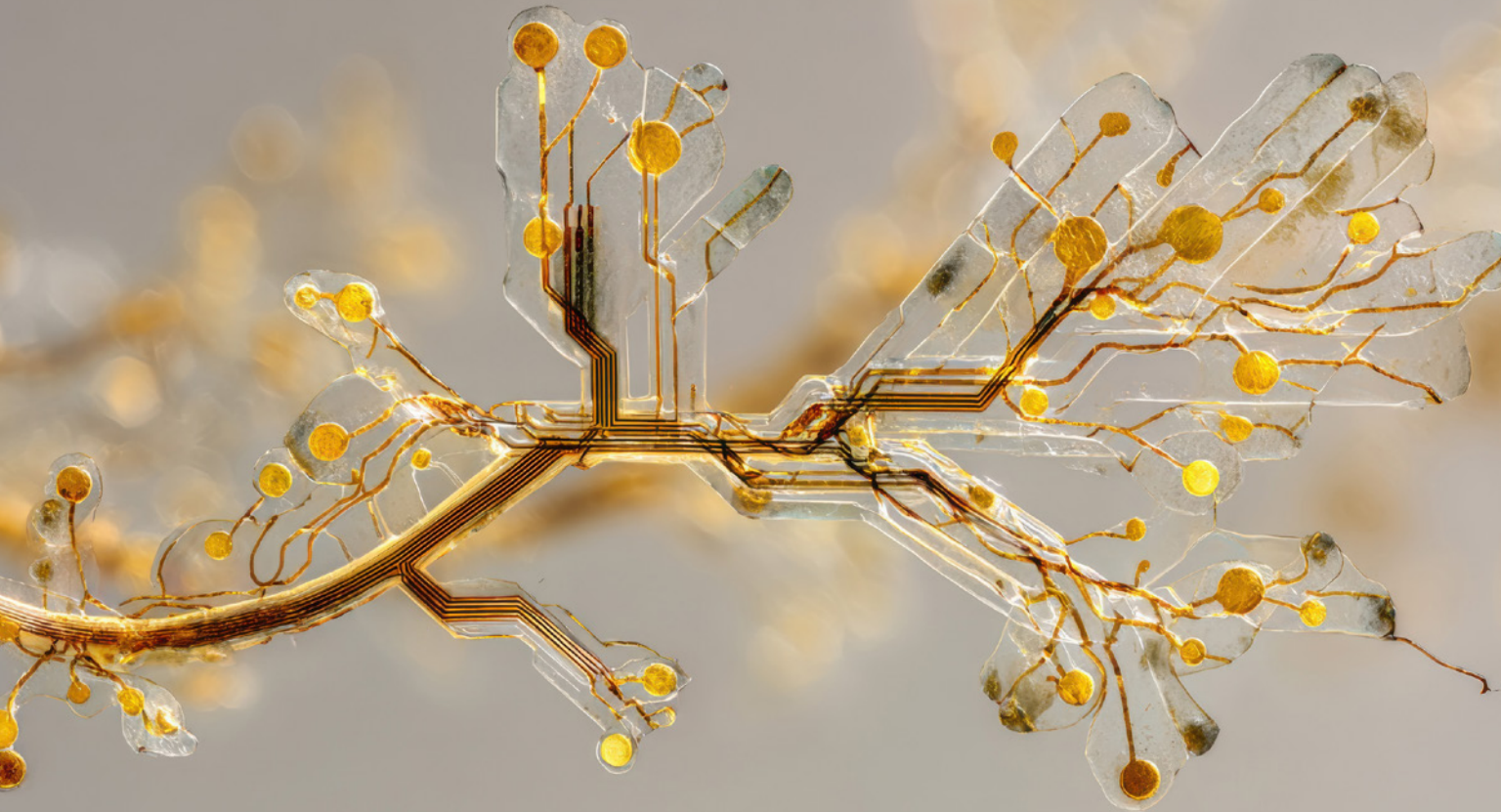
1. In 2015, Tesser Technologies, an Adeia member company in Santa Clara, California, acquired Ziptronix and added the oxide-bond process to its DBI IP portfolio.



Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. He is the author of several books, including *Design Guidelines for Surface*

Mount and Microelectronic Technology. To read past columns, [click here](#).

Rewiring Medical Brain-Machine Communication *With Flex PCBs*



Flex and rigid-flex PCBs are shaping the future through a range of innovative applications, including neural interface arrays that redefine brain-machine communication in the medical field. For decades, scientists and engineers have dreamed of tapping into this electrochemical symphony, and flex PCBs are finally making that dream clinically viable.

What Are Neural Interface Arrays?

The brain has always been the final frontier. Neural interface arrays are the first real map: micro-electrode grids thin enough to drape over living tissue, precise enough to read individual neurons, and powerful enough to let a paralyzed hand move

again. The human brain contains roughly 86 billion neurons, each firing electrical signals that collectively orchestrate everything from conscious thought to involuntary breathing.

Traditional rigid PCBs were never suited for neural applications. The brain is soft, gelatinous, and constantly shifting with heartbeat and respiration. Press a rigid board against cortical tissue and you get mechanical mismatch: micromotion that causes scarring, inflammation, and signal degradation within weeks. The implant effectively blinds itself through its own presence.

Flex PCBs change the equation entirely. Fabricated on polyimide or liquid crystal polymer

substrates as thin as 12 microns, they bend, flex, and conform to brain tissue without creating damaging stress concentrations. The modulus of elasticity of advanced flex materials is orders of magnitude closer to soft tissue than any rigid alternative.

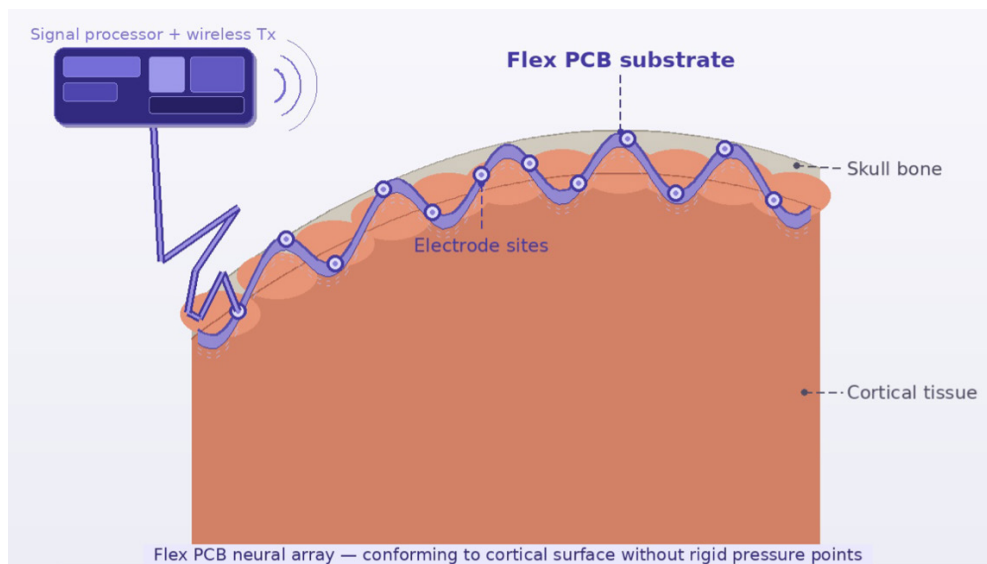
Next Generation Applications

The most advanced neural interface arrays, such as the Utah Array's flexible successors and next-generation electrocorticography (ECoG) grids, use flex PCB platforms to lay hundreds of recording and stimulation electrodes across the brain surface in a gossamer sheet that drapes naturally over cortical folds. Each electrode site communicates through traces no wider than a human hair, routed to an onboard amplifier and wireless transmitter.

Cochlear implants represent the most commercially mature application. A rigid-flex hybrid design places the signal processor behind the ear as a rigid unit while a thin flex electrode array, sometimes called a cochlear lead, threads through the scala tympani of the cochlea, a fluid-filled spiral canal barely 2 millimeters across. The flex array curves with the cochlea's natural geometry rather than fighting it, improving electrode-to-nerve proximity and sound frequency resolution.

Research labs are pushing further. Teams at the University of California, San Diego, and imec have demonstrated flexible neural probes that record from hundreds of individual neurons simultaneously, thin enough to be injected through a hypodermic needle. DARPA's Neural Engineering System Design program has funded work toward a million-electrode cortical interface, an ambition that would be physically impossible without flex PCB technology.

The challenges remain formidable. Biocompatibility over decades-long implant lifetimes requires careful selection of conductor and substrate materials. Hermetic sealing of active electronic compo-



nents against cerebrospinal fluid pushes packaging engineering to its limits, and wireless power delivery through skull and scalp demands extremely efficient circuit design to avoid thermal tissue damage.

Summary

The momentum is unmistakable. As flex PCB manufacturing processes improve, enabling finer traces, higher electrode densities, and better integration of active components, neural interfaces will move from laboratory curiosities to routine clinical tools. For patients with paralysis, epilepsy, depression, or sensory loss, that progress cannot come fast enough. **I-CONNECT007**

Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit*

Designer's Guide to... Fundamentals of RF/Microwave PCBs and Flex and Rigid-Flex Fundamentals. He is the author of *Thermal Management: A Fabricator's Perspective*, *The Printed Circuit Designer's Guide to DFM Essentials*, and *The Companion*



Guide to Flex and Rigid-Flex Fundamentals.

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Transforming PCB Design from *Reactive to Predictive* With Digital Twins

For decades, PCB development has largely followed a sequential process. Design teams create the schematic, develop the layout, fabricate prototypes, perform validation testing, identify problems, revise the design, and repeat the cycle until the product eventually meets specifications. While this approach has historically been accepted as normal, it is increasingly incompatible with modern product

demands, where development speed, quality, and predictability define competitive advantage.

The growing adoption of digital twin methodologies is fundamentally changing this paradigm.

A digital twin is far more than a 3D visualization of a PCB. In the context of PCB design, a digital twin is a connected and intelligent virtual representation of the product that enables engineers to model,

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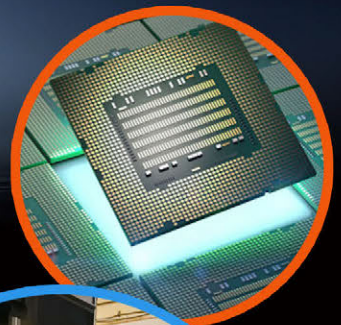
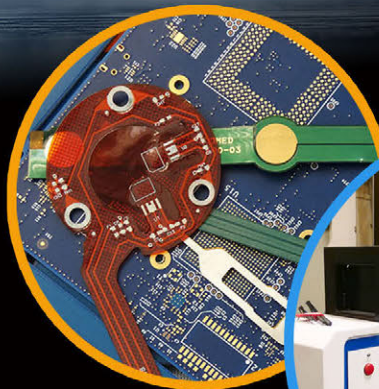


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simulate, validate, and optimize design behavior before physical hardware is built. When properly implemented, the digital twin becomes one of the most powerful engineering tools available to PCB design teams, transforming development from a reactive to a predictive process.

Understanding the Real Value of the Digital Twin

One of the biggest misconceptions surrounding digital twins is that they are primarily mechanical or visualization tools. In reality, the value extends into electrical, thermal, manufacturing, and systems-level engineering.

A PCB digital twin integrates multiple domains into a unified engineering environment, including:

- Electrical connectivity and constraints
- Signal integrity behavior
- Power integrity performance
- Thermal characteristics
- Mechanical fit and enclosure interaction
- Manufacturing considerations
- Assembly process validation
- Reliability analysis
- Lifecycle and configuration management

Rather than waiting for physical prototypes to expose design weaknesses, engineers can evaluate system behavior virtually and make informed decisions earlier in the development cycle. This shift is critically important because the cost of design changes increases exponentially as products move closer to manufacturing. The earlier the issues are identified, the lower the impact on schedule, cost, and product quality.

The Evolution from Verification to Prediction

Traditional PCB development often relies heavily on post-layout verification. Engineers complete the design and then analyze whether it works. Unfortunately, by the time significant issues are discov-

ered, layout decisions are deeply embedded into the design.

Digital twin methodologies fundamentally change the engineering mindset. Instead of asking, “Does the design work?” Engineering teams can ask, “How will the design behave before we build it?”

That distinction is profound. Using integrated simulation and modeling technologies, engineers can predict electrical and physical behavior during the design process itself. This includes evaluating:

- Return path discontinuities
- Impedance discontinuities
- Crosstalk coupling
- Power delivery network (PDN) resonance behavior
- Thermal hotspots
- Electromagnetic interference risks
- Mechanical interference conditions
- Manufacturability concerns

This predictive capability dramatically reduces design iterations and improves first-pass success rates. More importantly, it enables engineering teams to make design decisions with far greater confidence.

Digital Twins and Signal Integrity

As interface speeds climb, SI can no longer be treated as a late-stage validation exercise. The margins are simply too small. Modern high-speed designs demand accurate modeling of interconnect behavior across the entire signal path. The digital twin enables engineers to analyze these interactions continuously throughout development rather than after layout completion.

This includes modeling transmission line behavior, via discontinuities, reference plane transitions, differential pair coupling, timing margins, and reflection and loss mechanisms.

The ability to virtually validate these behaviors before fabrication significantly reduces the risk of discovering major issues during hardware bring-up. Equally important, digital twin methodologies allow designers to evaluate tradeoffs rapidly.



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For example, engineers can compare the electrical impact of back drilling vs. HDI structures, different stackup configurations, alternative routing topologies, material selections, and connector and critical component placements. This allows engineering decisions to be driven by measurable system behavior rather than assumptions or legacy practices.

Power Integrity: A Growing Necessity

PI has become one of the most critical challenges in modern PCB design, particularly with advanced processors, FPGAs, AI accelerators, and high-current applications. Voltage fluctuations that once may have been tolerable can now create catastrophic system instability.

A properly implemented digital twin enables engineers to model the PDN dynamically and evaluate current distribution, voltage ripple, decoupling effectiveness, plane resonance behavior, simultaneous switching noise, DC voltage drop, and transient response.

This provides engineers with the ability to optimize the PDN architecture before hardware fabrication begins. Without this level of predictive analysis, many designs are forced into expensive board spins to correct preventable PI issues.

Bridging the Gap Between Electrical and Mechanical Domains

One of the greatest strengths of the digital twin is its ability to unify traditionally disconnected engineering disciplines. Historically, ECAD and MCAD workflows often operated independently, with integration occurring late in development. This frequently resulted in enclosure conflicts, connector misalignment, airflow issues, and assembly complications.

Digital twin methodologies help eliminate these disconnects by creating a collaborative engineering environment where electrical and mechanical decisions are continuously synchronized. This becomes especially valuable in applications ranging from compact form factors and ruggedized electronics to aerospace and defense electronics, automotive, wearables and medical devices, and high density embedded systems. The result is fewer integration surprises and significantly improved development efficiency.

Manufacturing Awareness Earlier in the Design Process

A digital twin should not end with design validation, but should also extend into manufacturing and assembly considerations. Designing a board that functions electrically but creates manufacturing challenges is no longer acceptable in today's competitive environment.

Modern digital twin workflows enable engineering teams to evaluate:

- Fabrication constraints
- Drill aspect ratios
- Assembly clearances
- Solderability risks
- Component placement accessibility
- Testability
- Yield optimization

This allows manufacturability concerns to be addressed during design creation rather than after fabrication release. In many cases, this capability alone can save organizations significant time and costs.

The Digital Thread: Connecting Data Across the Lifecycle

The true power of a digital twin emerges when it becomes part of a larger digital thread strategy. The digital thread connects engineering data, decisions, simulations, revisions, manufacturing outputs, and lifecycle information into a continuous and traceable ecosystem. Advantages include:

- Improved design traceability
- Better configuration management
- Enhanced reuse of validated IP
- Faster collaboration across teams
- More efficient change management
- Greater product consistency

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of truth throughout the product lifecycle. This becomes increasingly important as designs grow more complex and globally distributed development teams become the norm.

Digital Twins and Engineering Productivity

Perhaps one of the most overlooked benefits of digital twin adoption is the impact on engineering productivity. PCB designers and engineers spend a tremendous amount of time reacting to problems that could have been identified earlier. Every unexpected SI issue, thermal problem, EMI failure, or mechanical conflict introduces delays, redesign effort, and unnecessary engineering churn.

Digital twin methodologies reduce this inefficiency by shifting validation forward into the design process itself. This allows engineers to spend less time debugging preventable issues and more time focusing on innovation and optimization. In some respects, the digital twin acts as an engineering force multiplier.

The Industry Shift Toward Predictive Engineering

The electronics industry is undergoing a broader transformation from experience-driven engineering toward data-driven engineering. That does not diminish the value of engineering expertise. Rather, it enhances it.

The most effective engineering organizations will combine deep domain knowledge with predictive digital technologies to accelerate development while improving product quality and reliability. Digital twins

are rapidly becoming a foundational component of this transformation.

Organizations that rely solely on traditional build-test-fix methodologies may find themselves increasingly constrained by schedule pressure, escalating costs, and growing system complexity. Conversely, companies embracing predictive engineering methodologies will be positioned to develop products faster, with greater confidence and fewer costly surprises.

Final Thoughts

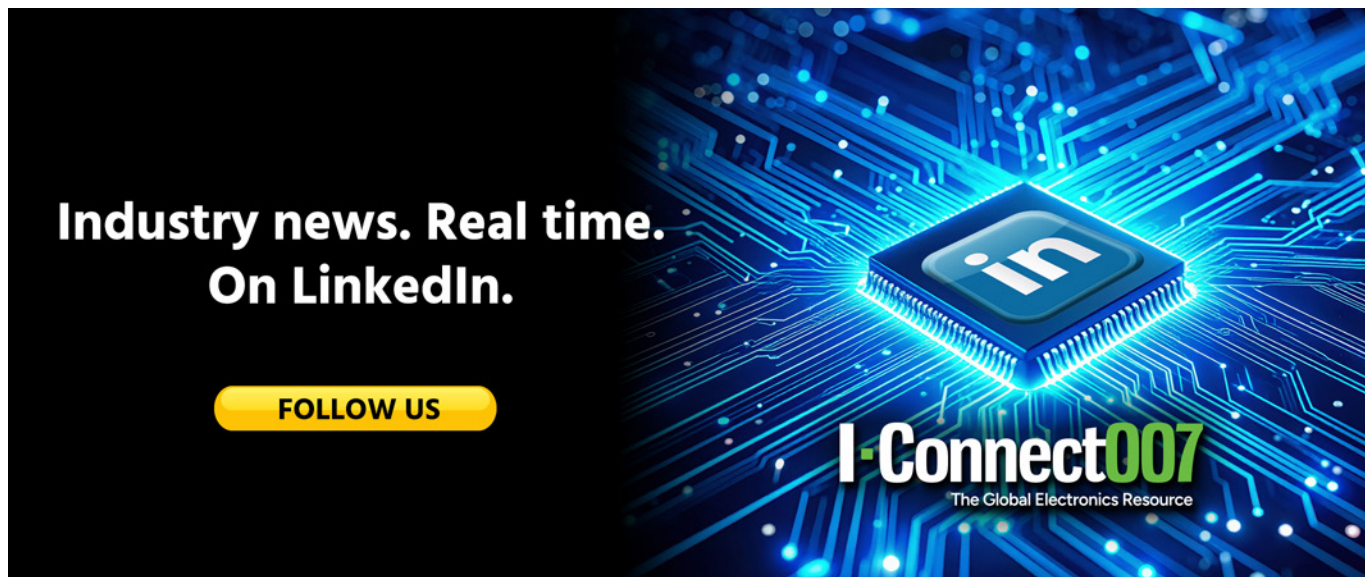
The PCB industry has historically excelled at solving problems after they occur. The digital twin enables something far more powerful: preventing those problems from occurring in the first place. The digital twin is an essential engineering capability for modern complex electronics, where the ability to model, simulate, validate, and optimize designs virtually, before fabrication, will become increasingly indispensable.

The transition from reactive engineering to predictive engineering may ultimately become one of the most important shifts in the future of PCB design.

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Stephen V. Chavez is principal technical product marketing manager at Siemens EDA and chair of PCEA.

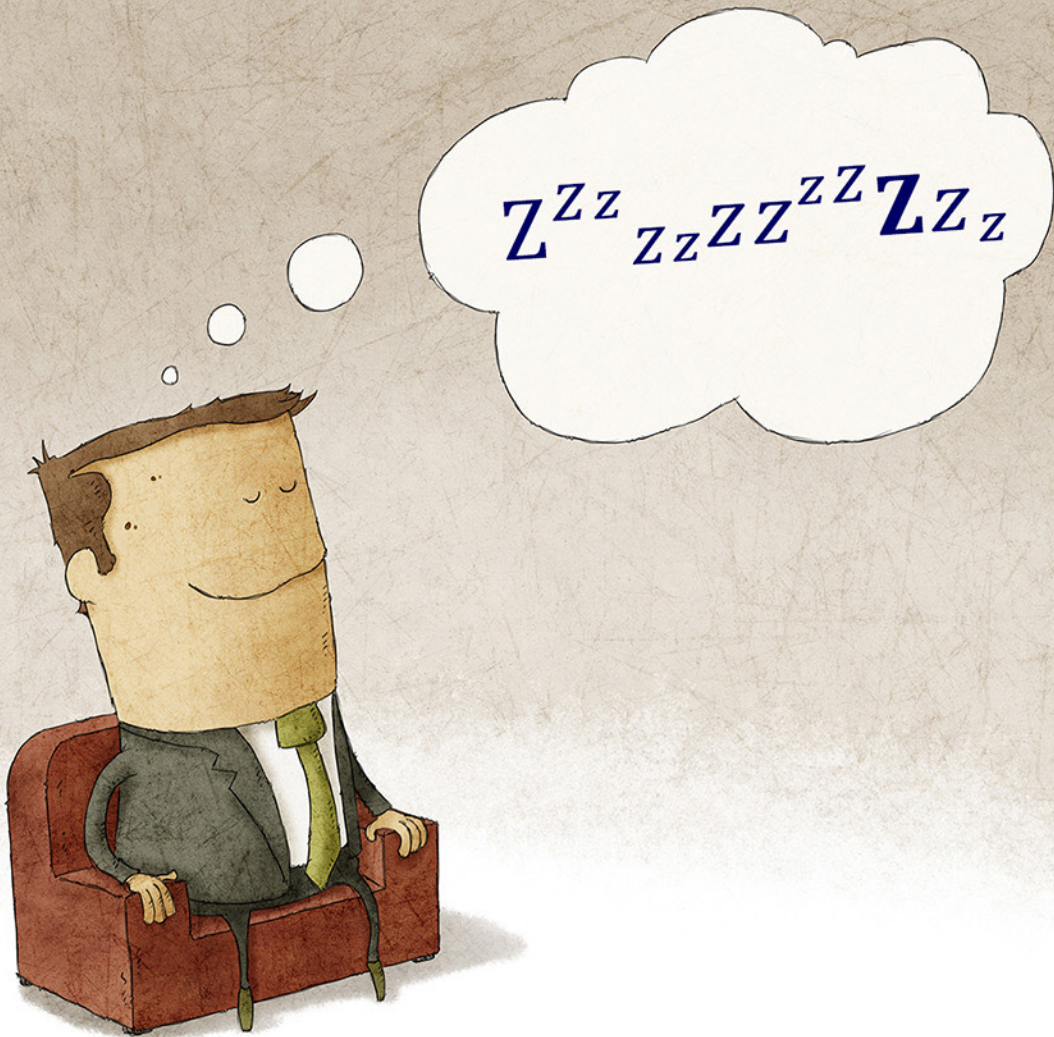
A promotional graphic for LinkedIn. The background is a dark blue field with glowing blue circuit traces. In the center is a glowing blue square with the white LinkedIn 'in' logo. To the left, white text reads 'Industry news. Real time. On LinkedIn.' Below this is a yellow button with the text 'FOLLOW US'. In the bottom right corner, the 'I-Connect007' logo is displayed in white and green, with the tagline 'The Global Electronics Resource' underneath it.

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PCB Manufacturing Focused on Value



BY MATT STEVENSON, ASC SUNSTONE CIRCUITS

PCB manufacturing has become more complex, not only to meet the growing need for more advanced, smaller boards, but also to address supply chain disruptions and uncertainty about the cost of critical raw materials. This environment makes it harder for our customers, too. Relatively straightforward decisions about choosing a PCB manufacturer have become more challenging.

Established paradigms, such as “offshore manufacturing is cheaper,” are not as reliable as they once were. A variety of risk factors, including trade policy and shortages of critical supplies, have added uncertainty. The seemingly simple value equation of “function plus quality divided by cost” now includes more variables, greater risk, and potential hidden costs.

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As manufacturers, we need to up our game to deliver value to our customers.

Total value management (TVM) is an approach to the quality-versus-cost balancing act that integrates components of total quality management (TQM) and Lean manufacturing. Like those other methodologies, TVM prizes customer focus, continuous improvement, and employee empowerment.

TVM applies all these qualities and improvement-focused concepts to PCB production. A TVM solution partner is collaborative, innovative, nimble, and resourceful. They will be able to help you formulate the best path forward for your PCB prototyping and manufacturing, be it domestic or offshore.

For customers facing increased decision-making complexity and evolving financial risk and reward models, it helps to focus on traditional value propositions:

- More effective, easier communication with the fabricator
- Reliable, dependable delivery
- Higher yield, better quality
- Smooth, faster production
- Reduced risk

Value at Each Stage of Production

Manufacturing value starts before the first blank board begins its journey through the production facility and continues well after the final products are shipped. The first opportunity for manufacturers to deliver value is at the initial point of contact, when many customers are addressing the global question: Where should I manufacture?

Providers of both domestic and overseas manufacturing solutions are well-positioned to objectively consult with customers to solve the domestic vs. offshore equation, an equation more complicated than simply calculating the per-unit pricing. When you factor in yield, reliability, and durability, domestic PCB manufacturing can often be the most cost-effective choice even for higher volume projects. You have to identify variables and run all the numbers to find out.

With larger production volumes, even modest per-unit savings often associated with offshore production can appear attractive on the surface. However, those savings paint only half the picture. Our experience tells us that less easily quantifiable cost drivers pose greater obstacles to offshoring than just volatile import taxes and port delays. It is the value equation that tells the story.

Is the risk associated with a globally sprawling supply chain offset by the value of slightly cheaper boards? Can you cost-effectively warehouse a sufficient supply to be resilient? Can delays and cost variances from shipping, tariffs, and transport fees be absorbed? How much will a lower yield or quality issues affect the cost savings?

These are the indirect costs associated with offshoring that may minimize or even eliminate potential savings. It still might be the right decision to go overseas, but a value-based partner can work with you to see clearly which path brings the most value.

Best Practices for Total Value Manufacturing

Total value—delivered to the customer through support, on-time delivery, quality boards, and high yield—is how manufacturers can support customer needs for PCB production in all circumstances. Its foundation is quality.

Schedule Adherence

It does not matter how good the boards are if they are not available for production of the electronic device they were built for. If a manufacturer ships an average of 1,000 orders per day, the difference between 95% and 97% on-time delivery annualizes to over 5,000 additional late shipments per year. Every late delivery has a cost. Because it affects each customer's bottom line, manufacturers focus on total value work every day to improve their on-time delivery rate.

Design Adherence

The key question facing every designer: Can the manufacturer build the board I designed?

Designs with manufacturability issues can cause production delays and drive up costs. Design adherence helps the design team concentrate on

the behavior of the design during prototyping and debugging, because the PCB manufacturer built what the design team specified.

The standard or widely accepted RMA rate for PCB manufacturers is roughly 2%. Fabricators who strive to provide TVM maintain a 1% RMA rate.

Responsiveness

PCB manufacturing is a collaborative process. A good partner helps the design team keep revision cycles to a minimum during prototyping and move the project along as fast as possible. Responsiveness is key to achieving this goal. Design teams are often working on tight project deadlines. To get clarity, they need prompt, reliable access to their fabricator.

A value-focused manufacturer will provide ready, constant access to experts who speak the language of design and product. They will do so with customer service phone call wait time measured in seconds, not minutes.

Yield

Production yield levels are a key leading indicator for ongoing service levels during the product's life-

cycle. Sound production processes, coupled with deep manufacturing expertise, a focus on quality, and a commitment to continuous improvement, produce higher yields.

Partnering With a Total Solution Provider

When a PCB manufacturing partner has a deep-rooted cultural value on quality and working together with customers, the result is accurate, efficient, and speedy fulfillment of orders, no matter the project, the factory, or the scale. Customers benefit from reduced decision-making complexity during pre-production, greater transparency throughout each phase of manufacturing, and high-quality boards.



Matt Stevenson is vice president and general manager of ASC Sunstone Circuits. Matt is also the author of *The Printed Circuit Designer's Guide to... Designing for Reality* To read past columns, [click here](#).

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Human Resources Business Partner

The HR Business Partner supports key HR functions including recruiting, onboarding, training, employee engagement, legal compliance and employee relations. The ideal candidate is hands-on, employee-focused, and comfortable partnering closely with production leadership and employees on the manufacturing floor.

This role manages full recruiting cycle, leads new hire onboarding, assists with benefits administration and open enrollment, ensures compliance with federal and state laws, and serves as a trusted resource for employee questions and support.

Facilities Technician

The Facility Technician is responsible for maintaining the safety, reliability, and operational readiness of facility infrastructure and supporting equipment in a manufacturing environment serving the electronics and semiconductor industries. This role is hands-on and highly collaborative, supporting daily operations, preventive maintenance, contractor oversight, and new facility integration activities.

The ideal candidate is technically versatile (machining/fabrication, electrical, plumbing), safety-minded, and comfortable working in a regulated manufacturing environment, including clean rooms and controlled production spaces.

Join Remtec and contribute to a collaborative culture focused on quality, integrity, and innovation. Learn more and apply below.

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Position Overview

We are seeking a Field Service Application Engineer to install, calibrate, and service advanced PV and PCB manufacturing equipment at customer sites.

Responsibilities

Install and commission PV and PCB machinery, including mechanical assembly, electrical wiring, and software configuration. Perform precision calibration and performance testing using diagnostic tools. Troubleshoot mechanical, electrical, and software issues on-site. Train customers on equipment operation, maintenance, and safety procedures. Maintain service documentation, interpret technical drawings, and ensure compliance with safety and PPE requirements.

Qualifications

Strong knowledge of electronics and mechatronics, with hands-on experience installing and servicing industrial equipment. Proficiency in diagnostics, calibration, and pneumatic and hydraulic systems. Familiarity with PCB lamination press systems preferred. Strong problem-solving skills and ability to work independently in field environments.

Education & Experience

Associate's degree or equivalent experience; 1–3 years of relevant experience. Valid driver's license, passport, and willingness to travel frequently, including internationally.

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Candidates must have:

- 10+ years in electronics manufacturing
- IPC certification (current or past)
- Bachelor's degree or equivalent
- Strong communication, teaching, and organizational skills
- A practical, problem-solving mindset and commitment to student success

You'll deliver hands-on demonstrations, maintain a positive learning environment, and stay current on industry trends.

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Sr. Test Engineer (STE-MD)

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

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The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

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Quality Assurance Specialist—Bare Board PCB Manufacturing

Accurate Circuit Engineering seeks an organized, technically proficient Quality Assurance Specialist dedicated to bare board PCB production. You will champion compliance with industry standards, lead internal audits, manage certifications, and drive continuous improvement based on product performance data and customer feedback.

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- **Standards Compliance & Certification:** Enforce IPCA600, IPC6012 (CIS/CIT preferred), and ISO 9001 quality standards throughout fabrication
- **Internal Process Auditing:** Conduct scheduled and ad hoc audits of incoming materials, fabrication stages, testing protocols (etest, AOI), and documentation traceability
- **Employee Training & Development:** Create and deliver training programs for inspectors and production staff on IPC standards, quality procedures, and inspection tools to maintain certification
- **Failure Analysis & Corrective Actions:** Investigate nonconforming boards—including internal findings and customer returns/RMAs—analyze root causes, and lead corrective/preventive actions (8D/CAPA)
- **Procedure Optimization:** Analyze quality trends and RMA data to update processes, inspection checklists, and control plans

Qualifications:

- Associate degree or equivalent experience in electronics manufacturing
- 3+ years in bare board PCB QA, with IPCA600/ CIS and IPC6012 certification
- Strong auditing, training, documentation, and cross-functional collaboration skills
- Proficient in rootcause failure analysis

Join us to ensure rigorous compliance, elevate fabrication quality, and continuously improve manufacturing standards.

Contact brandon@ace-pcb.com and James@ace-pcb.com to apply.

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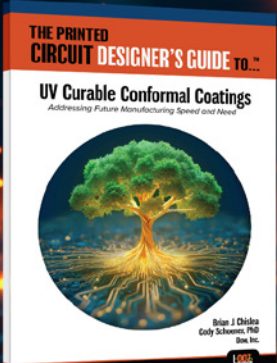
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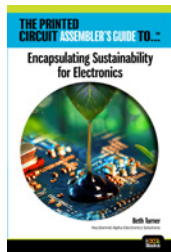
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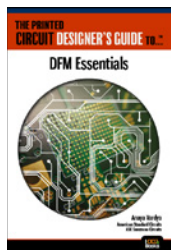
Look Inside



Encapsulating Sustainability for Electronics

by Beth Turner, MacDermid Alpha Electronics Solutions

This book discusses the growing demand for sustainable solutions in the market and highlights examples of bio-based resins and the demand from emerging technologies. [Read it now!](#)

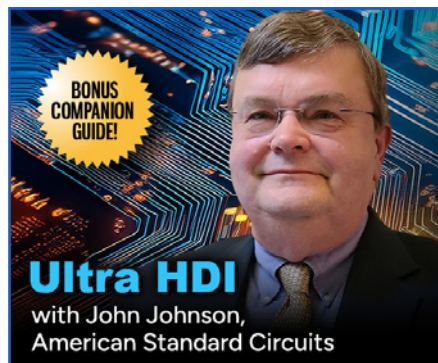


DFM Essentials

by Anaya Vardya, American Standard Circuits, ASC Sunstone Circuits

One of the biggest challenges facing printed circuit board designers is not understanding the cost drivers in the PCB manufacturing process, particularly the manufacturing of advanced technology PCBs. The guidelines offered in this book are based on both ASC recommendations and IPC standards. [Download your copy today.](#)

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