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Signal Integrity & Metallization

Signal integrity and additive manufacturing, particularly metallization, are hot topics in PCB design and fabrication. PCB layouts are carefully engineered to achieve specific electrical and power performance targets. Once the design moves into fabrication, metallization—particularly the plating of traces to precise specifications—is what enables the intended signal integrity to be realized.

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Additive Processes, Signal Consequences

BY MARCY LARONT, I-CONNECT007

Signal integrity and additive manufacturing, particularly in metallization, are defining themes in modern PCB design and fabrication. PCB layouts are meticulously engineered systems designed to meet strict electrical and power performance targets. However, achieving those targets does not end at the design stage. Once a design enters fabrication, metallization processes—the precise plating of conductive traces—play a critical role in ensuring that signal speed, reliability, and integrity are achieved in the final physical board.

As increasingly smaller electronic devices become more complex and performant, maintaining signal integrity becomes significantly more challenging. Higher data rates, tighter geometries, and denser routing all introduce new risks, from impedance mismatches to electromagnetic interference.

The industry is increasingly turning to modified semi-additive processing (mSAP) and semi-additive processing (SAP) to address these challenges, as these advanced approaches allow for finer feature definition, improved line-edge precision, and tighter tolerances than traditional subtractive methods. The result is better control over electrical performance and a pathway to supporting next-generation applications. At the same time, these technologies represent a fundamental shift for PCB fabricators because they require new materials, processes, and ways of thinking about production.

This issue of *I-Connect007 Magazine* explores these developments in depth, beginning with contributions from PCB007 authors focused on additive technologies. Columnist Don Ball provides a foundational overview, starting with conventional electroplating methods and progressing through mSAP and SAP processes. He examines how these approaches influence etching performance and highlights which techniques have proven effective and which have not. Expanding on the chemistry of metallization, Melbs LeMieux of

Electroninks offers insight into complex metal inks and discusses how his company is rethinking materials at the molecular level.

Carmichael Gugliotto of MacDermid Alpha Electronics Solutions writes about the importance of direct metallization as a key enabler of advanced PCB manufacturing. He cites the growing demands placed on PCBs and substrates used in AI infrastructure and high-performance computing, where reliability and performance margins are increasingly tight. The engineering team at MKS' Atotech addresses enhanced mSAP processes with a focus on microvia reliability, an area of critical concern in high density interconnect (HDI) designs, while also considering manufacturing efficiency. Notion Systems rounds out the semi-additive discussion with its inkjet solder mask technology, highlighting how digital deposition methods can improve precision and flexibility in PCB production.

Our Design007 contributors tackle the evolving challenges of signal integrity. Stephen V. Chavez writes about return-path discontinuities, while Kristin Moyer addresses common-mode and differential-mode noise in routing and signal integrity, as well as strategies for ensuring signal survival in increasingly hostile electromagnetic environments.

In his column, Barry Olney succinctly captures the shift in design philosophy: "Modern PCB design is no longer just about routing signals but about engineering transmission lines, maintaining continuous return paths, and managing resonant structures within multilayer boards." Columnist John Watson reinforces this perspective by urging designers to move beyond schematic-level thinking and consider the electromagnetic fields surrounding traces, dispelling the notion that signal integrity is somehow "black magic."

Meanwhile, Kelly Dack explores how AI-driven design tools are pushing boundaries, transforming signal integrity from a niche concern into a decisive factor in determining product success, and shares a list of PCB designers who have had the most influence on him and the industry.

This issue also features a range of forward-looking discussions tied to advanced manufacturing. Anaya Vardya focuses on integrating flex circuits into advanced packaging solutions. A new contributor, Flexiramics, introduces innovative approaches to reinforcement materials for electronic packaging. Mike Carano contributes insights into the role of organic solderability preservatives (OSPs) in advanced packaging and where they provide the most value. Chandra Gupta of Remtec examines RF design and integration, emphasizing that true performance gains often occur at the interfaces, where components either work in harmony or conflict.

Additional design-focused content includes a conversation between Paul Cooke and Kelly Dack on designing for reliability, as well as Matt Stevenson's overview of conductive via fill and what designers need to understand. Tracy Riggan interviews the leaders of the IPC-2581 Consortium about progress toward replacing Gerber files with a more secure and comprehensive data standard.

Happy Holden bridges the gap between design and fabrication by reviewing the growing role of digital twins, which integrate design and manufacturing data to improve outcomes, particularly as access to experienced manufacturing experts declines. In PCB fabrication, Richard Nichols continues his ongoing exploration of zero liquid discharge. We spotlight a roundtable discussion on cybersecurity and CMMC certification, and I explore the implications of the e-glass shortage in the AI era.

Together, these perspectives highlight, once again, that our industry is in transition, where innovation in materials, processes, and design methodologies is essential to meeting the demands of increasingly complex electronics systems.

I-CONNECT007

Marcy LaRont is the managing editor of I-*Connect007 Magazine* and executive director of IPC Publishing Group. Marcy started her career in PCBs in 1993 and brings a wide array of business experience and perspective to *I-Connect007.* To contact Marcy, click here.

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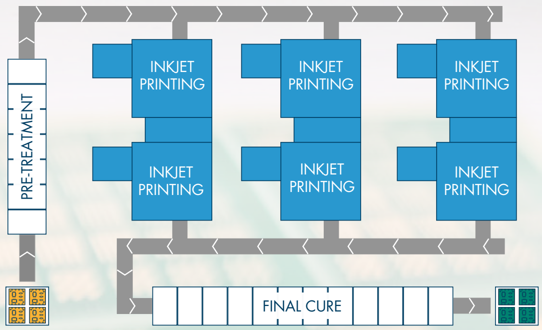

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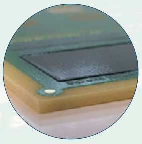
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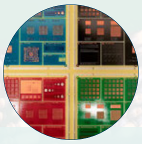
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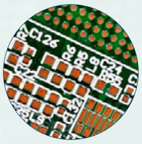
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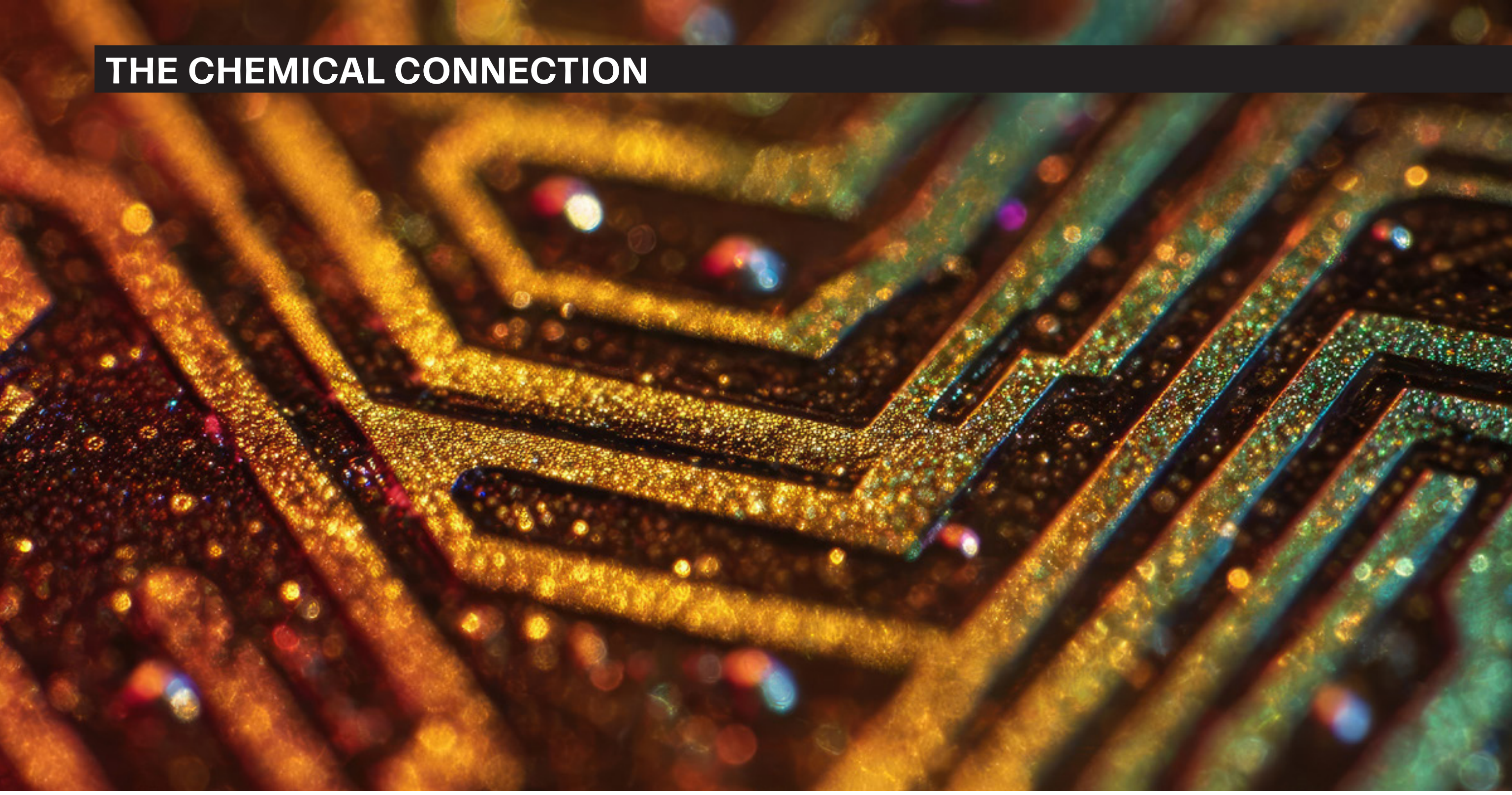


The Consequences of Additive Metallizing *on Etching Steps*

BY DON BALL, CHEMCUT

This month, I'm taking another look at additive manufacturing. What does mSAP, SAP, and additive metallizing (plating) look like in today's advanced PCB fabrication? I must confess I don't have a lot of insight, as my whole career has been devoted to removing copper from panel surfaces in even and controlled ways, and not to putting copper back on the panel. However, at some point in the additive process, especially in additive plating, copper must be removed from between the conducting surfaces to complete the circuits. Here, I can address some of the consequences of additive metallizing on subsequent etching steps.

Traditional additive metallization, or pattern plating, has been the primary way to get taller conductor heights for higher current capacities and less heat generation than is possible with just subtractive etching. The traditional process starts with a thin laminated foil (one-quarter or one-eighth ounce), then laminate and develop a plating resist with the desired circuit layout. The panel is put in an electroplating bath, and copper is plated until the desired circuit height is reached, followed by a solder or tin coating to serve as an etch resist. The base foil is etched with an alkaline etchant, leaving behind the desired circuit design.

A more recent technique is to sputter or flash plate an even thinner base copper, usually 2 to 4 microns, and electroplate the circuit lines to the desired thickness, but with no tin or solder. Then the panel goes through a flash etch in an acid etchant (usually cupric) at such a speed that etches away the base copper while having a minimal effect on the plated circuit lines.

Obviously, before the base copper can be etched away, the plating resist must be removed, and this is where problems can arise. Getting even plating over a large format panel, with several of these large format panels on a vertical flight bar, is difficult at best. It is not uncommon for areas of the

panels to be over-plated, trapping resist under the over-plated areas that interfere with the etching of the base copper.

The first thought is to increase spray pressures in both the stripper module and rinses, but it turns out that this is not as simple as it seems. One customer was using a power wash at 400 psi after stripping and requested a 400-psi rinse after the strip chamber for their proposed new stripper. This would involve special high-pressure pumps with a very high flow rate, stainless steel plumbing, very good filtration (it would have to have a recirculating sump to keep water consumption at a reasonable level), etc. When all is said and done, it is very expensive. We decided to put together a 400-psi test stand to get an idea of what would be involved in actually putting one of these things together, which turned out to be a good idea.

We got some test panels from the customer, and to my surprise, the 400-psi rinse seemed to have no effect whatsoever. Somewhat apprehensively, I stuck my hand under the spray and felt hardly any impact even though the pressure gauges were reading 400 psi. To achieve 400 psi with the pump they had available, our engineers kept reducing the nozzle openings until they reached 400 psi. Unfortunately, the opening size was so small that spray droplets were broken up into such tiny droplets that they had hardly any impact force at all, even at 400 psi.

We had invented a "velvet touch" high pressure spray system. A bigger pump was obtained, adding nozzles with a more reasonable opening size, and found that the customers' objectives could be reached with a 150-psi rinse—a much more reasonable proposition, but still requiring more effort than expected.

Another unanticipated consequence occurred when people started flash etching to remove very thin base copper from their boards. It should have been a simple proposition, a quick spray of etchant to remove two or three microns of base copper and on to the next process. However, we started getting reports of residues of base copper left on the panel in long strips, like tiger stripes. This did not occur on their normal copper weight panels (1-ounce, half-ounce, etc.), just their flash etch panels run at high conveyor speeds, so it was not due to clogged nozzles or misaligned conveyor wheels.

Measurements showed that the distance between the stripes was about the same as the distance between the spray tubes, so we speculated that the conveyor speed needed for the flash etch might result in a harmonic being reached with the spray tube oscillation rate. Most etchers and developers use some type of spray tube oscillation to sweep etch solution back and forth across the board surface as it travels through the etch chamber.

At the end of each oscillation stroke, even though it doesn't look like it, the tube must decelerate to a stop, then accelerate in the opposite direction. There is a brief time when the tube is stopped and, at this moment, the area directly under the spray gets a little more etch time. At the oscillation rates and conveyor speeds used for normal copper weight boards, these areas tend to even out as the panel goes through the etcher, as a different part of the panel is below the spray tube at the end of each oscillation stroke.

It is conceivable, however, that at the high conveyor speed needed for flash etching, a harmonic could be reached where the same part of the panel could be under the spray tube at the end of each oscillation stroke and that little bit of extra etching could accumulate and cause striping. This proved to be the case when altering the oscillation speed by 25% in either direction caused the tiger stripes to go away.

I doubt there is anyone who could have anticipated a harmonic relationship between conveyor speed and etcher oscillation rate when flash etching was first thought of (anyone who could have thought of it would probably not be working in the PCB business anyway). So, when taking another look at additive manufacturing, keep in mind that there will be consequences further down the process line. **I-CONNECT007**

Don Ball is a process engineer at Chemcut. To read past columns or contact Ball, click here.

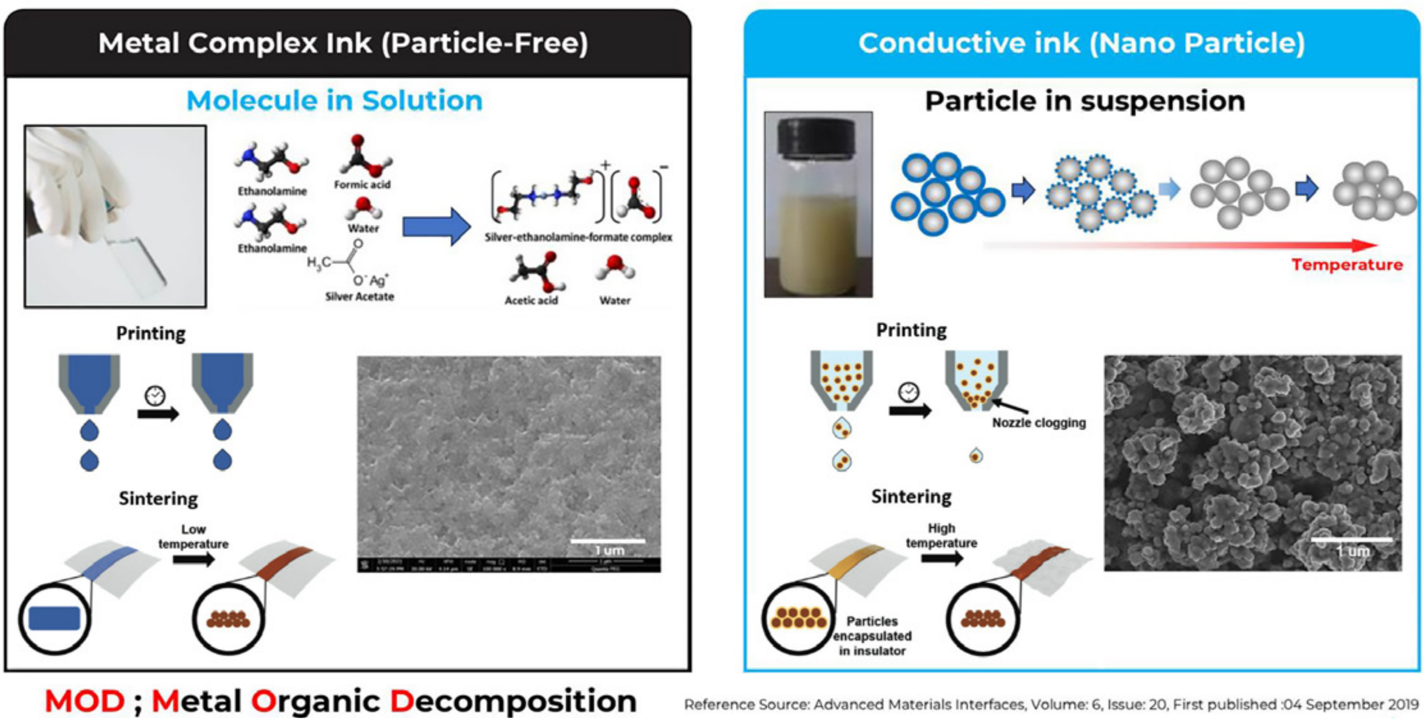
BY MARCY LARONT, I-CONNECT007

Rewriting Metallization ONE INK AT A TIME

Additive manufacturing has long promised to reshape how electronics are built, but that promise has remained just out of reach for many in the PCB industry who are limited by materials, performance trade-offs, and real-world manufacturability. Electroninks aims to change that equation by rethinking metallization at the chemical level by developing metal-complex inks that challenge established approaches and open new possibilities for advanced packaging, interconnects, and beyond. Co-founder and President Melbs LeMieux discusses the evolution of the technology, the realities of bringing new materials to market, and where additive manufacturing may finally begin to deliver on its potential.

Marcy LaRont: Melbs, please tell us a little bit about yourself and how Electroninks got started.

Melbs LeMieux: I grew up in Michigan and later earned my PhD in Materials Science from Iowa State, followed by a postdoc in chemical engineering at Stanford. Around 2013, I connected with our co-founder and CEO, Brett Walker. He was bringing some really strong chemistry to the table, and



This simplified illustration depicts printing, sintering processes for both types of ink, possible problems that may arise during printing (nozzle clogging of particle ink), and sintering (substrate degeneration upon sintering at high temperature for particle ink).

I had already spent time scaling metallization technologies commercially, so there was a natural fit.

From there, the idea behind Electroninks really took shape. We saw an opportunity to develop materials that could be deposited in a much more agile, additive way, especially for semiconductor metallization, advanced packaging, substrates, and PCBs. That combination of chemistry and manufacturability became the foundation for the company.


Melbs LeMieux

Let's talk about your product, which is described as "particle-free metal complex inks." Is that a fundamental shift from nanoparticle-based systems? Please explain its significance.

"Particle-free" is really more of a marketing term. Technically, these are metal complex conductive inks. With nanoparticle inks, the particles have to fuse together, and to keep them stable in solution, you need organic components to prevent agglomeration. The challenge is those organics remain in the printed film, and unless you cure at high temperatures, they can limit performance and reliability.

What we've done is take precursor chemistries—similar to what's used in ALD (atomic layer deposition) or CVD (chemical vapor deposition)—and adapt them into a printable ink. That allows you to metallize surfaces without vacuum processing or high-temperature deposition.

The key advantage is that these metal complex inks don't rely on those organic stabilizers, so the resulting film behaves much more like a pure metal layer, similar to what you'd see with electroless deposition or PVD (physical vapor deposition) in semiconductor backend processes.

Is it a purer ink with better metallization because of it, and is that why you can reach 90% bulk metal? Does it reach a higher concentration without other additives?

Yes, but the overall performance depends upon many other process factors. In general, we can reach higher levels of conductivity and reliability at the same, or even lower, curing temperatures. That is the best way to look at it. They offer lower, faster-curing profiles than conventional nanoparticle links.

In the past, Electroninks has given presentations aboutmetal complex inks, but are you also talking about equipment in your suite of solutions for additive manufacturing?

Yes, we partner with many printing companies, including spray coaters, inkjet, and aerosol jet companies. We make sure our materials are compatible with their tools, and then customers can have a full solution with the tooling and inks. There are a few integrators that pull it all together. Primarily, our customers will be the OSATs or the IDMs, but you know the story: OSATs and IDMs may not work well with ink/materials companies directly. They need total solutions, someone to tie everything together.

Will you talk about a couple of your process platforms: Circuit Jet and Circuit Shield?

Circuit Shield is the trademark name for the silver metal-complex ink used in our EMI shielding solution. Circuit Jet is our all-in-one, standalone PCB printer, now marketed to the defense and aerospace industry. It's a standalone, not a production line. It's used to make or repair specialized boards.

Everything you're doing seems like a natural evolution, but was there a specific impetus that led to creating a printer?

The company started with CircuitScribe, a kit that helps students learn the basics of electronics—the breadboard back in our day. Along similar lines, CircuitScribe uses a conductive ink pen to help teach the basics of electronics. So, at our core, we've always looked to build products and have a consumer-facing business. The next step up was Circuit Jet. Originally, the idea was a very basic printer for DIY printing of simple circuits and boards. However, some customers picked it up and asked us to build a printer specifically capable of handling advanced aerospace and

defense boards, so we have focused on that industrial market with this product, rather than direct to consumer.

The very best way to get into having an equipment line is when your customers ask you to do it.
That's right, because it wasn't our expertise and we didn't originally set out to do this technology, but it has grown into a powerful standalone system, with capabilities unmatched here domestically.

How did you originally begin to work with your customers? What does that partnership look like?
It boils down to finding some early champion customers, ones willing to spend time working with us, because they see the value and differentiation this technology can provide. Once you reach a critical mass of champion customers, you take things to a commercial level. It's tough because it's genuinely new technology, and you teach your customers as you go. We've traveled the world over the past six years, focused on educating the market, and now we have trust and some understanding of the technology. Metal complex inks are just now starting to reach the level of mainstream commercialization.

Are education and awareness the hardest and longest parts of the cycle?
Yes, but it comes down to two key elements: Does it provide new functionality, and does it break down a brick wall that customers are hitting? What problem does it solve? You don't want to be just a me-too product, but something that moves the needle on performance and works from a cost modeling standpoint.

Bringing new materials to market is obviously difficult, but we're in a very exciting space. We're entrepreneurs who want to bring new technology forward, and are driven by wanting to build new economic ecosystems.

Tell me about the silver metal ink for EMI shielding.
Our silver product line is very mature at this point, with 12 to 15 commercial ink products and two systems based on either different deposition methods or the different substrates and stackups they go into.

We also have gold, platinum, nickel, palladium, and copper metal-complex inks. Currently, we're focusing on copper, which customers like for various reasons: It's found in many places, and is cost-effective compared to silver, gold, platinum, and palladium. Obviously, copper has certain oxidation issues, but we've developed two distinct copper technologies, one of which is compatible with an ambient environment. To print copper and achieve good electronic performance at ambient temperature is a big win. The other copper technology we developed is better suited to a nitrogen-based environment, which is commonly used in assembly processes.

An initial focus for copper is on metallizing surfaces and vias with it to create a very thin seed layer that can be plated on directly. That's an important use case right now.

Additive technology offers sustainability benefits, with inherently lower waste and fewer processes, while achieving very fine features. But is sustainability a big selling point?
Certainly, OEMs want to tell that story about their supply chain. It's becoming increasingly important at the highest levels of manufacturing. People will talk about the importance of water and energy usage and even CapEx, but the manufacturing footprint is also a big issue. Additive tools generally have a much smaller factory footprint and offer flexibility in repositioning the line. Typically, a standard line is dedicated to a single technology, but with additive, you can change the printing or deposition patterns. You can reposition an additive line for different products relatively quickly. That eases the burden and the risk of a factory buying a specific tool set for a specific product that might go out to production in a relatively short timeline.

Electroninks has been growing rapidly. What does your global footprint look like today?
Even with the onshoring push, we must still have a very global supply chain to remain competitive. We have a manufacturing site in the Asia Pacific region and one in Delaware. We also have overseas sales offices. We are a company of just 50 people, so it is challenging to operate on a global scale. Our approach has been to choose our locations and our

partners wisely. Right now, we have outlets in the U.S., Taiwan, Korea, Japan, and, most recently, India.

Are you seeing more receptivity or enthusiasm in one region over another, or is it pretty even across the world?

Certainly, the domestic market has picked up in the last five years. But as the single global source for our portfolio of metals and technologies, we're getting interest everywhere.

That is good to hear. Do you see additive technology fitting within the spectrum of electronics and manufacturing several years out?

Obviously, there are different products for different markets, but we also see some growing trends. The first is the need to get around Moore's Law with more 2.5D or 3D IC stacking and advanced chips. The ability to perform additive metallization is becoming increasingly important for 2.5D and 3D architectures.

Another trend is the big partnerships happening in big tech with the hyperscalers and the AI ecosystem. Everyone wants their own custom chip, and for that, you have to understand its end use. The days of common chip types used across different platforms are waning, and you have to understand the application and the ecosystem it's going into. The flexibility and manufacturing capability of additive will become more prominent as a manufacturing method for these high-end, application-specific chips.

Melbs, this has been very interesting. Thank you for taking the time.

You're welcome, Marcy. **I-CONNECT007**

Inkjet Solder Mask: Notion Systems Takes the Mic

BY MARCY LARONT, I-CONNECT007

Additive manufacturing offers clear advantages in material efficiency, process simplification, and design flexibility. By depositing material only where needed, additive approaches reduce waste and enable new geometries not possible with traditional subtractive methods. However, challenges remain, including material formulation constraints, process control complexities, and the need to meet long-established reliability standards in high-volume manufacturing.


Celia Wenzler

Notion Systems, based in Germany, has already established itself as a leader in industrial inkjet technology for functional materials, with a strong focus on electronics manufacturing. Its core platform, the n.jet system, is designed to enable fully digital, additive processes for applications such as solder mask, legend printing, and etch resists. Its inkjet solder mask solution stands out as a significant advancement in PCB fabrication.

Design flexibility is a key advantage of the Notion system. Because the process is digital, manufacturers can eliminate photomasks and quickly adapt to design changes, making it ideal for high-mix, low-volume production. The system also enables variable thickness control, allowing engineers to selectively build up insulation in critical areas while keeping other regions thin or uncovered.

The platform, focused on reliability, supports high precision and repeatability through optical alignment, automated calibration, and integrated curing, ensuring consistent coating quality and reliable circuit protection. It also aligns with Industry 4.0 initiatives by enabling data integration, traceability, and automation, while reducing chemical use and waste.

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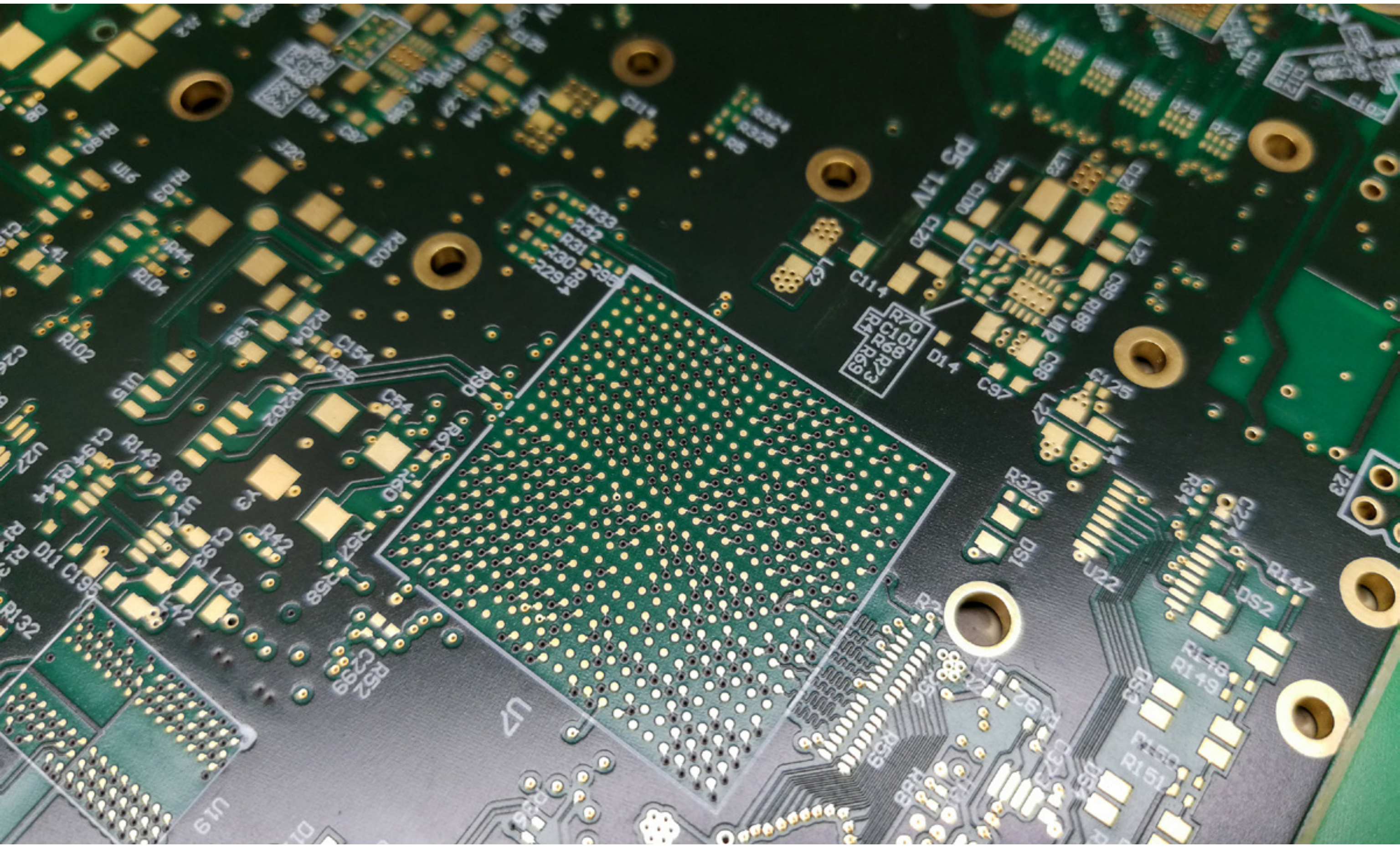
Celia's 'Take the Mic!' interview from APEX EXPO

The Role of Organic Solderability Preservatives in Advanced Packaging



BY MICHAEL CARANO, GLOBAL ELECTRONICS ASSOCIATION

Technology trends shaping the electronics industry supply chain—AI, IoT, ADAS, and high-performance computing (HPC)—are driving finer circuit features and higher layer counts. Advanced packaging drives the selection of surface finishes depending on the application.

Typical designs require excellent solder joint reliability and wire bondability. It is not uncommon for designers to specify the organic solderability preservatives (OSP) on the BGA side of the substrate and precious-metal-plated finishes on the top side, which facilitate wire bonding. This is essentially a process of selective surface finishing. The OSP is particularly useful for fine-pitch BGAs with pitches below 1.0 mm. In addition, the solder joint formed with an OSP finish is quite strong, as the tin in the solder forms a direct intermetallic bond with the copper.

The Trend Toward Mixed-metal Finishes

To achieve high-density surface mounting on printed wiring boards (PWBs), the number of terminals on circuit components has been increasing, and the pitch has been significantly reduced. With the trend toward increased packaging density has come the use of chip-on-board (COB), flip chip, and tape automated bonding (TAB).

In many instances, the surface mounting of such components may be required on PWBs with copper pads and other features plated with gold, silver, tin, or solder. These mixed-metal finish boards are becoming increasingly common, and the surface treatment of such circuits is becoming more important. The demand was such that a water-soluble surface-treating agent capable of protecting bare copper from oxidation without leaving a film on other metals needed to be developed and implemented. In other words, the need for an OSP that selectively bonds to the copper without adversely affecting other metals, such as gold or solder, was established (Figure 1).

Conventional OSP processes, based on long-chain alkylimidazole compounds and substituted benzimidazole compounds, have functioned adequately to protect the bare copper. However, these materials also deposited a significant film on other metals such as gold, tin, and solder. This additional film interfered with subsequent operations, such as wire bonding and surface mounting of quad flat packs on solder surfaces.

In addition, the contact resistance on the gold increased to unacceptable levels. Thus, when PWBs are fabricated with multiple metal finishes, the metals (such as gold or solder) must be masked to prevent OSP film formation on their surfaces. In some instances, the coating must be removed with alcohol, adding additional labor and cost to the fabrication process.

One factor in promoting this film formation on the metal surfaces is the copper present in many organic solderability formulations. The copper ions form a complex with the active azole ingredient in the OSP chemistry and actually help to promote film growth. When a copper-solder mixed-metal board is processed through such a process, the OSP forms on the solder and discolors it, making long-term solderability virtually impossible to achieve.

It has also been determined that the copper ions in the OSP protective film contribute to ionic contamination, a situation that is constantly scrutinized by assembly houses and end users. It is desired to keep ionic residues as low as possible. It has been demonstrated that the copper contributes to the staining/darkening of the solder and causes undue build-up of residue on the gold.

The Solution

The optimal solution to prevent OSP deposition on gold and improve solderability under lead-free assembly conditions is based on a unique organic compound: an imidazole synthesized as the active ingredient in the OSP (US Patent 5,795,409). This unique compound is solubilized in water and a nominal amount of acetic acid. Acetic acid helps maintain a buffered pH in the OSP process.

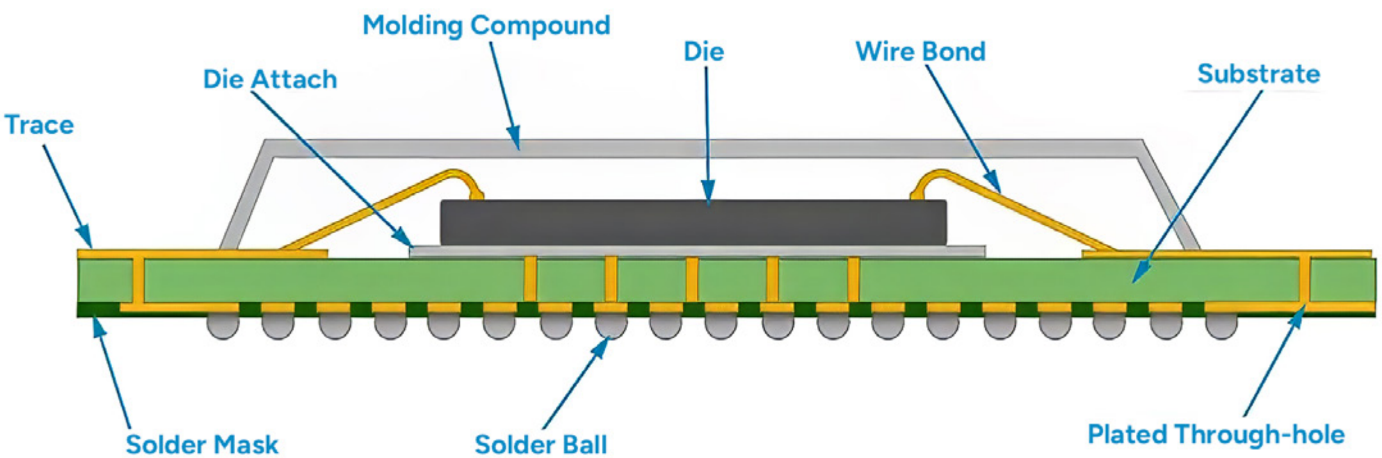


Figure 1: An advanced package with wire bonding (top side) and OSP processed copper on bottom side.[1]

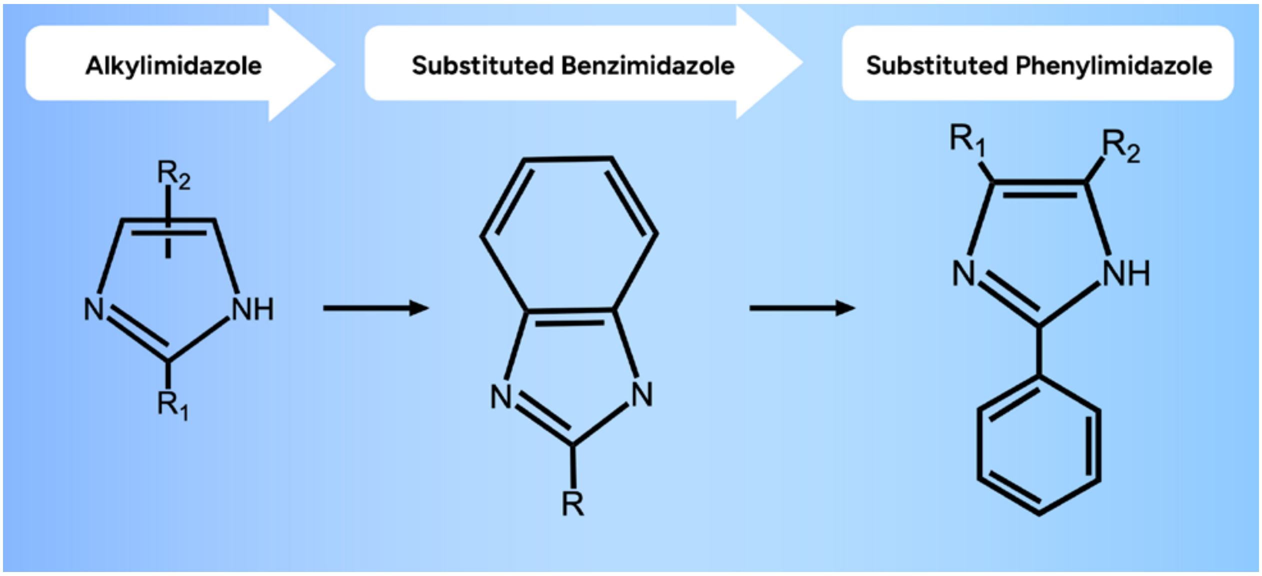


Figure 2: Evolution of OSP technology.

This process employs a combination of a phenylimidazole compound mixed in an aqueous solution with acetic acid, a complexing agent, and a water-soluble iron compound. The combination of these additives allows the uniform coating of the organic film on the copper without building any appreciable amount on the non-copper surfaces. After the PWB has been prepped in an acid cleaner, followed by a micro-etch, the OSP coating is applied to the PWB by dipping, spraying, or flood coating.

Figure 2 illustrates the latest generation OSP active compound. The substituted phenylimidazole represents a significant improvement in solderability protection as well as preventing subsequent OSP film deposition on other metals such as gold.

Therefore, it was imperative to develop an OSP process that would selectively deposit on the bare copper surfaces only, with low residual ionics. However, a film that forms on the copper must have sufficient ability to maintain the solderability of the base copper through multiple thermal excursions and with a variety of low-activity wave soldering fluxes and pastes.

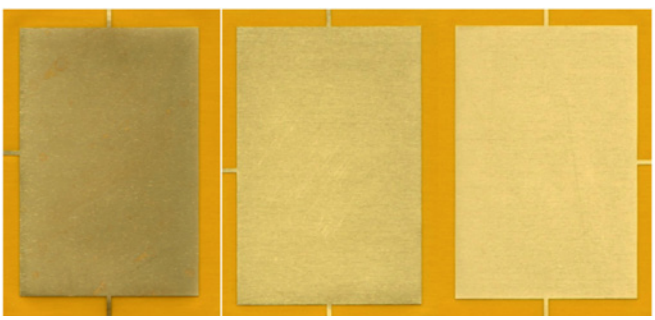


Figure 3: OSP deposit on gold: Conventional OSP (left), as plated center), and improved OSP (right).

The efficacy of this process is demonstrated in Figure 3. Note the discolored gold deposits on the left with the benzimidazole compound. The as-plated coupon is shown in the middle, and the gold-plated coupon processed through the improved OSP is shown on the right.

We should not underestimate the importance of minimizing organic deposits on gold, as they can interfere with successful wire bonding.

In a future column, we will take a more detailed look at OSP technology for advanced packaging. **I-CONNECT007**

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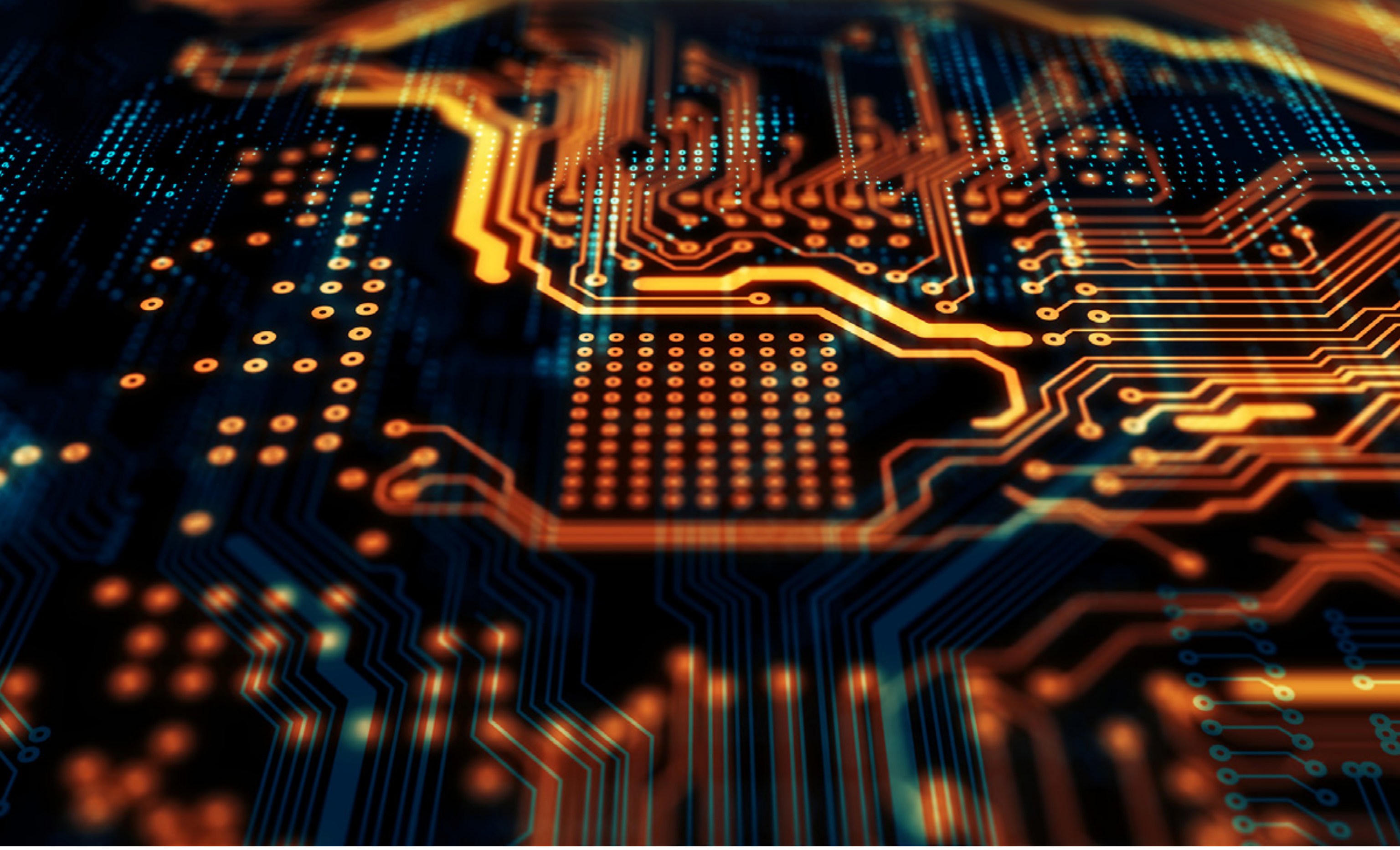
Michael Carano brings over 40 years of electronics industry experience with special expertise in manufacturing, performance chemicals, metals, semiconductors, medical devices, and advanced packaging. To read past columns, click here.

FEATURE ARTICLE

BY CARMICHAEL GUGLIOTTI, MACDERMID ALPHA ELECTRONICS SOLUTIONS



Direct Metallization

A Strategic Enabler for Advanced PCB Manufacturing

The increasing power and complexity of electronics systems are intensifying the demands on printed circuit boards and IC substrates. Applications that include AI infrastructure, high-performance computing, electric vehicles, and next-generation consumer electronics require higher interconnect density and uncompromising reliability. At the same time, PCB fabricators are navigating a manufacturing environment shaped by supply chain volatility, sustainability mandates, and ongoing cost constraints.

These forces prompt a broader reassessment of fabrication processes, particularly primary metallization, a critical step that directly influences reliability, yield, environmental impact, and operational resilience.

For decades, electroless copper plating has been the industry standard for primary metallization. However, as high-density interconnect (HDI) complexity increases and sustainability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pressures grow, more fabricators recognize direct metallization not just as an alternative process, but as a strategic enabler for future ready PCB manufacturing.

Primary Metallization: The Foundation of PCB and IC Substrate Fabrication

All multilayer PCBs and IC substrates rely on inner layer connections, typically created by buried through-holes, blind vias, or stacked microvias, to transmit electrical signals between layers. These vias are formed through mechanical or laser drilling. Primary metallization, commonly called "making holes conductive," prepares these non-conductive hole walls for electroplating.

The PCB industry currently utilizes two different processes for primary metallization: electroless copper and direct metallization.

> **"As stacked microvia architectures become more common, particularly in advanced packaging and IC substrate applications, this reliability margin becomes increasingly valuable."**

Electroless copper plating, the traditional primary metallization method, uses a chemical reducing agent (typically formaldehyde), along with multiple cleaning and plating baths, along with a palladium/tin catalyst to deposit a thin, conductive copper layer on via hole walls before electroplating.

While effective for conventional multilayer PCBs and some high-aspect-ratio through-holes, the process becomes increasingly difficult to control as feature sizes shrink and HDI complexity increases. The palladium-activated electroless copper interface introduces a distinct material boundary between deposited copper layers. Under repeated thermal cycling, this interface can become a mechanical weak point, particularly in stacked microvias. Failures may manifest as voids, cracks, or intermittent electrical connections.

In addition, electroless copper plating involves multiple chemical baths, tight process control windows, and ongoing bath maintenance. As feature sizes shrink, maintaining uniform deposition becomes more challenging, increasing the risk of defects and scrap. With rising board complexity and cost, yield losses carry increasingly significant financial implications.

The process also depends on palladium catalysts and other metal precursors, which are subject to price volatility and availability constraints. Furthermore, electroless copper plating consumes substantial water, energy, and hazardous chemicals. Aggressive sustainability targets and regulatory scrutiny around chemical handling, wastewater treatment, and worker safety continue to intensify globally, adding operational complexity and cost.

These factors are prompting fabricators to evaluate whether legacy primary metallization approaches remain optimal for the next generation of electronics manufacturing.

Direct Metallization: Enabling High Density Designs

Direct metallization is an attractive, technically robust alternative to electroless copper that offers reliable microvia performance, stable processing, and compatibility with today's high-density designs. Rather than chemically depositing a copper interface layer, the process applies a thin conductive carbon- or graphite-based coating to via walls. After selectiving microetching the exposed copper surfaces, electrolytic copper plating proceeds, forming a direct copper-to-copper bond.

Direct metallization delivers key reliability advantages over electroless copper for advanced HDI applications. By removing the electroless copper interface, the copper structure within microvias becomes more resistant to mechanical stress and thermal fatigue. These improvements have been consistently validated through industry standard tests, including via pull, IST, TCT, OM, CITC, and simulated reflow.

Reliability is further enhanced by optimizing the

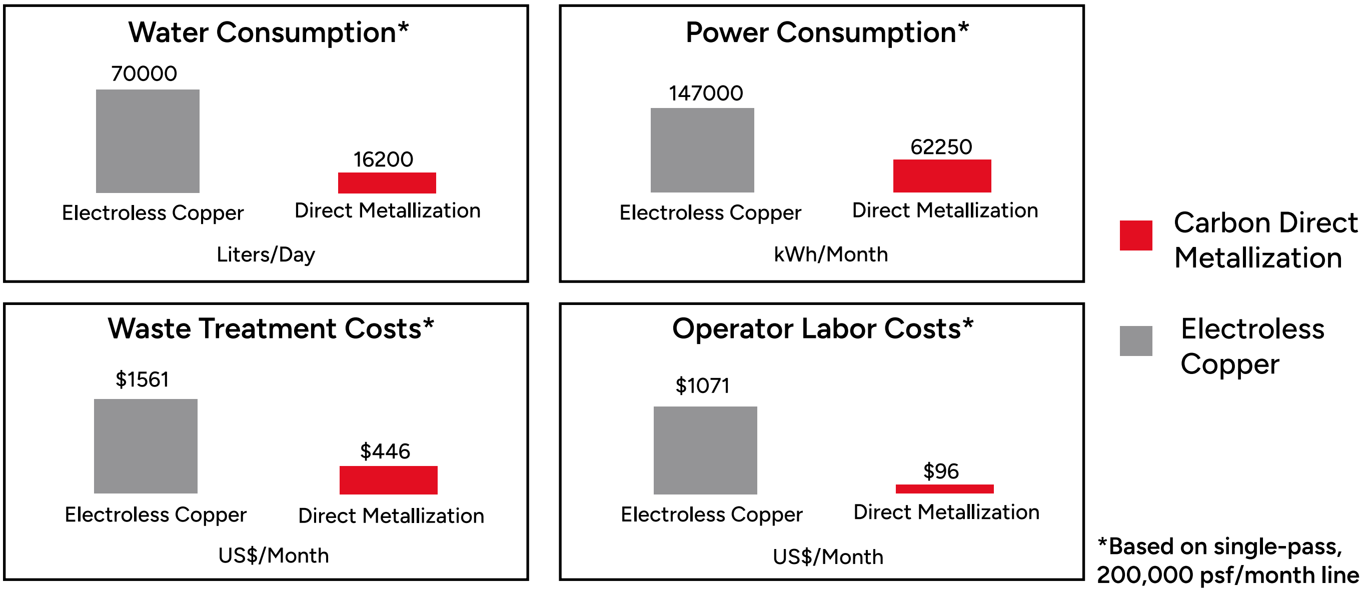

Figure 1: Comparing the metrics for a single-pass production line, using Blackhole® direct metallization and Via Dep® 4550 electroless copper.

interaction between direct metallization and via fill plating. Recent studies[1] show that improved control over direct metallization and electrolytic copper deposition reduces etching, lowers total copper consumption, and supports finer line and space capability. Next generation direct metallization systems, such as Shadow® Plus, paired with advanced via fill chemistries like MacuSpec™ VF TH 500, consistently exceed IPC reliability requirements. These chemistries demonstrate strong performance across IPC Class III testing, including solder dip, IR reflow, and OM tests, above the targets for IPC-TM-650 2.6.8, 2.6.26, and 2.6.27 specifications.

As stacked microvia architectures become more common, particularly in advanced packaging and IC substrate applications, this reliability margin becomes increasingly valuable.

Yield, Throughput, and Process Stability

Beyond reliability, direct metallization delivers significant gains in yield and manufacturing efficiency. Defects in the interfacial electroless copper layer can lead to separation failures, resulting in intermittent or open circuit failures during electrical testing. Direct metallization requires fewer processing steps and has a faster throughput than electroless copper. It simplifies quality control and increases yields.

The direct metallization process is highly stable, allowing for easy start-and-stop production, is non-dynamic, and has a longer bath life than standard electroless copper processes.

Direct metallization also supports a wide range of materials and design architectures and is suitable for both rigid and flex materials. It can work with small feature sizes, including microvias with an aspect ratio approaching 1.2:1 on thin substrates (~3 µm foil). It can also be applied to thicker boards with through-holes with an aspect ratio up to 20:1 without equipment modifications.

The technology is compatible with major HDI and IC substrate material sets, enabling fabricators to adapt quickly to evolving customer requirements without introducing new supply chain dependencies. Its lower copper etch factor supports tighter line and space geometries—a critical advantage for advanced designs.

Additionally, direct metallization is compatible with most existing electrolytic copper plating products. This enables efficient production across a wide range of designs, supporting supply chain resilience and adaptability.

Sustainability and Supply Chain Resilience

Environmental regulations, water scarcity, and material restrictions are increasingly influencing global PCB manufacturing strategies. As production footprints diversify geographically, sustainability and compliance are crucial factors for cost and risk management.

In this context, direct metallization stands out as a superior, sustainable, and cost-effective alternative to electroless copper plating. It offers key environmental and operational benefits, including:

- Up to 90% reduction in rinse water consumption and operator labor costs
- No continuous generation of by-products in the process tank
- Elimination of precious metal precursors such as palladium
- Removal of hazardous chemicals, such as formaldehyde

These advantages translate into significant savings in water, waste treatment, power, chemicals, and labor costs. Figure 1 provides a comparison of these metrics for a single-pass production line, using Blackhole® direct metallization and Via Dep® 4550 electroless copper, operating at 200,000 sq.ft./month.

Reducing the environmental footprint gives manufacturers more flexibility in choosing production sites, reducing their vulnerability to material, water, labor, and energy shortages. As companies prioritize sustainability and environmental regulations tighten, direct metallization allows manufacturers to remain compliant without compromising cost, efficiency, or quality.

Looking Ahead

As electronic devices shrink and functionality expands, PCB fabrication must support finer features, thinner layers, and higher interconnect densities without sacrificing reliability. In a volatile manufacturing landscape, constraints on materials, water, energy, and regulatory compliance are as critical as electrical performance.

Direct metallization addresses these challenges head on. It improves reliability, increases yield, enhances process stability, and reduces environmental impact, all while strengthening supply chain resilience. By eliminating interfacial failure points, supporting diverse materials and designs, and enabling more sustainable manufacturing, direct metallization provides a robust foundation for advanced HDI and IC substrate production.

Its ability to support both high and mid complexity designs on a single production line makes direct metallization a strategic enabler for long term competitiveness in the evolving electronics manufacturing landscape.

For more information on direct metallization for HDI PCBs and IC substrates, please contact MacDermid Alpha Electronics Solutions. **I-CONNECT007**

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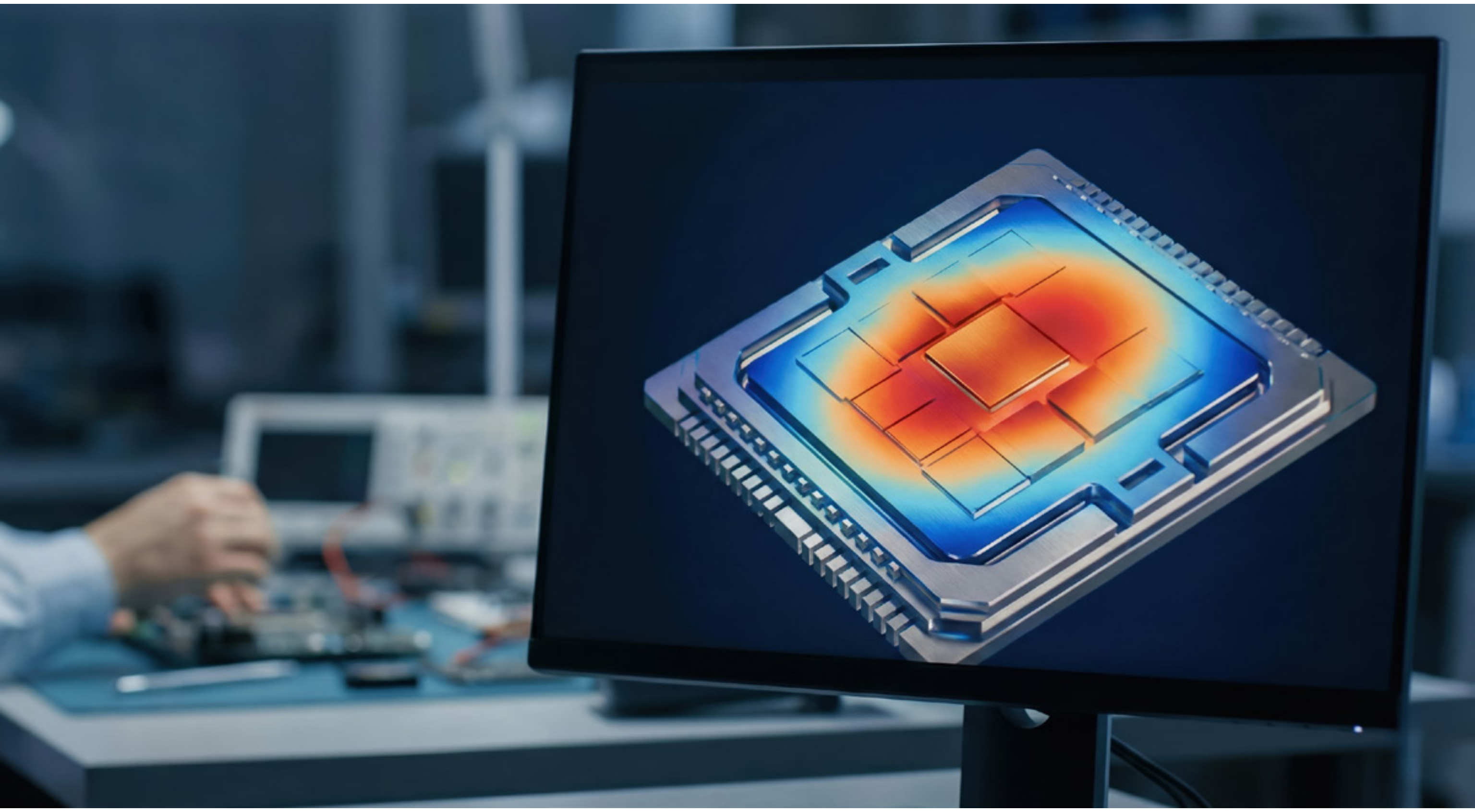
Carmichael Gugliotti is director of primary metallization for MacDermid Alpha Electronics Solutions and new author.

DIGITAL TWINS

Integrating Design and Manufacturing



BY HAPPY HOLDEN, I-CONNECT007

New product realization and design for manufacturing and assembly (DFM/A) are becoming increasingly visible as programs that can improve time-to-market and reduce product costs. These simulations of real-time manufacturing are now referred to as digital twins. While many companies are developing such programs, a unifying framework is needed to coordinate their application.

Concurrent engineering has been the basis for electronics design, but its one-way interactions with manufacturing constitute the old way of thinking. This column proposes a new framework based on digital twins, enabling manufacturing constraints to be incorporated earlier in the design process.

The capabilities of electronic technologies are growing at an ever-increasing rate. Unfortunately, we have also seen a corresponding increase in the complexity of packaging. Modern EDA tools and concurrent engineering are primary drivers of this phenomenon. What we have not yet developed is an effective way to feed manufacturing experience and knowledge back into design.

The Nature of the Problem

Experienced manufacturing personnel are becoming increasingly scarce, and developing that expertise takes years. In many cases, manufacturing is also geographically distant, making knowledge transfer even more difficult. As a result, input is often reduced to opinion rather than data, making it difficult to defend or apply consistently.

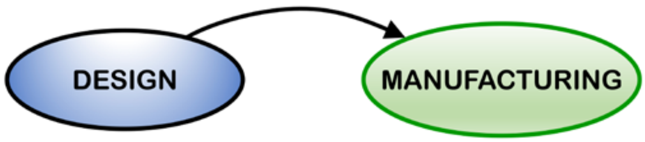


Figure 1: Current product data movement.

While this might be a viable solution for small, vertically integrated companies with extensive manufacturing experience, printed circuit packaging has advanced significantly. Not only is surface mounting now very fine-pitch, but we have ball grid arrays, flip-chip, and chip-scale packages.

These challenges have led to widespread adoption of DFM/A approaches, but they remain fragmented. They focus on separate domains, ranging from minimization of assembly and substrate costs, optimization of printed circuit design and layout, and analysis of test coverage.

The Opportunity of Design for Manufacturing (DFM/A)

There are four compelling reasons why predictive engineering is essential to the design of electronic products:

1. Products have become increasingly complex. Not only must products meet higher customer expectations, but they must also be environmentally friendly, energy-efficient, and resource-conserving in ever-shrinking product lifecycles.

2. Minimizing cost is imperative. DFM/A has been shown in benchmarking and case studies to reduce assembly costs by 35%[1], PWB costs by 25%,[2] and 75% of a product's manufacturing cost is determined by its design drawings and specifications.

3. In the electronic product design process, 60% of the manufacturing cost is determined in the first stages of design when only 35% of the design cost has been expended. The product definition process includes specifications and partitioning. This is a technology tradeoff analysis (the balance of loss and gain in various domains' performance vs. costs).

4. Manufacturing should be linked to design and R&D through a common language that

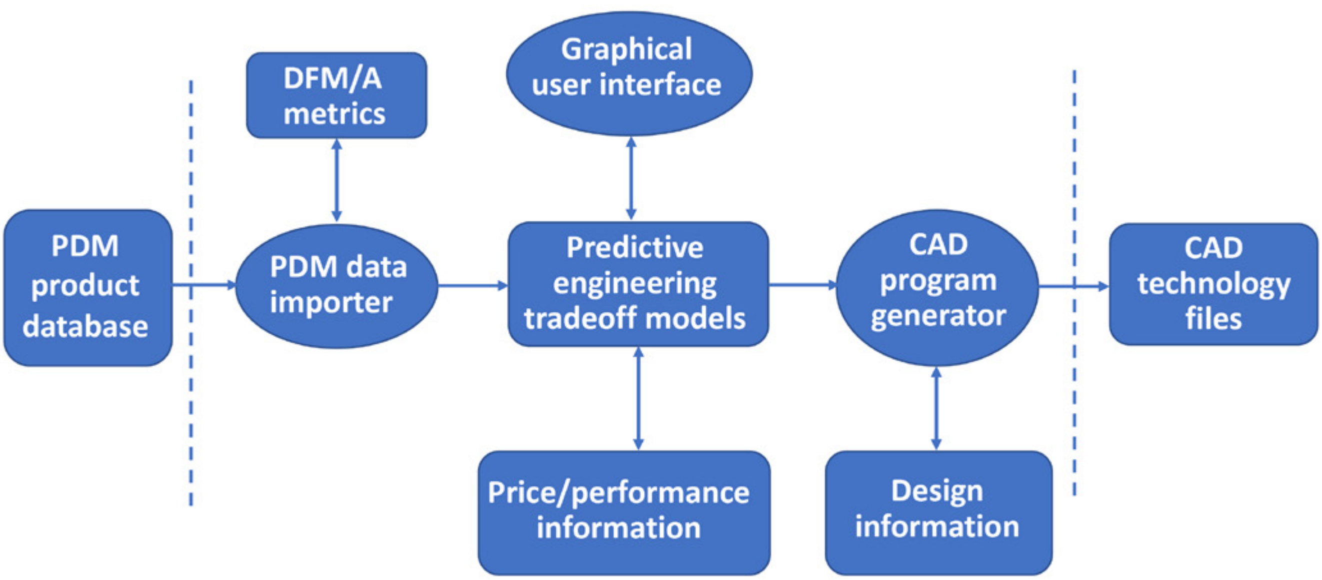


Figure 2: For the digital twin of a PCB, there should be simulations and tradeoffs that cover all the domains that a user finds critical, including costs, manufacturability, density, signal integrity, and reliability.

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Uniplate® IP3 – Where innovation meets virtuosity

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defines producibility as an intrinsic characteristic of a design. It is not a manufacturing inspection milestone. Producibility scores provide a non-opinionated basis for a team approach that results in a quality, cost-competitive product.

What they all have in common is metrics. But the design community is suspicious when the entire system is not considered. They are afraid of sub-optimization, where the cost of a particular domain is lowered, but the total system cost goes up. The industry does not lack DFM/A tools or metrics; it lacks a way to integrate them across the full design and manufacturing process.

Digital Twins

Digital twins (DT) enable systematic trade-off analysis across multiple design and manufacturing domains. It brings together product definition, fabrication, and assembly considerations into a single trade-off environment.

A digital twin of the performance and costs (yields) based on predictive models and simulations can be coded to allow the designer to see the effects of various parameters on the PCB without ever actually building it. As shown in Figure 3, this allows the user to improve on any product development or product change process.

One key element that's missing is the global assignment of custom ASIC pin locations. This would help to reduce PWB and assembly complexity and costs, while assuring better system performance and the best "time-to-profits."

The DT framework (Figure 3) imports critical metrics and data from manufacturing through the PDM database.[3]

The DT software architecture of tradeoff models and supporting software provides the user with global information. As features are selected, they can be placed back in the PDM database. Selection of layout factors, sizes, and design rules can be used to create technology files that drive modern CAD programs.

Digital Twins' IPC-2551

IPC-2551 is the digital twin standard for assembly automation that provides all DT developers with the information and guidance necessary to understand a full DT implementation. It also provides information and guidance on how manufacturers can benefit from digital twins, how to assess DT readiness levels, and how to prepare a factory of any size or production volume to implement a full DT approach to its factory and/or products.

The effect is that physical prototypes of any description can be avoided, including trial and error, resulting in vastly reduced lead-time, elimination of mistakes, and lower costs.

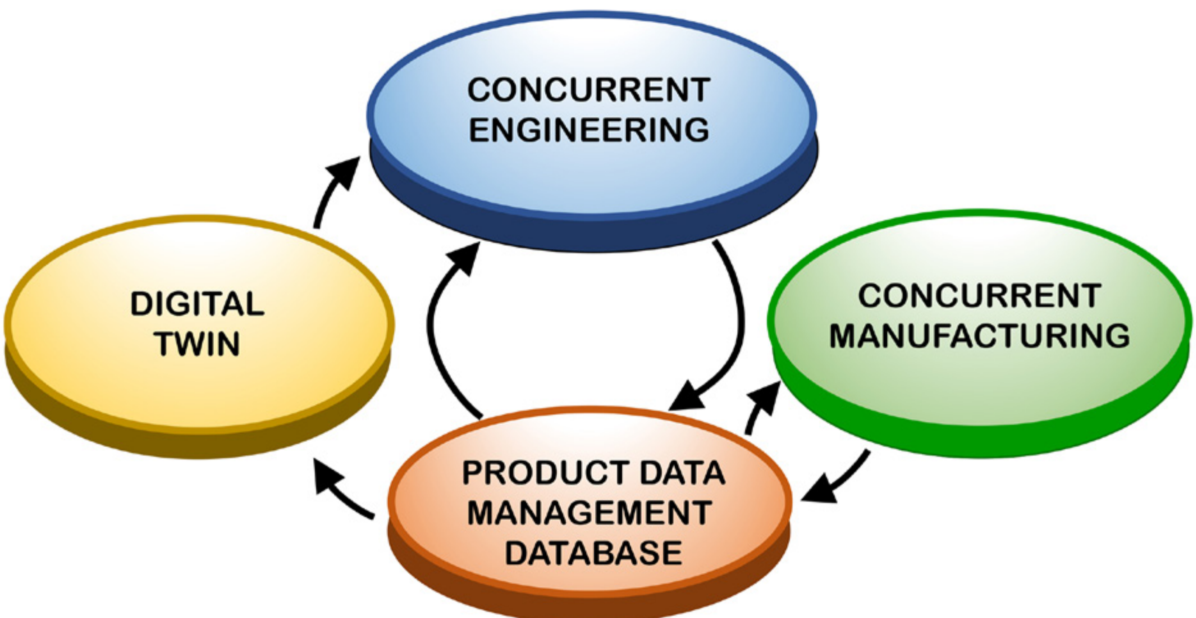

Figure 3: Proposed digital twin framework.

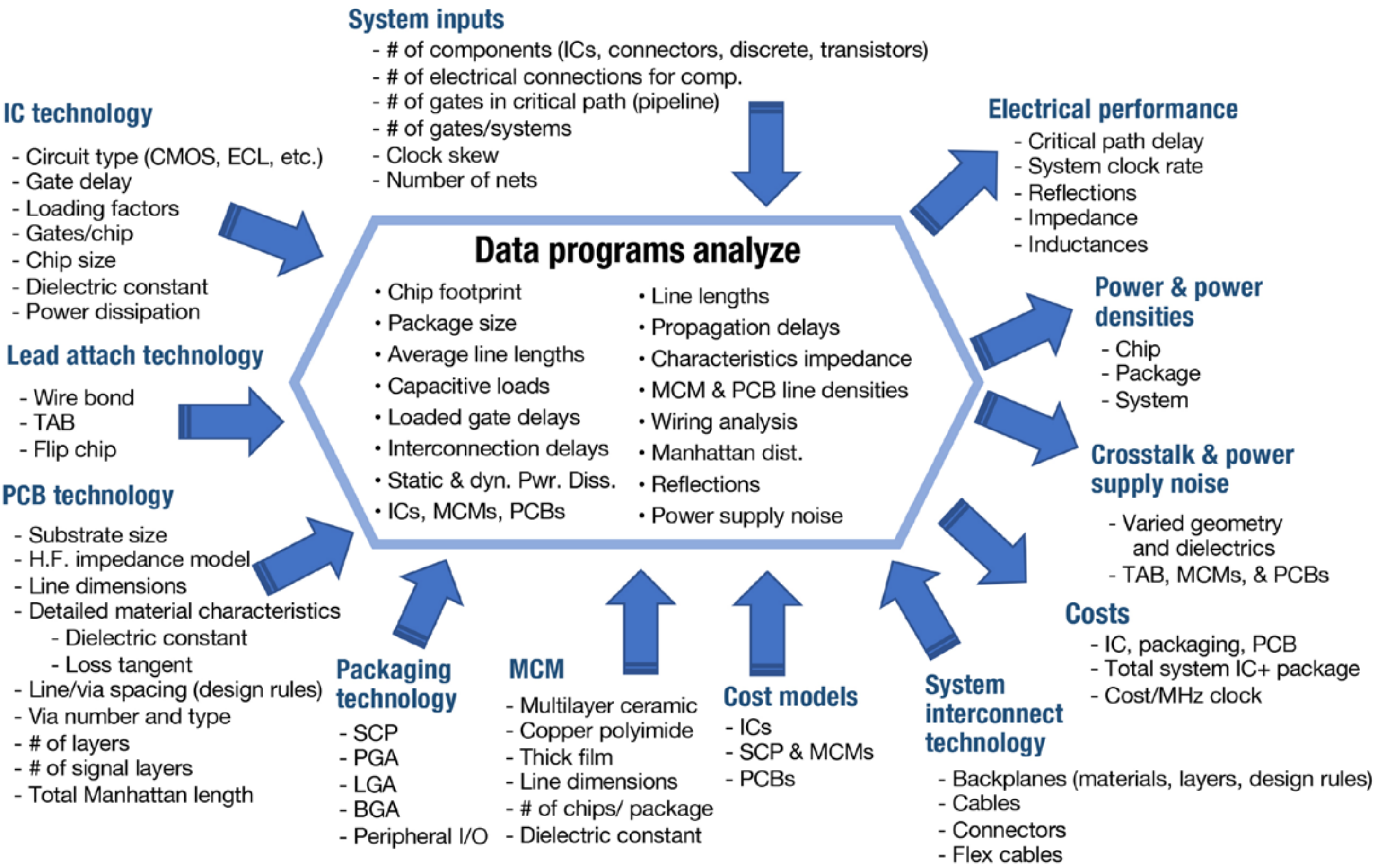

Figure 4: Proposed digital twin architecture.

Conclusion

To reduce time-to-market and production costs, companies must integrate DFM/A into a cohesive product generation framework that includes DT predictions, concurrent manufacturing, and PDM systems. This integration is essential for developing competitive electronic products. Typical digital twin software development tools are available from companies such as ScaleOut software.[4]

The tools, software, and elements of such a vision are shown in Figure 4. The remaining challenge is integrating these capabilities into a unified software environment that fully supports digital twin implementation. **I-CONNECT007**

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BY ANDREAS SCHATZ AND MUSTAFA ÖZKÖK, MKS' ATOTECH

Innovative Flash Copper Plating Technology

For Enhanced mSAP Via Reliability, HDI Manufacturing Efficiency, and Advanced Production Control

Editor's note: This paper was first presented at IMPACT 2025 in Taiwan.

The continuous push toward higher functionality, miniaturization, and performance in modern electronic devices—such as smartphones, wearables, and advanced computing platforms—has intensified the demand for high-density interconnect (HDI) printed circuit boards. Central to HDI performance is the reliable formation of blind microvias (BMVs), which serve as critical interlayer connections in modified semi-additive processes (mSAP).

As BMV geometries shrink and core materials become thinner (≤25 µm), conventional electrolytic copper plating systems encounter significant challenges: achieving sufficient copper coverage inside the via while minimizing unwanted surface deposition that inhibits fine line/space (L/S) capabilities. Furthermore, inconsistencies arising from glass fiber protrusions, copper overhang, wedge formations, and drilling variability can negatively impact via reliability.

To address these challenges, a newly developed electrolytic flash copper plating system introduces

major innovations in anode design, electrolyte distribution, contamination control, and transport precision. These advancements collectively deliver superior uniformity, improved microvia copper structure, enhanced system sustainability, and lower cost of ownership.

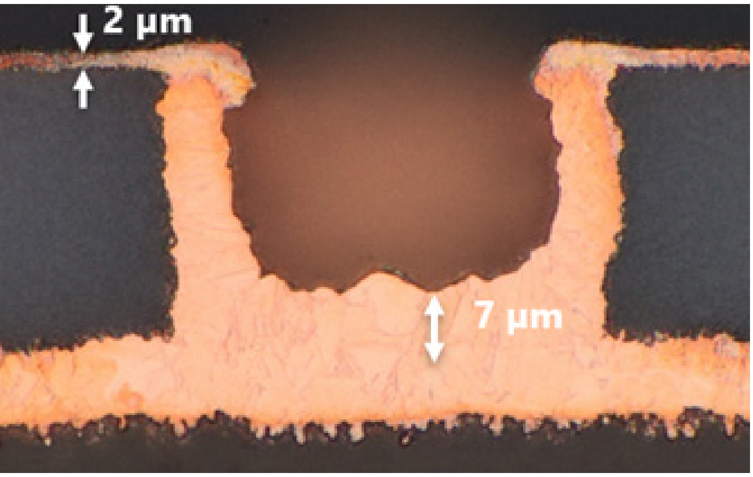


Figure 1: Low copper thickness (on top) for good L/S capability and high copper thickness (on bottom) for good reliability.

Process Background and Core Advantages of Flash Plating

The previous generation of flash copper plating systems gained substantial industry adoption due to an efficient wet in wet integration between electroless copper deposition and electrolytic flash copper reinforcement. Key advantages of this approach include:

1. Prevention of oxidation: Direct transition between process steps avoids drying-induced oxidation on electroless copper, preserving interface quality and improving metallurgical bonding.
2. Enhanced BMV reliability: The process effectively reinforces copper in BMV wedges, masks glass protrusions, and levels irregular drilling defects, leading to durable via structures.
3. Superior copper-to-copper epitaxy: A highly uniform crystallographic transition between electroless and electrolytic copper improves electrical and mechanical reliability.

These strengths form the performance baseline for the newly enhanced plating system.

Next-generation Plating System Design

To better meet the stringent technological requirements of advanced HDI manufacturing, the system was optimized to ensure uniform surface copper distribution. This was achieved through a comprehensive redesign of the anode system, focusing on fluid dynamics and electric field control.

Redesigned Anode Box for Superior Uniformity

The newly engineered anode box increases flow rate by more than 130% and triples the number of spray nozzles, producing a far more uniform and controlled spray pattern. At the same time, the upgraded filter pump circuit boosts energy efficiency, cutting power consumption by over 40% per cubic meter of transported fluid.

To enhance electric-field control, the anode was resegmented to provide 50% more independently controlled zones within the same footprint, significantly improving copper uniformity, especially behind the clamp area, where thinner copper-clad is prone to edge etching. A redesigned clamp with advanced 3D printed shielding further redirects field lines and improves electrolyte exchange. Together, these upgrades minimize edge etching and ensure more consistent plating quality across the entire panel.

Advanced Particle Control for High-yield Manufacturing

Effective particle control is essential for maintaining high yields in advanced plating. To prevent particle ingress at known generation points—such as the clamp's sliding contact—a targeted extraction system was added to capture debris immediately and route it to a dedicated collection chamber, keeping contaminants out of the electrolyte. The anode box was fully enclosed with glass lids to block airborne particles from settling on its surface.

Electrolyte management was also strengthened through a major upgrade of the filter pump circuit, increasing filtration efficiency by 210%. A new catwalk behind the filtration unit allows for quick, convenient filter changes, minimizing downtime and supporting stable, high quality production.

Inline Optical Quality Control (IOQC) for Closed-loop Process Stability

Inline optical quality control (IOQC) complements next-generation flash plating by adding objective, image-based verification of panel condition before and after critical steps. High-resolution inline inspection can flag and empower the prediction of surface anomalies and handling-related defects (e.g., scratches, clamp/edge marks, localized stains, or particle-related artifacts) early enough to prevent yield loss downstream.

When linked to product traceability, IOQC enables trend monitoring across lots and supports faster root-cause analysis by correlating visual signatures with process conditions (transport, filtration performance, and local uniformity effects).

Used as a "digital layer" around the plating module, IOQC strengthens process robustness by turning sporadic defects into measurable signals that can be acted on promptly, supporting stable high-yield manufacturing in advanced HDI and mSAP production.

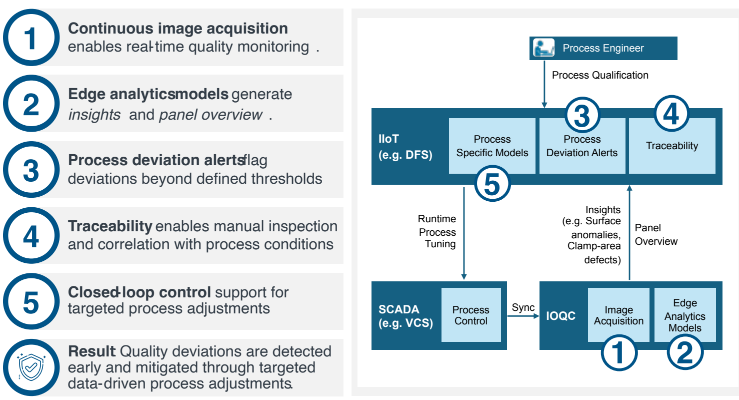


Figure 2: Precision transport for ultra-thin cores.

As HDI designs advance, particularly with mSAP, inner layer thicknesses are dropping to 30–50 µm, and in leading-edge cases to ≤25 µm. Combined with thin copper-clad, this creates growing challenges for horizontal transport. To address this, specialized guiding zones were added at the plating unit's inlet and outlet to ensure stable and reliable panel handling.

Compact, Energy-efficient System Design

To support sustainable production, the plating unit was redesigned to reduce material use and improve energy efficiency. A lower housing height decreases material consumption while improving maintenance access. A more compact internal layout cuts electrolyte volume by 24%, reducing both heating demand and holding tank capacity, and enhancing overall environmental and operational efficiency. These improvements reduce energy, water, and chemical consumption while simplifying maintenance.

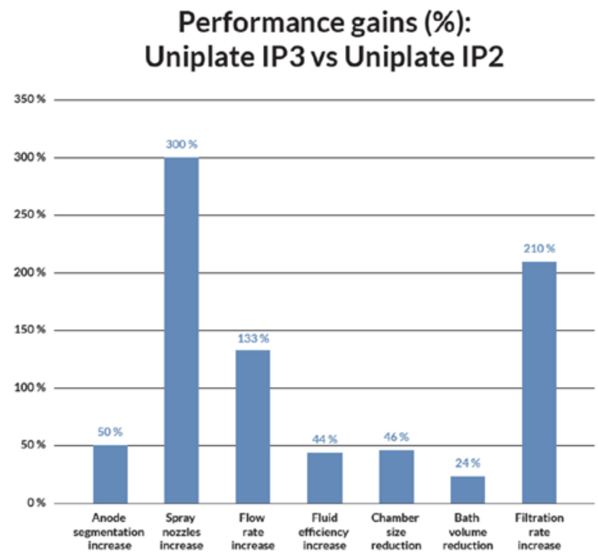


Figure 3: Improvement of new copper plating line: New vs. old.

Results of the Upgraded System

The upgraded flash plating system underwent extensive evaluation, comparing its copper deposition performance to the previous Process of Record (POR). The goal was to improve copper's physical properties while preserving the POR's strengths, including BMV reliability and wet in wet compatibility.

The upgrade focused on three key objectives:

- Improved material performance through better copper uniformity, grain structure, and adhesion for higher interconnect reliability.
- Greater process efficiency by lowering chemical consumption, shortening process times, and enhancing bath stability.
- Maintain BMV integrity, ensuring strong copper fill and leveling for robust mechanical performance.

Initial results show that the upgraded system not only meets but surpasses the previous POR, delivering a more cost effective and technically advanced solution for high density interconnect manufacturing.

Minimal Surface Copper Formation

Surface copper thickness is a critical factor, as excessive surface buildup limits achievable line and space resolution. To demonstrate the performance of the new flash plating system, a PCB with substantial copper overhang was used, as shown in Figure 4 (left).

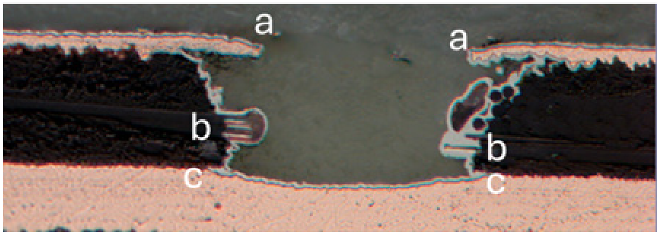


Figure 4: As received condition of BMV with Ø75 µm, 45 µm depth with a) big copper overhang; b) big glass protrusions; and c) wedge formation.

BMVs with this shape are very difficult to plate. With the newly developed flash plating system, excellent results could be achieved as illustrated in Figure 5.

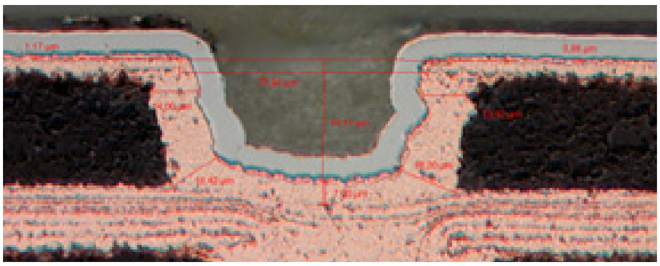


Figure 5: BMV after flash plating with only 1 µm of plated copper on the surface.

These results clearly demonstrate the system's excellent flash copper plating capability. Drilling defects such as wedge voids, copper overhangs, and glass protrusions can be effectively masked while keeping surface copper buildup to a minimum.

Flash Plating of Small BMVs

We also evaluated plating on smaller BMVs. Even at reduced diameters, the system achieved very good BMV reinforcement with minimal surface copper thickness.

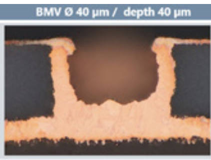
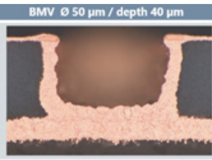
	BMV Ø 40 µm / depth 40 µm	BMV Ø 50 µm / depth 40 µm
BMV x-section		
CCL / electroless	2 µm / 0.6 µm	2 µm / 0.6 µm
Plating time	6 min	6 min
BMV Pitch	250 µm	250 µm
CuT BMV dense area	~1.8 µm	~1.8 µm

Figure 6: BMVs with 40 and 50 µm opening plated with the new system.

Copper Crystal Structure and Epitaxy Analysis

The copper crystal structure was analyzed using Scanning Electron Microscopy (SEM) at two via diameters: 40 µm and 50 µm.

The evaluation showed a well formed epitaxial interface between the electroless copper and the new flash copper layer at the BMV capture pad, indicating excellent metallurgical continuity for strong mechanical and electrical reliability. Distinct copper twin boundaries were also observed, confirming a robust copper to copper bond and high integrity grain growth. This improved epitaxial alignment is expected to support superior NCL test performance, further enhancing long term via reliability.

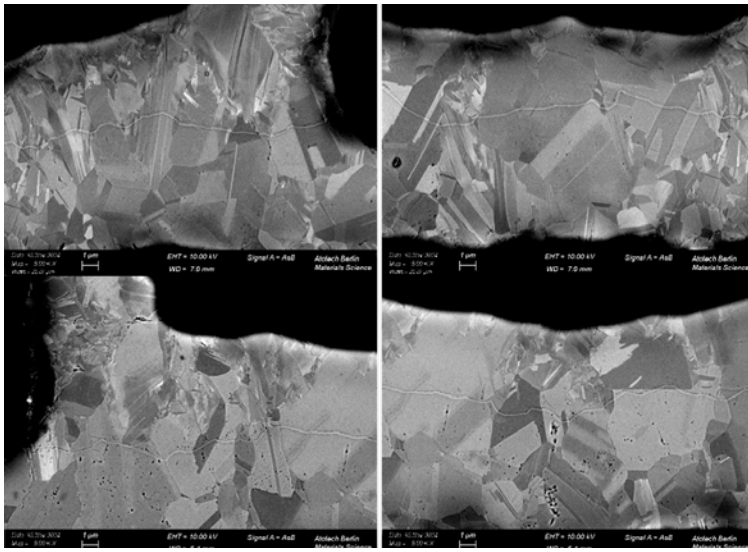


Figure 7: Crystal structure of 50 µm BMV corner (left) and center (right).

Normalized Tentative Crack Length (NCL) Method

Assessing copper epitaxy is often subjective, relying heavily on expert interpretation of SEM images. To provide a more objective and quantifiable evaluation, the Normalized Tentative Crack Length (NCL) Method[1] can be used. This approach enables direct comparison between the current POR and the new flash plating process through standardized image analysis and scoring criteria, ensuring consistent and reproducible assessment of interfacial integrity.

Figure 8 and Table 1 illustrate the evaluation framework used to determine NCL values.

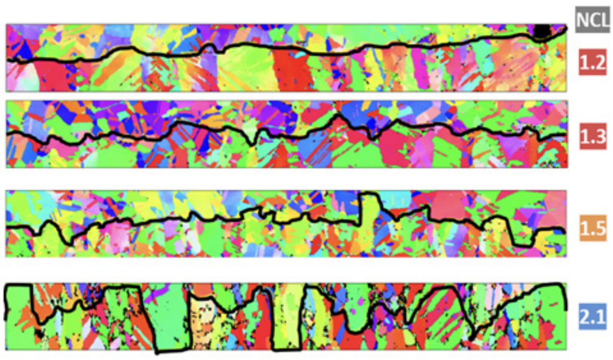


Figure 8: Used evaluation framework to determine NCL values.

TABLE 1: DESCRIPTION OF NCL NUMBERS

NCL Result	Degree of epitaxy	Risk
1 ≤ NCL ≤ 1.3	Low degree of epitaxy	Potentially high risk of cracks
1.3 < NCL ≤ 1.5	Medium degree of epitaxy	Potentially medium risk of cracks
1.5 < NCL	High degree of epitaxy	Potentially low risk of cracks

Using this method, we analyzed 36 BMVs plated with both the legacy and upgraded flash processes. The results, summarized below and shown in Figure 9, demonstrate a clear improvement in NCL values with the new system. These findings confirm that the upgraded flash plating enhances copper to copper bonding and improves the mechanical reliability of the plated vias.

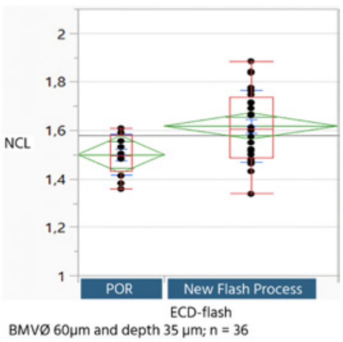


Figure 9: Results of NCL for POR vs. the new flash process.

Conclusion

The newly developed electrolytic flash copper plating system represents a major technological advancement in HDI and mSAP PCB manufacturing. It delivers exceptionally uniform copper distribution while minimizing surface buildup, ensuring consistent layer quality even in demanding designs. The system significantly strengthens BMV structures, reliably compensating for severe drilling defects and enhancing overall reliability. Its optimized crystal structure promotes superior metallurgical bonding, further improving long term performance.

In addition, the technology introduces major improvements in particle control, resulting in higher yield stability and more predictable production outcomes. Enhanced transport precision supports the handling of ultra thin cores with greater accuracy and reduced risk. Beyond performance gains, the system also lowers chemical, water, and energy consumption, making the process more sustainable. Together, these advancements provide a substantial reduction in total cost of ownership and establish a new benchmark for next generation PCB fabrication.

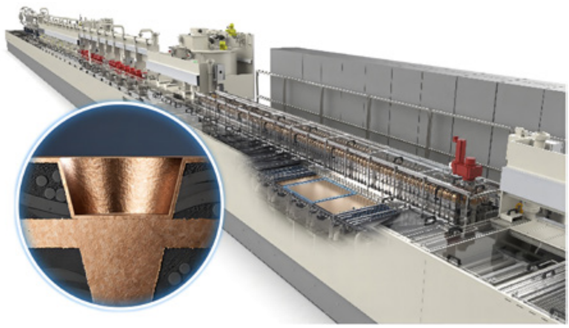


Figure 10: Horizontal desmear, electroless copper deposition, and electrolytic copper plating line featuring next-generation horizontal copper plating technology.

Building on a POR already regarded as best-in-class, this upgraded system further advances uniformity, L/S capability, and sustainability. It provides PCB manufacturers with a robust, scalable solution tailored to the stringent demands of next-generation electronics. **I-CONNECT007**

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BY MARCY LARONT, I-CONNECT007

The AI Tipping Point

Transforming Global Material Supply Chains

While the AI revolution has the world focused on the promise of solving our most complex challenges, some laminate and PCB fabricators are raising concerns that the high-performance materials used to build AI data centers will gobble up the precious resources needed to produce them.

PCB industry expert Mark Goodwin, COO of Ventec International, is among a growing handful of suppliers who have been vocal in expressing their concerns about the critical shortage of glass and copper, which they believe will only get worse. Mark has specifically emphasized that copper-clad laminates (CCLs), the foundational substrate for

PCBs, are closely linked to macroeconomic forces, including fluctuating copper prices and demand from data centers and advanced electronics. High-end AI applications absorb a disproportionate share of materials, manufacturing capability, and supply chain attention.

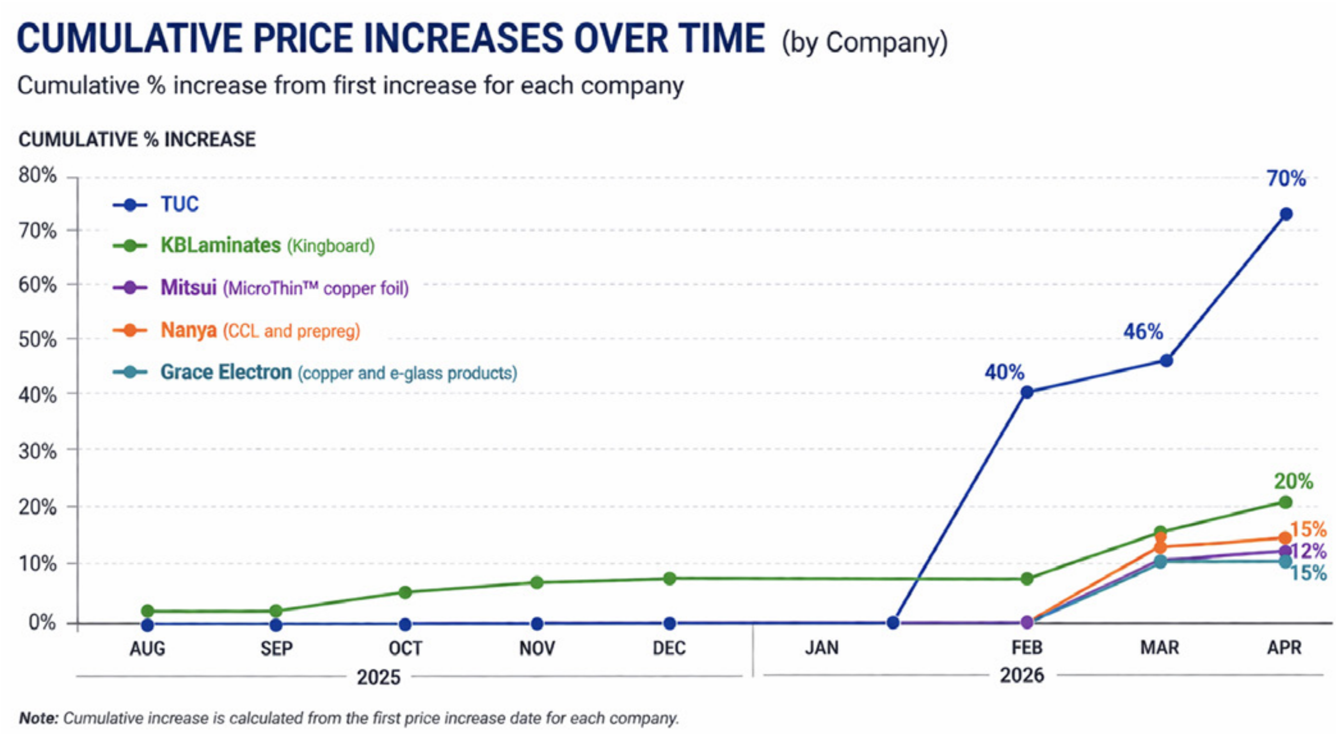
So, what happens to everything else that requires a PCB when the market cannot secure supply at a viable cost or to a scale matching consumer demand? We know that the demand for these products will not disappear, but the capacity to support them will be squeezed significantly.

The Great Reallocation: AI Claims the Supply Chain

After China entered the WTO, the rebalancing of the world's manufacturing base accelerated, and the reshaping of some of the world's largest economies. Major OEMs and manufacturers—HP, Dell, Motorola, Flex, and Apple—migrated their manufacturing operations to Asia, which had a significant effect on PCB manufacturing in the United States. In 1990, there were roughly 1,500 PCB fabrication shops in North America. By 2010, that number had dropped to 300, and today, there are an estimated 150 or fewer PCB shops.

AI is, unarguably, the next tipping point. It will bring sweeping transformation to the global supply chain and the world economic balance. Chips are at the core of the AI era, and the PCBs that support them have become central to one of the industry's most significant growth opportunities in decades. PCBs are finally getting their due, viewed now as critical, even strategic.

However, this rapid rise of AI infrastructure means capacity will be reallocated across the PCB supply chain. According to QYR Research, "The global market for PCB in AI Servers was estimated to be worth US$7452 million in 2024 and is forecast to reach a readjusted size of US$11252 million by 2031 with a CAGR of 6.8% during the forecast period 2025-2031."[1] AI server boards use more layers, higher-speed/low-loss laminates, and heavier board content per system than mainstream electronics, thus their share of laminate glass and copper is higher than may be indicated by the number of PCB units purchased. Within the global CCL market, estimated at $16–$19 billion, AI is a dominant consumer.[2]



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Supply Tightens, Prices Surge Again and Again

Over the past several months, there have been rapid, repeated price increases across the base materials supply chain, driven by rising copper costs (see sidebar) and an industry-wide fiberglass shortage. Given current resource scarcity, a partial summary of recent price increases based on corporate announcements is as follows (Table 1).

The pace and frequency of these increases point to more than normal market fluctuation, which ranges between ±5 to ±15% year over year, according to data from the London Metal Exchange (LME), the U.S. Geological Survey (USGS), and the World Bank Commodity Price Data. We're likely to see more price increases in the coming months, with no forecast for when market stasis might be reached.

At the same time, changes in the global supply base are reinforcing this strain. Japanese glass manufacturers, for example, are pivoting toward higher-value glass semiconductor substrates, further narrowing the glass supply available for supporting products that are less complex to build. Geopolitical risks such as the ongoing U.S. conflict with Iran have introduced volatility, not only into energy markets, but also global logistics with blocks and delays at the Strait of Hormuz, adding further uncertainty to an already stressed electronics supply chain.

If You're Not AI, Do You Still Matter?

High-end and AI applications are not only driving growth but competing for and often securing the materials and capacity the rest of the industry depends on. So, there is an incentive to secure a position within the AI ecosystem. The margins, growth, and visibility are all there. But what happens to everything else?

A significant portion of the global PCB market supports applications beyond AI and high-speed computing, conservatively estimated at over 50%.3 These include automotive systems (non-autonomous or EV), industrial controls, consumer electronics, appliances, and so many other everyday products. While some of these segments are evolving to incorporate more advanced electron-

The Copper Conundrum

Copper prices have climbed sharply over the past year due to both structural and short-term market forces. Supply has been constrained by mine disruptions, declining ore quality, and a slow pipeline of new projects, while demand is surging from electrification, renewable energy, electric vehicles, and expanding digital infrastructure such as AI data centers. This imbalance has pushed the market into a sustained deficit.

Financial dynamics, including investor flows into commodities and favorable macro conditions, have resulted in a broad repricing of copper as a critical global material.

For the PCB industry, rising copper prices directly translate into higher costs for copper foil and laminates, the foundational materials of circuit board fabrication. As copper has become more expensive and volatile, laminate suppliers are passing through the increases. This puts pressure on fabricators' margins and complicates quoting and long-term pricing agreements.

Tight supply conditions also affect availability and lead times for copper-clad materials. At the same time, the same demand drivers pushing copper prices higher—electronics, data infrastructure, and electrification—are increasing PCB demand, creating a dual pressure of rising input costs and high demand.

Resources

- "Copper Prices Have Hit Record Highs, but Smelters Face Mounting Strategic Pressures," International Energy Agency, 2024.
- "Copper Outlook: Structural Deficits to Support Prices," JPMorgan Global Research, 2025.
- "Copper Prices Hit Record Highs as Demand from AI and Data Centers Surges," Business Insider, 2026.
- "Global Copper Supply Shortage Driven by Production Disruptions," ABC News, Oct. 7, 2025.
- "Copper Reaches Record $12K per Ton as Demand Surges," New York Post, Dec. 23, 2025.

ics, many will never require the highest-end materials or designs that drive today's supply constraints.

Should manufacturers shift their focus entirely? Will lower-margin segments face chronic shortages? Will prices for everyday goods rise to untenable levels that the market cannot easily absorb? Will we see many manufacturers shut down once again?

These questions are the logical extension of a system already under strain. AI may be the industry's greatest opportunity in decades, but it is exposing the limits of the systems that support it.

Final Thoughts: The AI Era Will Not Be Evenly Felt

Just as Apple and its contemporaries reshaped global manufacturing decades ago, AI is doing it faster, and with more immediate consequences. This transformation is already revealing strain within the systems that support it, particularly across materials, manufacturing capacity, and global supply chains.

More than just growth, we see a reallocation of resources, priorities, and ultimately, of opportunity. However, that reallocation will not be evenly felt. Some segments will expand rapidly, while others may struggle to maintain footing. Some companies will successfully adapt, while others may be forced to rethink their place in the market.

I anticipate another busy era of mergers and acquisitions, and some companies will even close their doors. Entire portions of the supply chain will likely be reshaped in ways we do not yet fully understand. We may see a rebalancing of global production and economic influence as regions and companies adapt to shifting priorities and domestic incentives to bring manufacturing closer to home. But even in the best-case scenario, the transition will not be smooth or evenly distributed.

AI may well become the most transformative force our industry and our world has ever experienced, but it will not be painless. How much disruption can the system absorb, and who will bear the weight of that change when it does? These answers are just beginning to emerge, and they won't be for the faint of heart. **I-CONNECT007**

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2. "Copper-clad Laminate Market Size & Share Analysis – Growth Trends and Forecast (2026-2031), Mordor Intelligence.
3. "Printed Circuit Board Market Size & Share Analysis – Growth Trends and Forecast (2026-2031), Mordor Intelligence.

From Dilution to ZLD
Optimizing Used Process Water Management

Last month, we began discussing the journey from dilution to zero liquid discharge (ZLD). I highlighted that approximately 70% of the used process water (UPW) is generated from the dilute stream. This significant volume underscores the necessity for effective treatment processes that ensure the safe return of water into the production cycle while minimising environmental impact.

To this end, a multi-faceted approach is employed to treat the UPW and reclaim it for reuse.

The treatment process begins with advanced oxidation (AOX), a sophisticated technology designed to break down organic pollutants in the water. This method utilises powerful oxidising agents to generate hydroxyl radicals, which are highly reactive and effectively decompose organic contaminants. By deploying AOX, facilities can significantly reduce the levels of chemical oxygen demand (COD) and other harmful substances often found in process water.

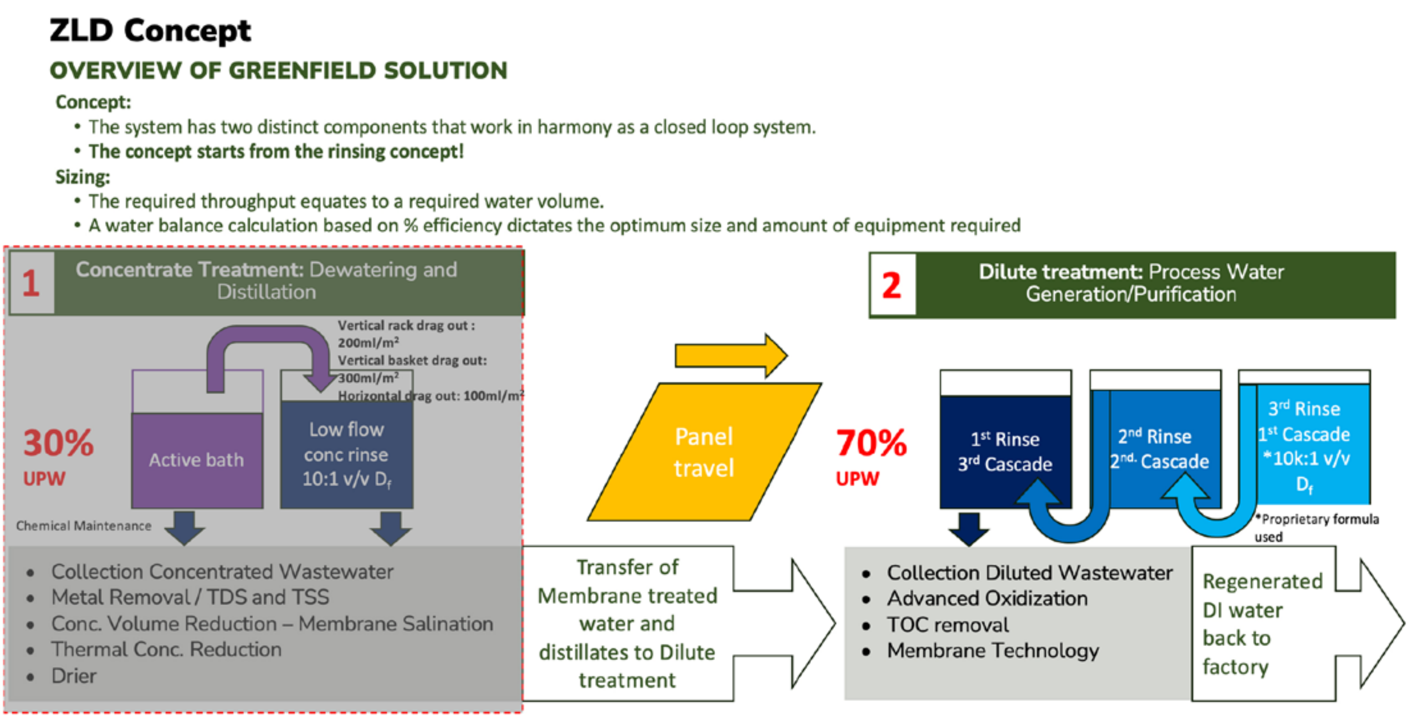

Figure 1: An overview of the major components to design a ZLD, closed-loop, water recycling system.

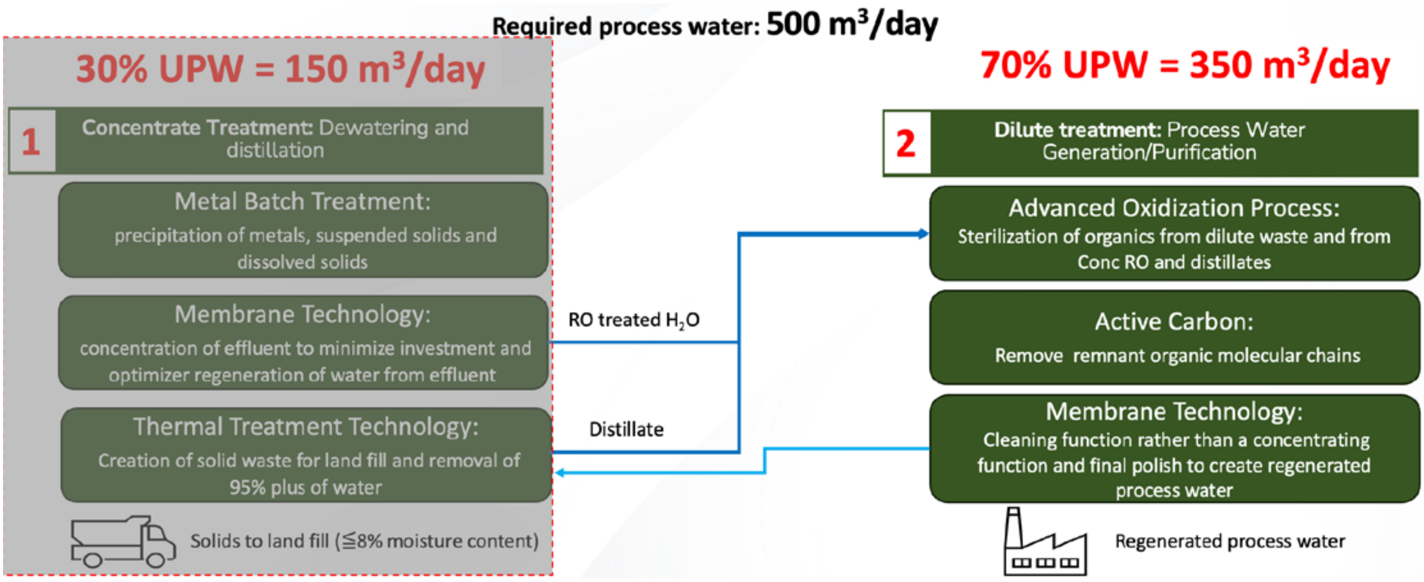

Figure 2: The planning of a 500m3/day ZLD system.

Case Study

Following AOX treatment, water is purified using granular activated carbon (GAC) and/or ion exchange (IX) media. The use of GAC is particularly noteworthy; the granules possess excellent adsorption properties, which allow them to attract and hold onto a broad spectrum of impurities, including dissolved organic compounds and chlorine, making it more suitable for various applications.

IX media, on the other hand, provide a different mechanism for water treatment. By exchanging undesirable ions in water with more benign ones, these systems can effectively reduce hardness and remove specific contaminants, such as heavy metals. The combination of GAC and IX media ensures a comprehensive treatment solution, capable of tackling a wide range of pollutants that may be present in the UPW.

Once through these initial purification stages, the water is subjected to reverse osmosis (RO) membrane technology, and is, by necessity, complemented by electro-deionization (EDI). RO is a highly effective method of filtration that uses a semi-permeable membrane to separate contaminants from water. It operates under pressure, allowing only water molecules to pass through while retaining larger molecules, ions, and impurities. The integration of EDI technology further purifies the water by continuously removing ionised species, producing ultra-pure water that meets stringent quality standards. The step has generated DI water with TOC>1 ppm and conductivity> 1 µS/cm at a flow rate of 18 m3/hour. These values meet even the most stringent PCB water quality requirements.

An essential aspect of this treatment process is managing waste. The reject streams generated by the GAC, IX media, and RO processes are returned to the concentrate waste stream evaporators. This step is critical to completing the overall water balance within the facility and ensures that the operational workflow is both efficient and sustainable. By recycling and managing waste effectively, industries can significantly reduce their environmental footprint, cutting down on the quantity of water extracted from natural sources and minimising the discharge of pollutants.

The entire process not only enhances water quality but also underscores the importance of sustainable practices in industrial settings. With increased regulations surrounding water usage and waste management, industries must adapt to these challenges while still maintaining operational efficiency. Implementing advanced water treatment technologies is no longer just an option; it is a necessity for any operation that values sustainability and regulatory compliance.

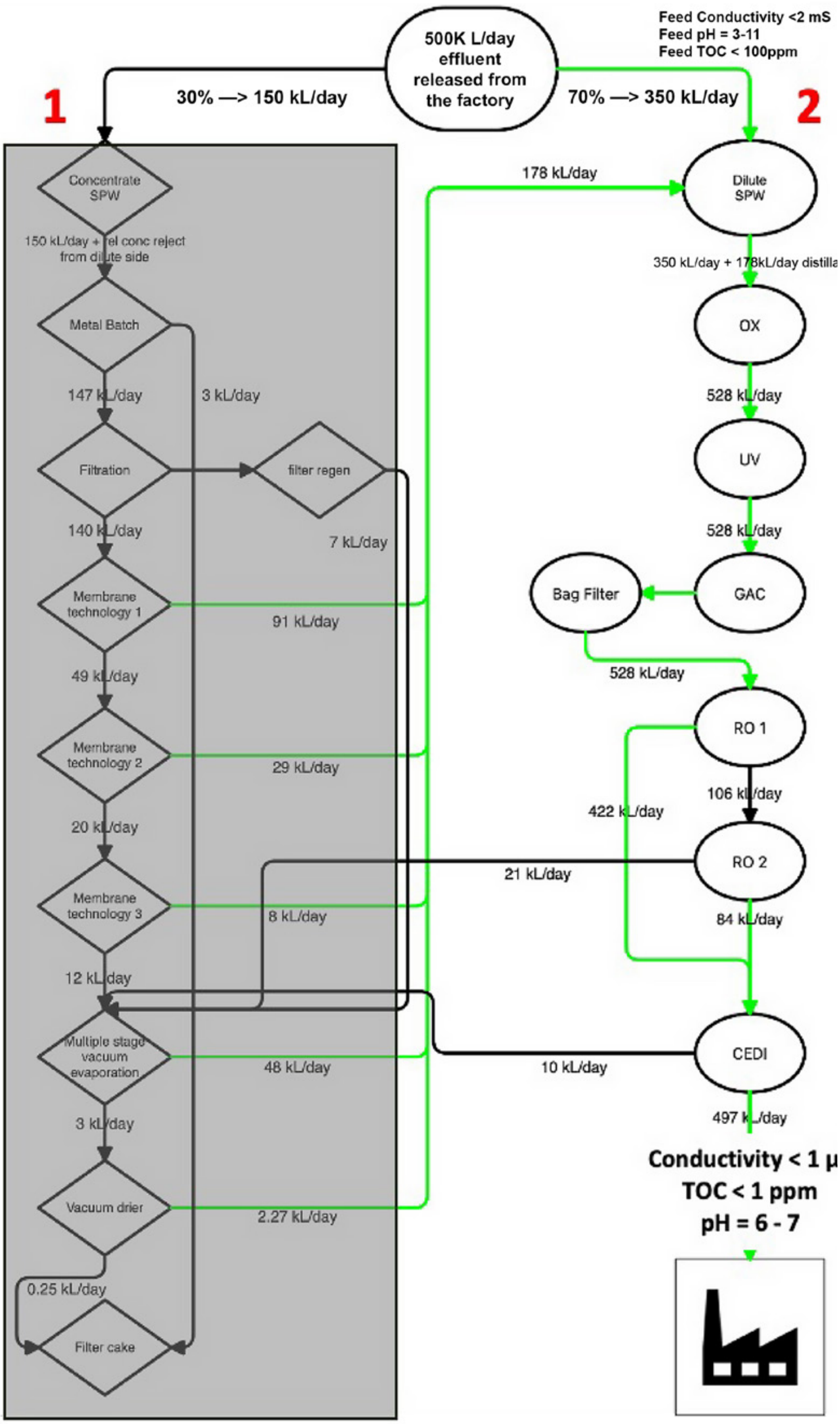

Figure 3: Flow diagram of the used process water treatment.

Conclusion

The treatment of used process water, particularly the 70% generated from the dilute stream, involves a sophisticated series of steps, from advanced oxidation to granular activated carbon and ion exchange media, ultimately culminating in reverse osmosis technology. Each stage plays a pivotal role in ensuring that the water is not only treated effectively but is also suitable for reuse in the industrial process.

For PCB or IC substrate fabricators looking to optimise their water management systems or seeking more information about implementing these advanced technologies, we invite you to reach out for further support. Embracing innovative water treatment solutions is essential for fostering a sustainable future, and we are here to help you navigate this vital journey. **I-CONNECT007**

Richard Nichols is technical marketing director at GreenSource Engineering. He can be reached at Richard.n@greensourceeng.com.

BY JAMES KIM, ARENTFOX SCHIFF LLP

How New Metals Tariffs Impact the Electronics Industry

Editor's note: Tariff Terminal is a new series exploring how trade policy, tariffs, and customs developments impact the electronics manufacturing industry. This is the first installment.

If you work in surface mount assembly, EMS, or anywhere along the electronics supply chain, you probably think of tariffs as something that happens upstream: raw materials, bulk commodities, maybe the occasional headache with Chinese imports. Steel and aluminum tariffs? That's someone else's problem.

Not anymore.

On April 2, President Trump signed a sweeping new proclamation that fundamentally restructures how Section 232 "national security" tariffs apply to steel, aluminum, copper, and their derivative products. The changes took effect on April 6, and the ripple effects are headed straight for the electronics industry.

A Quick Primer on Section 232

Since 2018, the U.S. has imposed tariffs on imported steel and aluminum under Section 232 of the Trade Expansion Act of 1962, a statute that allows the President to restrict imports that threaten national security. Over time, the program expanded to

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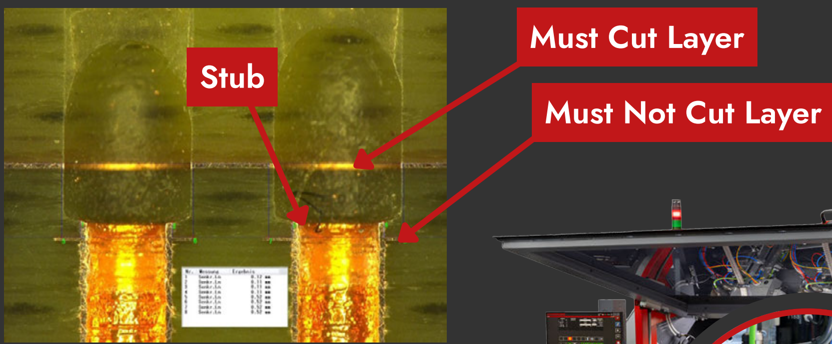

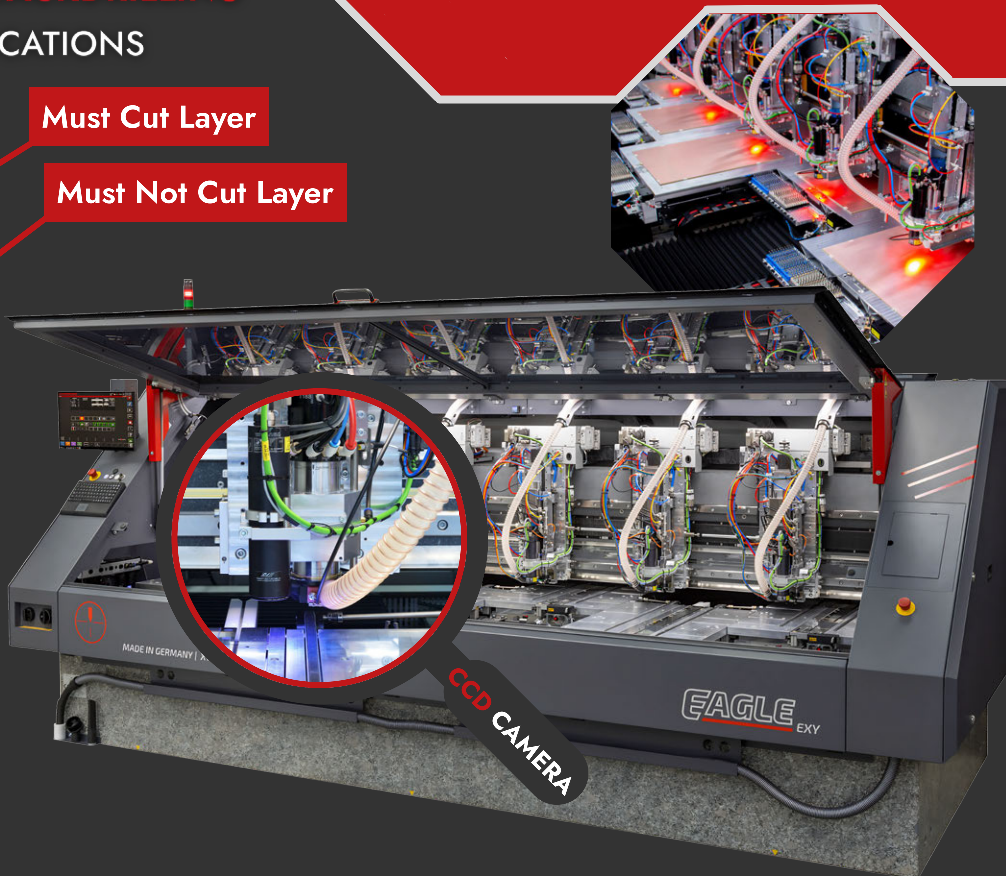

Back Drilling: stop of depth drilled hole before must-not cut layer within stub length tolerance

Depth Drilling: precise and reliable drilling to defined inner layers, enabling high-quality blind vias.

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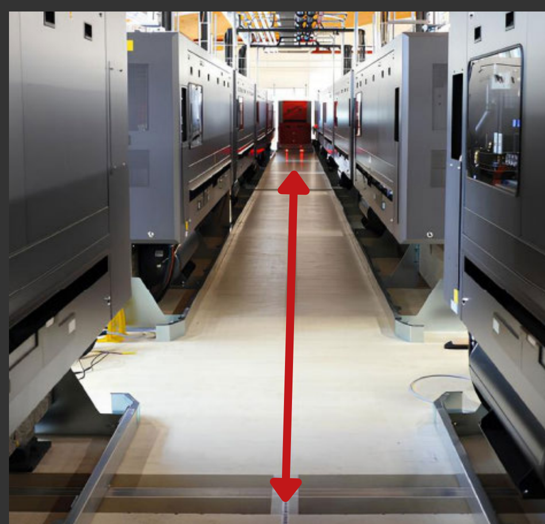


include copper and hundreds of "derivative" products: Goods that contain these metals but aren't raw metal themselves, such as cables, transformers, connectors, enclosures, and circuit board materials.

Under the old rules, importers of derivative products paid tariffs only on the metal content portion of the product's value. That meant if you imported a cable harness worth $100 and the copper inside it accounted for $30 of that value, you paid the tariff on $30. It was complicated to calculate, but for many electronics importers, it kept the duty bill manageable.

That system is gone.

Full Value, Full Impact

The new proclamation eliminates the metal-content methodology entirely. Now, Section 232 duties apply to the full customs value of the imported product. That same $100 cable harness? The 25% tariff now applies to the full $100, not just the $30 of copper. For products where the metal is a relatively small share of total value, which describes a lot of electronics, this is a significant increase in duty exposure.

The administration has organized covered products into a tiered structure. Primary metals and closely related articles are subject to a 50% tariff. A large category of downstream derivatives, including many electronics components, falls under a 25% rate. A temporary category of metal-intensive industrial and electrical grid equipment is eligible for a reduced 15% rate through Dec. 31, 2027, before stepping up to 25%.

So, What's Actually Affected?

For the SMT and EMS worlds, the new tariff lists capture a surprisingly broad range of products that move through electronics assembly operations every day:

- **Wire, cable, and harnesses.** Insulated conductors (the copper and aluminum wiring that connects everything) are now squarely in scope at 25% on full value. This includes everything from winding wire used in coil assemblies to finished cable harnesses with connectors.
- **Transformers and power conversion.** Both liquid-filled and dry-type transformers are covered at 25%. Power supply printed circuit assemblies, ferrite cores, and inductor components are on the temporary 15% list through 2027, a meaningful but time-limited reprieve.
- **Connectors, switches, and enclosures.** A wide swath of switching and connection devices, terminal blocks, boards, panels, and control cabinets now draw 25% on full value.
- **Copper foil and clad laminates.** This is the upstream gut punch. Copper foils and copper-clad laminates, foundational inputs for PCB fabrication, face the top-tier 50% rate with no de minimis escape. That cost pressure will flow through to laminate pricing across the industry.

The 15% Weight Escape Hatch

There is one important relief valve. For derivative products classified outside the primary metal chapters of the tariff schedule, which includes most electronics, Section 232 duties apply only if the covered metal accounts for at least 15% of the product's total weight. If the product falls below that threshold, the tariff doesn't apply.

This matters for mixed-material electronic assemblies. A data cable with lightweight copper conductors wrapped in heavy polymer jacketing might qualify. A printed circuit assembly where the FR-4 substrate dominates the weight could also clear the bar, but it's not likely for a power harness with heavy-gauge copper.

The catch is that you need to prove it. Importers claiming this exemption should expect scrutiny from U.S. Customs and Border Protection, including requests for a bill of materials and detailed weight breakdowns.

Supply Chain Tremors Ahead

These changes will reshape sourcing decisions. Electronics supply chains have been diversifying toward Southeast Asia and Mexico for years, driven by the China Plus One strategy. But Section 232 tariffs apply on a most-favored-nation basis. Unlike the China-specific Section 301 tariffs, these tariffs generally apply to imports regardless of origin. Moving production to Vietnam or Thailand doesn't sidestep Section 232.

That said, the temporary 15% rate on power supply PCAs and magnetics components creates a narrow window for companies to adjust. If your sourcing strategy includes products on the temporary list, the clock is already ticking toward 2028 when those rates jump to 25%. Now is the time to evaluate designs, classify your products accurately, and model cost scenarios under both the current and future rate structures.

What Comes Next

The new Section 232 framework is broader and simpler in some ways, and more expensive in many others. For an industry that already operates on thin margins, the shift from metal content to full-value assessment is not a rounding error but a material change in the cost of doing business.

In the next installment, I'll dig deeper into compliance strategies, documentation best practices, and how the new tariffs interact with other trade measures affecting electronics imports. In the meantime, if you haven't already mapped your product lines against the new tariff annexes, that should be at the top of your to-do list. The rules have changed, and for this industry, the stakes are higher than most people realize. **I-CONNECT007**

James Kim is an international trade lawyer at ArentFox Schiff LLP.

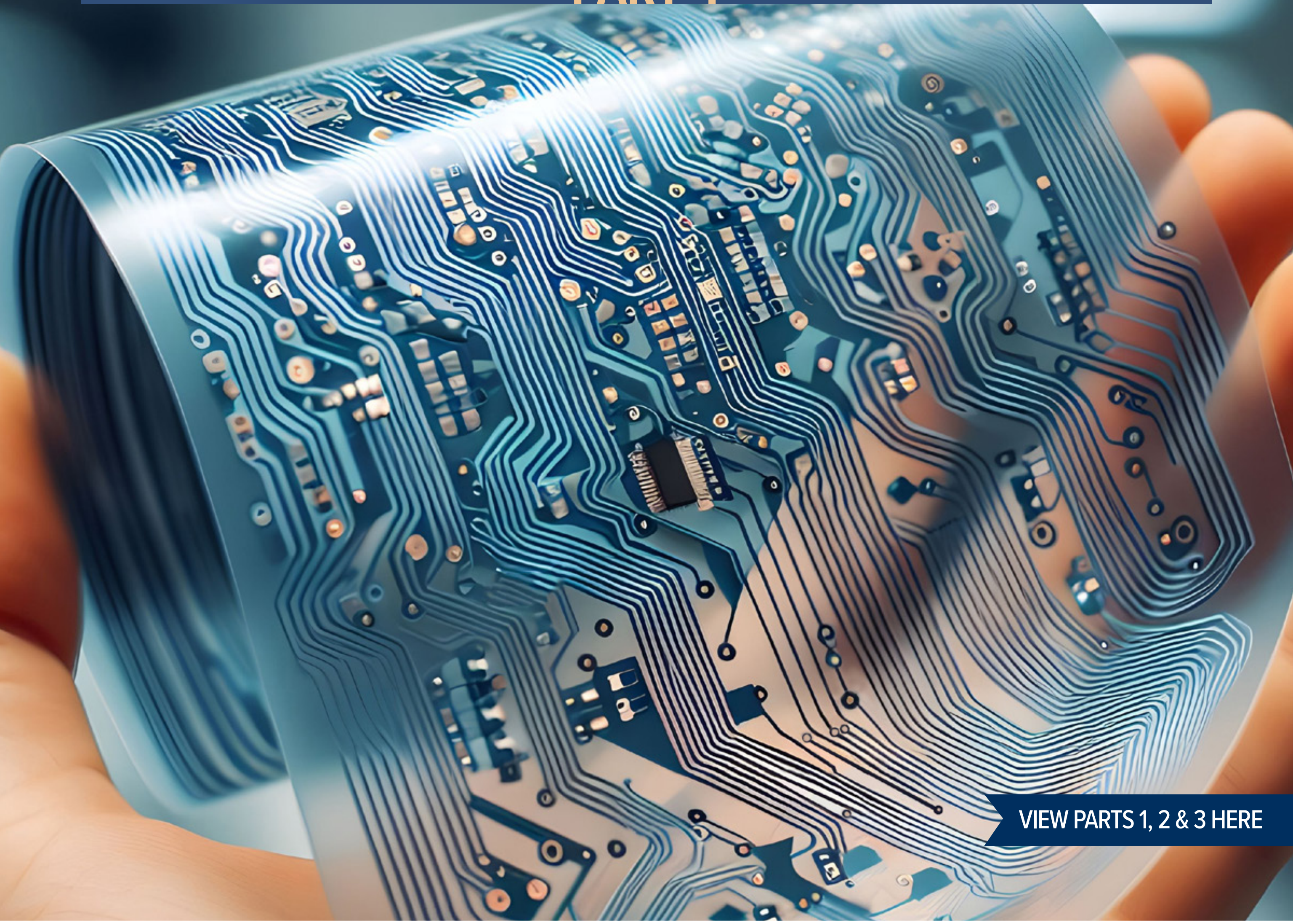
Roundtable: Data Protection Lays the Groundwork for Cybersecurity Strategies

This multi-expert roundtable explores cybersecurity measures specific to electronics manufacturing. NEC's Hiroyuki Watanabe, Divyash Patel, CEO of MX2 Technologies, and Ali Pabrai, CEO at EC First, join moderator Nolan Johnson for a deeper discussion on cybersecurity certifications.

BY ANAYA VARDYA, AMERICAN STANDARD CIRCUITS

Manufacturing Readiness and Scaling Flex-Packaging Integration

PART 4



VIEW PARTS 1, 2 & 3 HERE

Parts 1–3 of this series examined the technical foundations, application landscape, and strategic imperatives surrounding the convergence of flexible PCBs and advanced semiconductor packaging. Part 4 turns to the factory floor: What must change in manufacturing processes, equipment, and quality systems to bring this convergence from prototype to production scale?

Process Readiness at the Flex–Package Interface

The assembly of advanced packages onto flexible substrates demands process controls that exceed conventional PCB manufacturing norms. Fine-pitch solder deposition, controlled-atmosphere reflow, and precision placement must all be adapted for inherently compliant substrates.

Key process gaps that manufacturers must address include:

- Stencil design for ultra-fine pitch on flex, where substrate deflection affects paste volume consistency
- Fixture and carrier systems that maintain dimensional stability during reflow without constraining flex behavior
- Underfill dispensing processes calibrated for the compliance mismatch between silicon packages and polymer substrates

Equipment Investment and Qualification

Scaling flex–packaging integration requires targeted capital investment. High-accuracy pick-and-place systems with active vision correction, laser-based soldering for heat-sensitive areas, and advanced AOI systems capable of inspecting warped or curved surfaces are among the equipment upgrades most commonly required. Qualification of this equipment against hybrid assembly specifications, not traditional PCB or package-level standards, is essential before production launch.

Quality Systems and In-Process Control

Quality management for hybrid flex–package assemblies must evolve beyond legacy approaches. Effective in-process control strategies include:

- 3D SPI (solder paste inspection) adapted for flex substrate topology
- Post-reflow X-ray inspection of BGA and LGA joints on compliant surfaces
- Mechanical bend and thermal cycle qualification protocols specific to the flex–package assembly

Conclusion

The technology case for flex–packaging integration is well established. The remaining challenge is execution at volume. Manufacturers who invest now in process development, equipment qualification, and adapted quality systems will be positioned to serve the growing wave of demand from automotive, medical, and high-performance computing customers. Production readiness, not just design capability, is the next frontier for this convergence. **I-CONNECT007**

Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals*. He is the author of *Thermal Management: A Fabricator's Perspective, The Printed Circuit Designer's Guide to DFM Essentials*, and *The Companion Guide to Flex and Rigid-Flex Fundamentals*.

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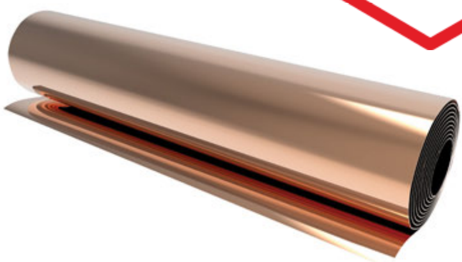

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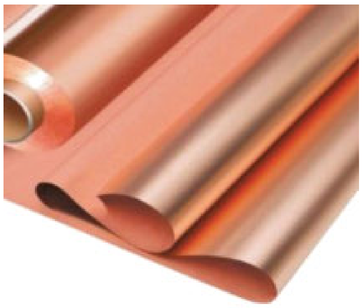

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Rethinking Reinforcement Materials
for Advanced Packaging

BY IVANA IVANOVIC, FLEXIRAMICS


Ivana Ivanovic

Materials that once quietly supported the industry are now becoming limiting factors. The electronics industry is experiencing unprecedented pressure as RF systems push into mmWave frequencies, high-speed digital architectures advance into their next performance generation, and power densities climb across automotive, telecom, aerospace, and computing. Reinforcement materials, long treated as a background detail in laminate design, are suddenly at the centre of performance, reliability, and supply chain discussions.

For decades, glass fiber has been the default reinforcement platform for substrates and laminates. It is familiar, available, and deeply integrated into manufacturing. But the demands placed on electronics are no longer aligned with the properties of glass. Thermal bottlenecks, frequency-dependent loss, dielectric variability, and supply chain fragility are forcing engineers and material suppliers to reconsider what reinforcement should be, and what it must enable.

This article explores why reinforcement materials are under scrutiny, how thermal and frequency challenges are reshaping substrate design, and why the industry should evaluate new reinforcement platforms, including flexible ceramic nonwovens, as a path forward for next-generation electronics.

Reinforcement as a Performance Driver

When engineers think about improving signal integrity or thermal performance, they often focus on resin chemistry, copper roughness, or stackup design. Reinforcement rarely gets top billing, yet reinforcement fibers influence nearly every critical property of a laminate, such as dielectric constant and loss, thermal conductivity and heat spreading, mechanical stability, dimensional control, manufacturability, and yield.

Glass fiber has supported the industry for decades, but RF/mmWave and high-speed digital systems are pushing materials into new performance regimes. As frequencies rise and thermal densities increase, reinforcement becomes an active design parameter rather than a background choice. This is why the industry is exploring new materials.

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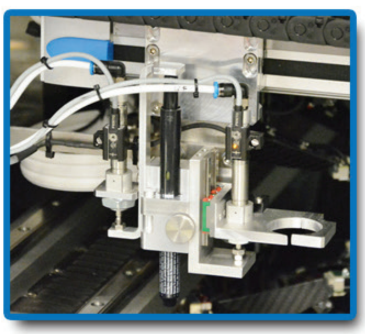

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Everspin Executes $40M Agreement for Mil-Aero MRAM Applications ▶

Everspin Technologies, Inc., the world's leading developer and manufacturer of Magnetoresistive Random Access Memory (MRAM) persistent memory solutions, announced an agreement with a U.S. prime contractor to provide state-of-the-art Toggle MRAM process technology capabilities and engineering services for U.S. Defense Industrial Base customers.

AMETEK Announces Agreement to Acquire First Aviation Services ▶

AMETEK, Inc. announced that it has entered into a definitive agreement to acquire First Aviation Services, a leading provider of highly engineered, mission-critical defense and aviation maintenance, repair and overhaul (MRO) services and a manufacturer of related proprietary components.

RTX's Raytheon Delivers Second Missile-warning Sensor to U.S. Space Force ▶

Raytheon, an RTX business, has delivered its second sensor to Lockheed Martin for the U.S. Space Force's Next-Generation Overhead Persistent Infrared (Next-Gen OPIR) Geosynchronous Earth Orbit (GEO) Block 0 satellite program. The satellites, commonly referred to as NGG, will provide enhanced missile warning and tracking to address evolving space-based threats.

NASA's Perseverance, Curiosity Panoramas Capture Two Sides of Mars ▶

NASA's Curiosity and Perseverance rovers have captured two 360-degree landscapes that highlight how the missions are revealing details of the Red Planet's formation, watery past, and potential for life. Located 2,345 miles (3,775 kilometers) apart from each other on Mars—about the distance from Los Angeles to Washington, D.C.—both rovers are exploring areas that are billions of years old. But as the nearly 15-year-old Curiosity reaches ever-younger terrain in the foothills of Mount Sharp, the 5-year-old Perseverance is venturing into some of the oldest landscapes in the entire solar system.

Sikorsky, Robinson Unmanned Win U.S. Marine Corps Autonomous Logistics Contract ▶

The U.S. Marine Corps awarded a $15.5 million contract to Sikorsky, a Lockheed Martin company, for the Medium Aerial Resupply Vehicle–Expeditionary Logistics (MARV-EL) Increment 2 program. The offering selected for award is the R66 TURBINETRUCK, an autonomous cargo helicopter commercially developed by Sikorsky and Robinson Unmanned that combines Sikorsky's proven MATRIX™ autonomy system with the rugged R66 airframe from Robinson Helicopter Company to provide flexible, affordable and rapid combat sustainment.

Peru Selects Lockheed Martin F-16 Block 70, Strengthening Sovereignty and U.S. Partnership ▶

Lockheed Martin welcomes the Government of Peru's announcement to purchase 12 new F-16 Block 70 aircraft to modernize the nation's fighter fleet and strengthen its national defense capabilities. The F-16 will provide Peru with a proven, highly capable, and interoperable multirole fighter aircraft that enhances air sovereignty, supports regional security, and enables long-term operational readiness.

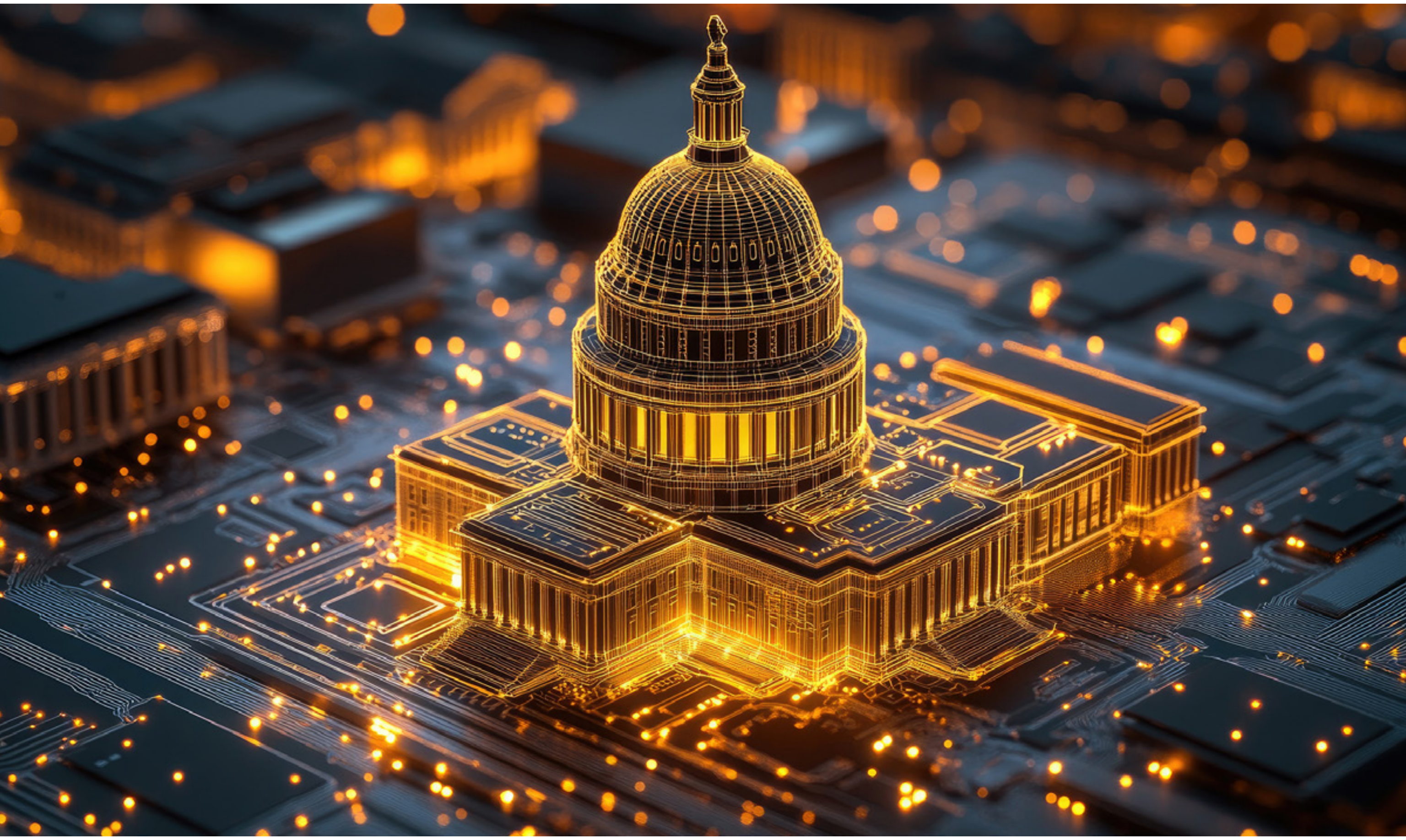
Boeing, U.S. Navy Achieve Successful MQ-25A Test Flight ▶

Boeing and the U.S. Navy have successfully completed the first test flight of an operational MQ-25A Stingray™. The milestone advances the Stingray closer to aircraft carrier operations and marks the beginning of a new era in naval aviation.

Meet Emerging Engineer Dennis Donovan, Kratos Space Commercial ▶

Like many of today's engineers, Dennis Donovan grew up interested in how things worked. He wanted to see what was inside and how to make it better. Now, he has three bachelor's degrees, is earning his master's, and works as an electrical engineering technologist. He aspires to work in PCB assembly with a particular focus on aerospace electronics.

Five Years of Educating, Advocating, and Influencing Legislation and Policy



BY **SHANE WHITESIDE,** PCBAA

Five years ago, five companies decided that the PCB industry needed its own voice in Washington. The Printed Circuit Board Association of America was created largely in response to the fact that PCBs were not included in the CHIPS Act legislation.

Starting an advocacy organization from scratch, attracting members, and making an impact in Washington's crowded infosphere is no small feat. A small core team and volunteers serving in executive positions dug in and put PCBs on the map. At PCBAA, we are grateful to everyone who has participated and made our first five years a resounding success.

Getting attention is not easy for an electronic component that is not known or understood outside the industry. Our core strategies have been delivering the industry trade and mainstream media a steady flow of information resulting in supportive coverage, educating our elected representatives

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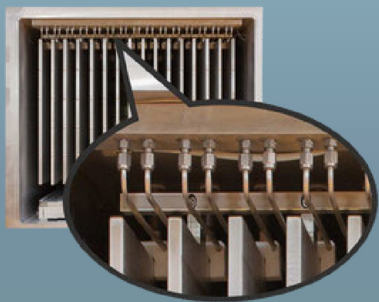

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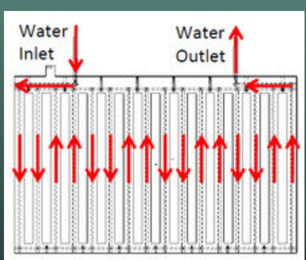

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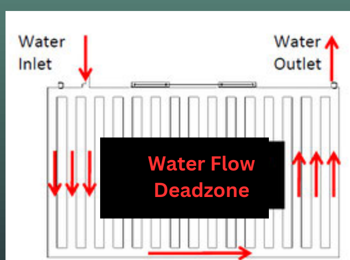

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on the criticality of PCBs, participating in PCB trade shows, activating members to write opinion editorials in regional newspapers, appearing on influential podcasts, writing and submitting draft legislative language for major bills, and drafting and managing the introduction of the Protecting Circuit Boards and Substrates (PCBS) Act in the House of Representatives which will soon have a Senate companion bill.

PCBAA executives have met with the Senate Armed Services Committee staff and Department of Defense (War) officials responsible for the health of the Defense Industrial Base to provide factual data to inform policy. PCBAA has also made significant inroads with the Department of Commerce to educate and advocate for supportive policy for our industry by inviting staff to visit member companies to get a firsthand look at what happens on the front lines of the PCB industry, and by providing access to our members to participate in extensive studies by the Department of Commerce.

We have grown from the original five members to almost 100 because the value proposition of PCBAA membership is worth the investment. We provide members with weekly industry intelligence, periodic video meetings with government officials, a monthly newsletter, and help with their outreach with elected officials. PCBAA holds a first-class annual meeting in Washington each year, featuring high-level speakers from Congress, think tanks, and government agencies, along with a day on Capitol Hill meeting with our members' representatives. This year's Annual Meeting is June 16–18, and we encourage you to join our team and attend.

This year, PCBAA collaborated with the Alliance for American Manufacturing to produce "The New Frontier," a documentary film on the PCB industry, which has drawn more than 3,000 viewers, gained significant notice in the trade press and has been submitted for several awards. Our movie premiere in Washington, D.C., at The Miracle Theatre was well attended by Congressional staff, media, and members.

The business and political environment is in the midst of radical change. There are strong tailwinds for Defense as we support restocking the munitions expended in the Iran war. Advanced PCBs are also critical for AI data center servers, and there is significant interest and analysis ongoing by our government to assess our nation's PCB manufacturing capacity to support these initiatives.

Challenges remain, and through the efforts of our PCBAA staff and dedicated members, we have seen significant traction for our call to reshore and restore the PCB industry to support our national and economic security. To learn more about our mission and consider joining this growing coalition, I encourage you to visit pcbaa.org. **I-CONNECT007**

Shane Whiteside is president and CEO of Summit Interconnect and current chair of the Printed Circuit Board Association of America. To read past columns, click here.


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BY SEAN PATTERSON, CROSSGEN AI

Part 1

Don’t Buy AI, Learn It

A Fabricator’s Guide to Getting Started

The first hard truth about AI in PCB fabrication is that you can buy software, but you cannot buy capability.

You can sign a contract, schedule demos, put a few logos on a slide, and tell your team you now have an AI strategy. Plenty of companies are doing some version of that right now. But if the people in your plant do not know how to use AI in real work, then your purchase was more akin to buying a gym membership and never going. (Don’t take that as criticism; it’s just how it works.)

In our industry, we have seen plenty of software promises, where we bought into systems that were supposed to make quoting easier, communication tighter, or production more predictable. Sometimes they helped, but sometimes they also created new work. I understand the skepticism, and I am not asking you to suspend that skepticism for AI.

I want to point you in the right direction, so instead of asking, “What AI package should we buy?” say, “How do we help the people in our plant become more capable with the tools that are

already available to them?"

Over the coming months, I will walk you through this in a practical way. I'll show you how to use AI in a real fab for a better RFQ review, cleaner shift handoffs, stronger CAPA drafts, clearer supplier comparisons, faster SOP cleanup, and better thinking when something starts going sideways in the process.

Remember, I'm learning, too. Even though I've spent a lot of time using and teaching AI in manufacturing environments, I still find new ways to get an edge every week. Those getting the most from AI are usually not the ones making the biggest claims. They are the ones using it daily, checking its work, and getting better.

The Moment Most Fabs Will Recognize

Picture a typical morning in a PCB shop. A customer package came in late yesterday. The print is not terrible, but it leaves enough ambiguity to create risk. One person in receiving is deciding whether the board really fits your standard capability window. Someone else is drafting clarification questions. Operations wants to know whether this job will become a hot lot in three days. Quality is already thinking ahead to what could go wrong if the requirements get interpreted differently by different people. Meanwhile, there's an open defect investigation from yesterday, a supplier email waiting on a response, a shift handoff note written too fast, and an operator instruction that everyone "knows" but nobody has cleaned up in writing.

That's a PCB fabrication workday, and it is exactly why AI matters here. Not because it should run your process, tell you what the IPC specs say from memory, or replace the judgment of your best process engineer, quality manager, buyer, or ops lead, but because a plant produces a constant stream of work that must be interpreted, summarized, clarified, structured, and communicated effectively. It's where AI is immediately useful.

What Most People Miss

Most AI conversations in manufacturing start too high. They jump straight to automation, platforms, big roadmaps, and enterprise rollouts. That is understandable. Leaders are supposed to think at the system level. Most people miss that AI adoption is personal before it is organizational. It is non-delegable.

If you are a VP of operations, learn AI yourself. The same goes for the process engineer, quality engineer, buyer, and production control lead. Don't outsource your own understanding. Develop the habit of knowing when to use it, how to frame a problem, how to spot a weak answer, and how to ask a better follow-up question.

It's why I keep coming back to this phrase: Don't buy AI, learn it. Two fabs might pay for the same tool, but the difference will come from the people who know how to use it on their own work.

Start Where the Risk Is Low, and the Value Is Visible

For Month 1, don't use AI to set process parameters, interpret customer requirements without review, or quote IPC criteria from memory. Use it where the work is real, the output is reviewable, and the risk is low. Here are a few fabrication-specific starting points that make sense right now.

1. RFQ Clarification and Requirement Review

A surprising amount of pain in a plant starts before the job ever hits the line. Ambiguity early becomes scrap, delay, rework, or customer frustration later. AI is useful here because it can help you read a package, summarize what is being asked, and surface missing information. It's not deciding for you, but helping you think.

2. CAPA (Corrective Action, Preventive Action) and 8D First Drafts

Most quality teams do not struggle because they lack structure. They struggle because they have rough notes, incomplete facts, too many interruptions, and not enough time to turn those into a clean draft. AI is very good at helping you turn messy input into an organized first version, and that matters because a first draft is often the hardest part.

3. Troubleshooting Checklists

When an issue arises in imaging, etching, plating, solder mask, or electrical testing, the first challenge is the structure. What changed? When did it start? What products are affected? Which equip-

Your Assignment: Try One of These Four Prompts This Week

Prompt 1: RFQ Clarification

- **Context:** I work at a PCB fabrication shop, and I'm reviewing a new customer package for a multilayer rigid board.
- **Role:** Act like a senior PCB fabrication product engineer.
- **Interview:** Ask me questions one at a time before making recommendations.
- **Task:** Based on the information I provide, summarize the board requirements and generate a list of clarification questions before quoting.

This prompt works because it helps sales, engineering, quality, and operations all at once, and it reduces the odds that important ambiguity gets buried in email.

Prompt 2: CAPA First Draft

- **Context:** I'm a quality engineer in a PCB fabrication shop. I have rough notes from a defect investigation and a customer complaint.
- **Role:** Act like an experienced PCB quality engineer familiar with CAPA and 8D structure.
- **Interview:** Ask me for missing facts one at a time before drafting.
- **Task:** Turn my notes into a structured first draft of a corrective action report. Clearly mark assumptions, missing information, and open questions.

This prompt works because it turns scattered information into something usable without pretending the answer is finished.

ment, chemistry, maintenance, material lots, or handling conditions align with the timing? AI can help build a disciplined investigation outline, so your team starts stronger.

4. Supplier Comparisons

Buyers and engineers spend a lot of time comparing laminate options, chemistry notes, technical data, lead-time communication, change notices, and basic commercial differences. AI can organize this faster and often more clearly than we can by hand on a rushed Tuesday. That matters to more than procurement; better supplier comparisons improve risk visibility for engineering, operations, and leadership before a material or vendor decision turns into a schedule problem.

5. Shift Handoffs and Production Summaries

This one is more powerful than it sounds. A rough handoff can create a bad day for the next shift. AI can take shorthand notes and turn them into priorities, risks, open issues, and escalation items. That is not flashy. It is useful.

6. SOP Cleanup and Tribal Knowledge Capture

Many fabs are full of instructions that exist partly in a binder and partly in someone's head. AI can help rewrite procedures into clearer language, identify steps that need clarification, and even help you interview your veterans so the real know-how becomes easier to document. That is a meaningful use of AI because it strengthens the organization without pretending the tool is the expert.

A Simple Way to Prompt: CRIT

In this series, I will be using a prompt structure called CRIT:

- **C** is for Context: What kind of fab, role, or problem?
- **R** is for Role: What expertise do you want the AI to bring to the conversation?
- **I** is for Interview: Asking the AI to ask you questions one at a time before answering.
- **T** is for Task: What output do you want?

Prompt 3: Shift Handoff Cleanup

- **Context:** I manage PCB plant operations and need to hand off critical issues from one shift to the next.
- **Role:** Act like an operations coordinator in a PCB fabrication environment.
- **Interview:** Ask me what jobs, delays, equipment issues, and quality concerns matter most.
- **Task:** Convert my raw notes into a clear shift handoff with priorities, risks, and escalation items.

This prompt works because small communication improvements often have bigger operational value than people expect.

Prompt 4: Supplier Comparison

- **Context:** I'm comparing two laminate or chemistry suppliers for a PCB fabrication shop.
- **Role:** Act like a supply chain leader who understands PCB plant constraints.
- **Interview:** Ask what attributes matter most to us before evaluating.
- **Task:** Build a comparison table and flag where I still need to verify manufacturer data.

This prompt works because it gives supply chain, engineering, and leadership a common starting point without hiding the need for human review.

That third step matters more than most people realize. If you skip the interview step, people often use AI like a search engine: They throw a question over the wall and hope for something useful. But AI gets much better when it becomes a thought partner. That means it should ask you questions, pull context out of you, and make you think more clearly before it drafts anything.

The Rule You Cannot Skip: Verify Everything That Matters

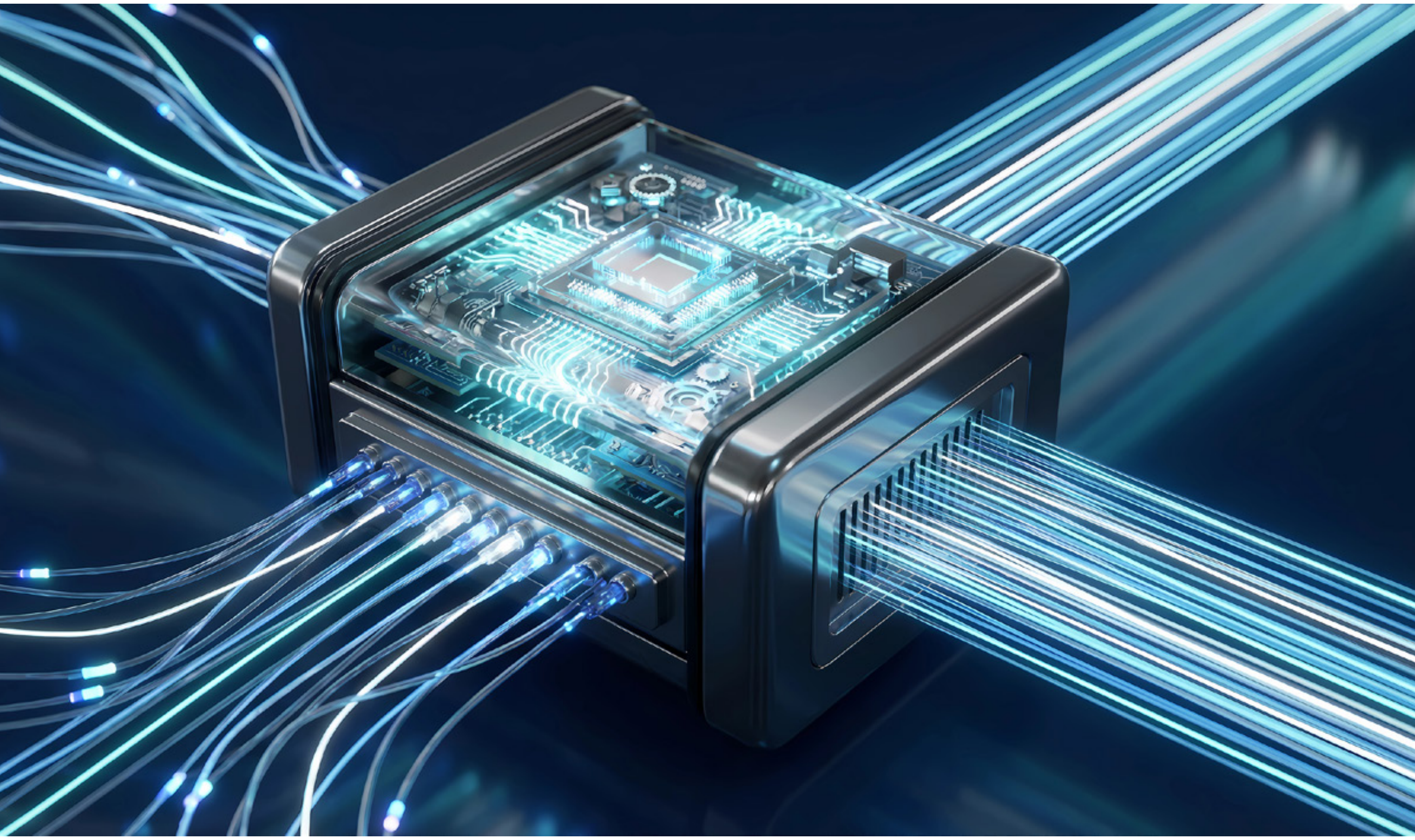
AI is useful, not authoritative, and that matters a lot in PCB fabrication. If the output touches IPC criteria, customer requirements, process limits, chemistry targets, equipment settings, acceptance criteria, or anything else that can affect quality, compliance, or yield, you must verify it against the real source. Check the actual standard, customer spec, and your actual process sheet and equipment documentation.

Use AI to structure your thinking, draft your communication, and help you ask better questions. Do not treat it like a final authority on your shop. This is one of the reasons I believe AI can fit manufacturing well when used correctly.

In Part 2, I'll provide a fabricator's guide to getting started with AI. I-CONNECT007

Sean Patterson is the founder of CrossGen AI. He previously served as COO and CTO at Summit Interconnect, held senior multisite roles at TTM Technologies, and was CRO of Nano Dimension, a former Amazon executive and U.S. Navy Submarine Veteran.

How Signals Survive the Hostile PCB Environment



BY BARRY OLNEY, IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

Modern digital signals exhibit behavior more characteristic of RF waveforms than the slow logic transitions of the past. With fast rise times, a PCB is no longer a collection of copper traces, but a distributed electromagnetic system. Successful design isn't about routing signals anymore; it's about engineering transmission lines, preserving uninterrupted return current paths, and controlling the resonant structures that naturally form within the multilayer PCB.

Rise time, not clock frequency, is the real driver of signal behavior, dictating when reflections, ringing, and RF-like effects emerge. At fast edge speeds, every trace becomes a transmission line with its own characteristic impedance and propagation behavior. Understanding these interactions

is essential for optimizing high-speed digital designs, ensuring reliable performance, and minimizing electromagnetic interference. This approach shifts the design paradigm from simple routing to sophisticated electromagnetic management, crucial for modern high-speed electronic systems.

Arguably, the most critical factor in high-speed PCB design is the impedance of the interconnect. Controlled impedance is the foundation of the design's integrity. It forms the essential baseline, as reflections, terminations, return-current behavior, and even plane interactions all assume a stable, controlled impedance along the interconnect.

Impedance is at the core of the methodology that is used to solve signal integrity issues:

1. Signal quality issues arise because voltage signals reflect and are distorted whenever the impedance changes along a transmission line.

2. Crosstalk arises from the coupling of electric and magnetic fields between adjacent traces or between traces and return paths. The inductance and capacitance between the traces establish an impedance that determines the amount of coupling.

3. Differential-mode propagation can be converted to common mode by parasitic capacitance or by any imbalance caused by impedance variation, signal skew, rise/fall-time mismatch, or channel asymmetry. Common-mode currents are the main source of electromagnetic radiation.

The iCD Stackup Planner, in Figure 1, illustrates the three most common transmission line structures of a multilayer PCB. For embedded microstrip (solder mask-coated microstrip), the electromagnetic field propagates partially in the dielectric material, the solder mask, and the air. Whereas, in both stripline structures, the electromagnetic field propagates in the dielectric material sandwiched between the planes.

A characteristic impedance of 40–60 ohms is typically used for a digital design. However, this value becomes more critical as the edge rates become faster. Also, different technologies have their specific impedance requirements. For example, Ethernet is 100 ohms differential, USB is 90 ohms differential, DDR2 memory is 50/100 ohms single-ended/differential impedance, and DDR3-5 is 40/80 ohms single-ended/differential impedance. So, controlling impedance simultaneously across each signal layer with multiple technologies can be challenging. Also, as operating voltages are reduced, the associated noise margins are also reduced, making it even more important to match the impedance.

Once we define the characteristic impedance, the next challenge is ensuring the signal actually sees that impedance along its entire path. When a transmission line is perfectly matched to the driver and load, the signals propagating electromagnetic (EM) energy are totally absorbed by the load. This is the perfect scenario that all electronics designers strive for.

UNITS: mil | 12/2/2019 | Total Board Thickness: 44.2 mil

Differential Pairs > 50/100 Digital | 40/80 DDR3 | 90 USB

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5							
1	8 8 4 4	Signal	Top	Conductive			2.2	12	4	0.43	51.67	98.65	Embedded
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9							Microstrip
2		Plane	GND	Conductive			1.4						
		Core		370HR; 1-7628; Rc=42% (1GHz)	4.4	7							Asymmetric
3		Signal	Inner 3	Conductive			1.4	10	4	0.31	53.26	99.85	Stripline
		Prepreg		370HR; 7628; Rc= 50% (1GHz)	4.19	8							
4		Plane	PWR	Conductive			1.4						
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
5		Signal	Inner 5	Conductive			1.4	16	4	0.31	51.23	99.63	Dual 48.89
		Prepreg		370HR ; 2116 ; Rc= 56% (1GHz)	4.14	4.8							Symmetric
6		Signal	Inner 6	Conductive			1.4	16	4	0.31	51.23	99.63	Stripline 48.89
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
7		Plane	GND	Conductive			1.4						

Figure 1: Microstrip, asymmetric and dual symmetric stripline configuration. (Source: iCD Design Integrity)

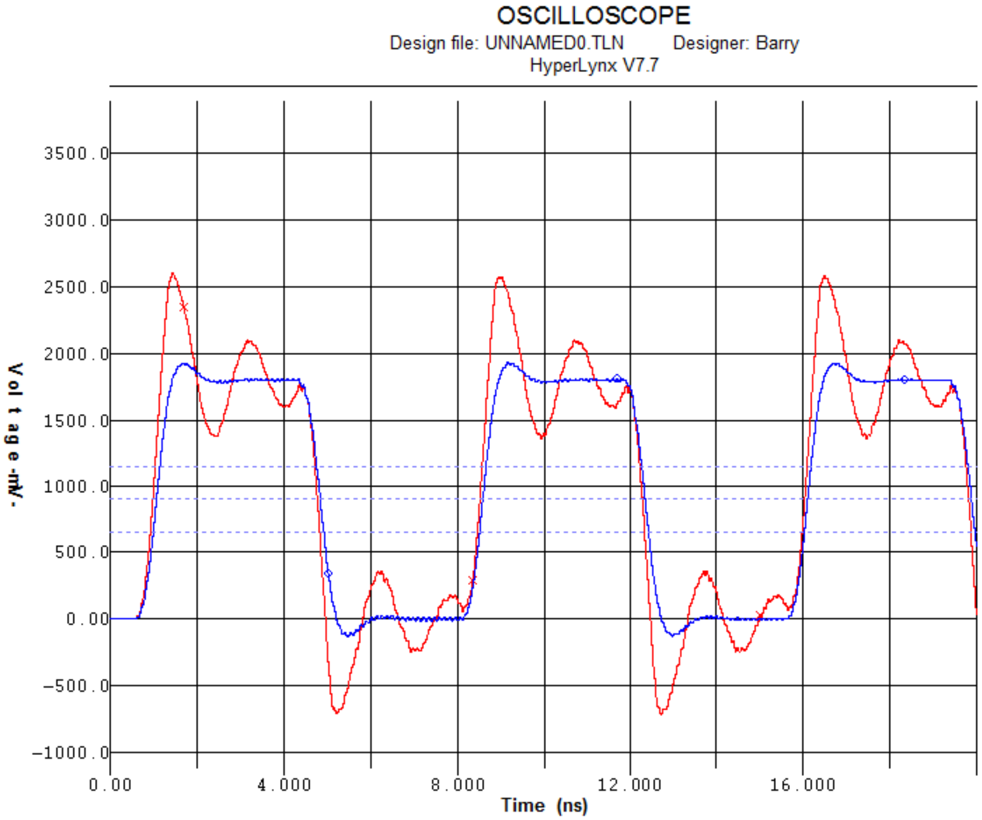


Figure 2: Unmatched (red) vs. matched (blue) transmission lines.

Unfortunately, drivers do not have the same impedance as the transmission line (typically 10–35 Ω), so series terminations are used to balance the impedance, match the line, and minimize reflections, particularly on long traces where on-die termination is not provided. Impedance matching slows down the rise and fall times, reduces the ringing (over-/undershoot) of signal drivers, and enhances the quality of a high-speed signal. The ringing is dramatically reduced by adding a series terminator as in Figure 2. From this, we can see that the impedance has to be matched, but to what value?

In Figure 3, using a 12 mA LVCMOS 1.8V driver of a Spartan 6 FPGA, an 18.7 Ω series resistor is required to match the driver to the 51.67 Ω trace on the outer layer. This is automatically derived from the IV curves of the Spartan 6 IBIS model by the iCD Termination Planner.

When a signal's electromagnetic energy propagates from the driver to the receiver along a transmission line, it changes along its length. The original signal will be received with varying degrees of distortion and degradation. This signal distortion happens due to factors such as impedance mismatch, reflections, ringing, crosstalk, dielectric loss, jitter, and ground bounce. The PCB designer's primary objective should be to minimize these issues at the source, so that any signal distortion is eliminated. But unfortunately, even with perfect impedance and termination, a signal can still be corrupted if its return current is forced to take a detour.

Another culprit is crosstalk, particularly on long parallel trace segments. Crosstalk arises as a result of the unintentional coupling of electromagnetic fields and causes both forward and reverse reflections. The easiest way to reduce crosstalk from a nearby aggressor signal is, of course, by increasing the spacing between the signals in question. Crosstalk falls off very rapidly with distance, plummeting roughly quadratically with increased separation. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level. A good rule of thumb for this is Gap = 3x trace width. However, in today's complex designs, it is not always possible to use up valuable real estate to satisfy the


Hmm, what is recommended **minimum distance for copper to board edge?**

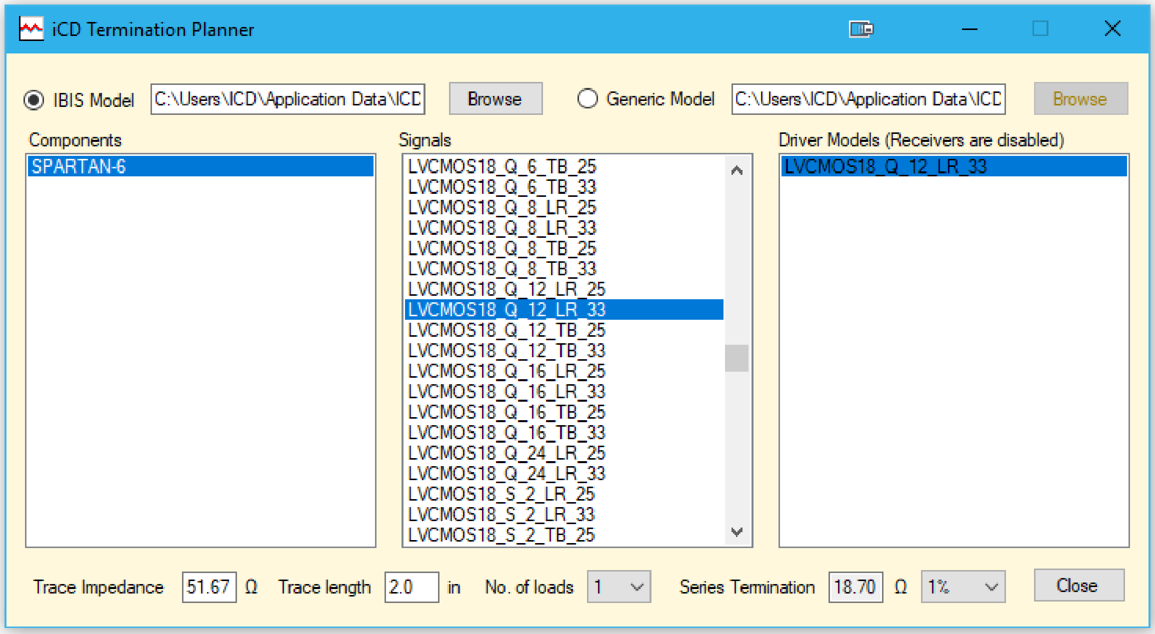


Figure 3: Matching the Spartan 6 driver to the transmission line. (Source: iCD Termination Planner)

above. Reducing the signal trace to reference plane dielectric thickness can also reduce crosstalk while not requiring additional space. Also, different technologies should not be mixed as higher voltages create higher crosstalk, and long parallel trace segments should be avoided.

Crosstalk also depends on the load, which may vary considerably when driving banks of memory modules, for example. Keep in mind that the total crosstalk on a victim trace is the sum of the crosstalk from each of several nearby aggressors.

Small discontinuities, such as vias and non-uniform return paths on a bus, are also becoming an important factor for the signal integrity and timing of high-speed systems. They produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel-to-channel noise, and may promote mode conversion. In the case of differential pairs, the transformation from differential-mode to common-mode typically occurs on bends and non-symmetrical routing, near via and pin obstructions, but can also be caused by small changes in impedance due to return path issues.

One must also understand the importance of referencing and how to control the return displacement current flow of a signal. Each signal layer should be adjacent to and closely coupled to a reference plane, creating a clear, uninterrupted return path and eliminating broadside crosstalk. As the layer count increases, this concept becomes easier to implement, but decisions regarding returning current paths become more challenging.

The return current of a high-speed, fast-rise time digital signal will always follow the path of least inductance, which is directly beneath the signal path, as in Figure 4. However, discontinuities tend to divert the return current, increasing the loop area, inductance, and delay. The best way to identify the discontinuities is to follow the signal path and imagine the return path closely coupled on the nearest plane. If multiple planes are present in the layer stack, the displacement current will still take the path of least inductance and closely follow the signal trace. If a discontinuity (e.g., split plane) interrupts this return flow, then the return current will be forced into a distant plane where it has a clear run, creating increased loop area and hence more inductance.

A via that connects signal traces referenced to different planes also creates discontinuities. In other words, the return current has to jump between the planes to close the current loop, which in turn increases the inductance of the current loop, affecting the signal integrity. This return current also excites the parallel plate mode of the planes, causing significant EMI. If the reference planes are at the same DC potential, then they can be connected by stitching vias near the signal via transition to provide shorter paths for return currents. However, if the planes are at different DC potentials, then decoupling capacitors must be connected across the planes at these points to create a path. In addition, some of the return current flows through the interplane capacitance to close the loop.

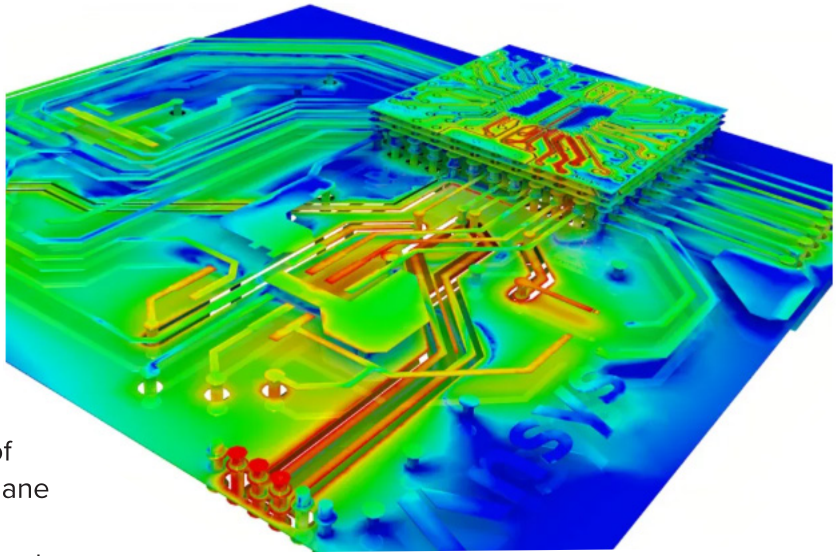


Figure 4: HFSS simulation of return paths. (Source: Ansys)

Unfortunately, discontinuities can never be totally eliminated, but we can take steps to minimize their effects significantly. It is all about inductance! If the return path loop area is increased in any way, then the inductance will also increase. When return currents are disrupted, the energy they shed doesn't disappear; it often couples into the planes themselves.

Plane pairs in multilayer PCBs are essentially unterminated transmission lines, just not the usual traces or cables we may be accustomed to. They also provide a very low impedance path, which means they can present logic devices with a stable reference voltage at high frequencies. But as with signal traces, if the transmission line is mismatched or unterminated, there will be standing waves (ringing). The bigger the mismatch, the larger the standing waves, and the more the impedance will be location-dependent.

When the cavity has open-end boundary conditions, resonances arise when a multiple of half-wavelengths can fit between the ends of the cavity. When the clock or data harmonics overlap with the cavity resonant frequencies, there is the potential for long-range coupling between any signals that run through the cavity, thus affecting signal integrity as a consequence of inadequate power integrity.

High-speed signals behave like RF, turning the PCB into a distributed electromagnetic system. Rise time is the real driver of signal behavior, as every trace becomes a transmission line with its own characteristic impedance and propagation behavior. Variations in impedance, crosstalk, and disrupted return paths distort signals and can excite resonances in the power-ground cavity, making stable impedance, proper termination, and continuous return paths essential for reliable performance. With all these interactions, SI is not a set of isolated problems. It's a system of controlling electromagnetic energy. **I-CONNECT007**

Resources

- **Beyond Design** by Barry Olney: Interconnect Impedance, Controlled Impedance Design, The Fundamental Rules of High-Speed PCB Design Part 2, Reflecting on Reflections, Return Path Optimization.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.

BY TRACY RIGGAN, GLOBAL ELECTRONICS ASSOCIATION

A Necessary Shift From Gerber to IPC-2581

IPC-2581 is an open, vendor-neutral data exchange standard developed by the Global Electronics Association to streamline the exchange of PCB design information across fabrication, assembly, and test. It replaces multiple legacy formats—including industry standards, Gerber, and ODB++—with a single, comprehensive, XML-based dataset that captures all manufacturing details.

By enabling a unified digital product model, IPC-2581 has been shown to reduce errors, eliminate ambiguity, and improve efficiency across the electronics manufacturing process. It is a key enabler of modern, data-driven, and Industry 4.0 manufacturing workflows. As OEMs, such as Cisco Systems and Amazon, push this forward, the IPC-2581 Consortium, led by Hemant Shah, chair, is working to educate a reluctant industry to help them help themselves by adopting the IPC-2581 data format. IPC-2581 was created by merging two previous formats: ODB++ and IPC's GENCAM (back in 2004). It has been used to fabricate, assemble, and test boards since Jan 1, 2016.

In this interview, Hemant and consortium colleague Terry Hoffman, technical leader in product operations at Cisco Systems, explain how IPC-2581 is an unavoidable solution for superior data integration and communication as manufacturing moves forward.

Hemant Shah and Terry Hoffman

Hemant, you led a full-day summit on the adoption of IPC-2581 at APEX EXPO this year, focused on getting more companies to adopt this standard. What topics were covered during the summit, and what do you hope attendees gained from participating?

Hemant Shah: We hold these summits to bring together companies from the design and manufacturing sides to learn from each other and understand their challenges in adopting the standard. In some cases, as Terry presented, they've successfully replaced Gerber with 2581 on their designs. What did they learn and how did they go through the process of adopting it?

Many companies have been using IPC-2581 since 2016. This was a follow-up to the October summit and was intended to provide them with an update and several other presentations, including one from Cisco talking about its migration from Gerber. Another was from Aegis discussing how their contract manufacturing customers use 2581. Dana Korf of Victory Giant spoke about why manufacturers should use 2581, showing that much of the data passed to manufacturing is defective and needs correction. A presenter from Amazon spoke about how the company is using 2581 for stackup exchange and what challenges they're facing getting it to fabrication.

Two very interesting things came out of the discussions. First, a request to validate the output of their tools that produce data files to 2581, to confirm whether the files produced by their tools are correct against the schema. That was a hot topic.

Next, to our surprise, was that many companies are interested in using AI with the 2581 data to develop their own tools to get work done faster.

Terry Hoffman: IPC-2581 is inherently AI-enabled, so it's a very good format for doing that.

Shah: It's everything in one file, so you don't have to train the AI to understand multiple files, missing data, and so on. You just feed it the 2581 file, and AI can do the check.

What are the next steps to ensure this becomes the global standard for data transfer?

Shah: One recurring theme from the summit was how companies are requesting educational materials they can pass to suppliers or their design houses, so the design houses can send them to their manufacturers to learn about 2581, and vice versa. We need a best practice for spreading the message about the benefits of IPC-2581 and broadening our reach, with the help of the Global Electronics Association.

Hoffman: The enhancements that we make in the standard as we progress are important. Version 4 has several enhancements that we've requested over the past couple of years. We need to let people know what it supports today vs. what it supported even just last year, and make sure they know they can ask for changes to be included as we continue to update the standard.

Are there any major hurdles to adoption that you're still facing?

Hoffman: The industry has been using Gerber data for decades, and people don't like to change. The PCB industry is just as bad as the power industry. They just don't want to spend the money to change. I'm trying to break that down.

Some OEMs are asking whether 2581 is supported, and they're being told no, so they just give up. But Cisco, on the other hand, found that it would protect their IP. Now we're telling our vendors that we'll be sending you 2581 data, and it's good data. It has everything the vendors need to build and assemble boards.

Shah: Changing over from Gerber to 2581 is a process, not a light switch. When Terry said he told his suppliers, they worked together to develop a process and made sure the transition would go smoothly before they actually switched formats.

Hoffman: Yes, and we did extensive testing ahead of time to ensure the data was being exported properly. There are ways to compare the Gerber to the IPC-2581 data output and demonstrate that the data is good. If it wasn't, we'd go back to our CAD vendor and have them update their software. It's important to make sure that everybody is good with it. You have to prove it to them.

Shah: But the key to migrating is for a design house to make the decision that they want to modernize how they communicate with their manufacturing partners for their own benefit, as well as for the manufacturing companies to realize that 2581 saves them time, improves their efficiency, and gives them data to work on to improve that process in the future. Then they must educate their customers and say, "If you give me 2581, it's better for you and for me. It works for both sides." Both sides win by using 2581.

Do you have any closing comments about IPC-2581 or, specifically, the work of the consortium? How can industry members support this effort?

Shah: Yes, we're an open consortium, and there's no fee to join. Participate as little or as much as you want, but as a consortium member, the more you participate, the more you can influence the direction of the standard and the decision-making.

Hoffman: You can also attend just to ask questions about problems you're having.

Shah: There are two email addresses they should remember. TC@ipc2581.com is for technical questions about the format, the schema, the usage, and info@ipc2581.com is for all other questions regarding adoption.

Those email addresses go to multiple people, so you not only get somebody to respond quickly, but you also get multiple perspectives if there are multiple perspectives to the answer.

Hoffman: That's the nice thing about having multiple people. There are different opinions for different things. Hopefully, we can all come to the same conclusion eventually. Sometimes we differ, but that's the way things happen, so it's all good.

Thank you so much for your contributions to this effort and for joining the Technology Conference.

Hoffman: Thank you.

Shah: Thank you for having us. **I-CONNECT007**

Tracy Riggan is senior director, Community Technology Solutions, Global Electronics Association.

Reliability by Design

Aligning Intent With Fabrication Reality

LISTEN NOW!

At APEX EXPO, Kelly Dack caught up with Paul Cooke, director of engineering at Summit Interconnect, following Paul's well-attended presentation on design for reliability. Paul shared practical insights on how reliability expectations shift across industries, from commercial applications to high-stakes aerospace and defense. He discusses the critical role of communication between designers and fabricators, the importance of understanding evolving materials and processes, and the challenges posed by legacy designs and incomplete documentation.

The Modern Masters of Signal Integrity *and AI-driven Design*

BY KELLY DACK, CIT CID+, PIONEER CIRCUITS, INC.

Signal integrity (SI) in PCB design has moved from a niche engineering concern to the defining factor in whether modern electronics succeed or fail. As data rates push beyond PAM4 (4-level 112G) gigabit territory and SerDes components exhibit edge speeds as fast as 50–100 picoseconds, PCBs behave less like collections of simple traces and more like complex electromagnetic systems.

At these speeds, a trace is no longer just a connection between two points, but a transmission structure governed by field behavior, discontinuities, and propagation delay. Even small imperfections in routing, stackup design, or return path management can lead to timing errors, signal distortion, electromagnetic interference, and, ultimately, system failure.

The Founders of Signal Integrity

I've compiled a list of contributors to the signal integrity evolution (see sidebar). It isn't meant to be comprehensive; it reflects my personal recollec-

The Masters of Signal Integrity

These individuals helped define SI before it was widely formalized.

Early Foundations (1980s–mid-1990s)

Both Morrison's grounding in electromagnetic principles and Johnson's early work translating high-speed behavior into practical PCB design rules laid the intellectual foundation for SI as a discipline.

Ralph Morrison

Ralph Morrison established many foundational principles that underpin modern PCB design. His work on grounding, shielding, and current flow emphasized that electrical behavior is fundamentally about loops and fields rather than isolated conductors. Morrison's teachings clarified that ground is not a physical destination but a reference system, and that shielding effectiveness is entirely dependent on how currents are controlled and returned. These ideas are now so embedded in engineering practice that they are often repeated as rules of thumb without attribution to their origin. He died in 2019.

Howard Johnson

One of the earliest and most influential figures in this transformation was Howard Johnson. When many engineers still viewed digital signals as idealized voltage transitions moving through perfect wires, Johnson reframed the entire mental model. He insisted that high-speed digital signals must be understood as electromagnetic waves traveling through a transmission medium. His work, most notably High-Speed Digital Design: A Handbook of Black Magic, helped engineers recognize that reflections, impedance discontinuities, and propagation delays are not secondary effects but fundamental design constraints.

Formalization and Expansion (mid-1990s–2000s)

This group brought SI into mainstream engineering practice through books, seminars, and early EDA alignment. This era marks the explosion of SI education: Design rules became teachable, measurable, and repeatable.

Lee Ritchey

While foundational thinkers established the physics, engineers like Lee Ritchey brought structure and repeatability to real-world design. Ritchey's philosophy, developed through decades of consulting and training at the Speeding Edge, is grounded in the belief that system success is determined early in the design process. In his view, stackup planning and architectural decisions made at the beginning of a project dictate signal integrity outcomes more than any later routing optimization. His "right-the-first-time" approach has influenced countless high-speed designs by emphasizing prevention rather than correction.

Doug Brooks

Doug Brooks has contributed extensively to education in PCB design and electromagnetic compatibility. Through decades of teaching and writing, he has helped engineers understand the behavior of currents in practical PCB structures. His work consistently emphasizes clarity and accessibility, translating complex electromagnetic interactions into actionable design guidance that engineers can apply immediately.

Eric Bogatin

Building on this shift in thinking, Eric Bogatin expanded the discipline into a measurement-driven science. Through his work in industry and academia, including Bell Labs, Sun Microsystems, and the University of Colorado Boulder, Bogatin emphasizes that intuition alone is insufficient without validation. His philosophy centers on the idea that engineers do not design signals themselves, but rather design for the behavior of energy in a system. His teaching style, which blends theory with experimental validation, has become a cornerstone of modern signal integrity education.

Industry Scaling and Power Integrity Era (2000s–early 2010s)

The focus expanded from signals alone to full-system behavior, including power distribution.

Istvan Novak

Istvan Novak has played a central role in defining modern power integrity as a foundational discipline that directly impacts signal integrity. His work demonstrates that without a stable and well-designed power distribution network, even the most carefully routed signals will fail to perform reliably. His contributions have helped formal-

tion of experts I've read about or had the pleasure of meeting. I've loosely organized them by decade, though there is significant overlap. It is not a tidy relay race where one group hands the baton to the next.

These engineers worked concurrently, challenging, debating, and refining one another's ideas, collectively pushing the industry (sometimes reluctantly) toward a deeper respect for physics. I struggled to organize their contributions chronologically, and that difficulty itself may mirror how AI is now learning from them faster, and perhaps with greater precision, distilling decades of human trial, error, and hard-earned intuition into algorithms.

Signal integrity did not evolve in isolation. It was built gradually over decades, drawing on insights from a diverse group of engineers who transformed abstract electromagnetic theory into a practical design discipline. They translated physics into intuition, and then into repeatable engineering practice. Today, as AI absorbs the accumulated knowledge of the field, SI is transitioning from something engineers learn through experience into something that can be partially encoded, simulated, and scaled.

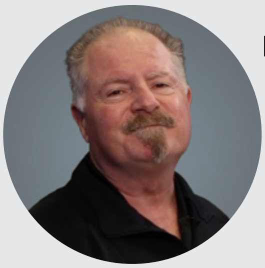
Why Signal Integrity Became the Center of Modern Design

PCB design engineers have learned that, at high speeds, digital design is no longer dominated solely by logic behavior. Rather, it is by energy traveling through a physical medium. Every transition on a line is subject to reflection if impedance is not controlled. Every return current must find a path, and if that path is disrupted, it creates loop area expansion and radiated emissions. Even a via is no longer electrically transparent; it introduces frequency-dependent impedance changes that must be accounted for.

These effects are no longer "edge" cases. Engineers are realizing that they define system behavior. As a result, modern PCB failures frequently manifest not as functional design errors but as subtle physical-layer issues, such as bit errors, electromagnetic compatibility violations, degraded timing margins, or unexpected coupling between adjacent structures. In many cases, these ize decoupling strategies, PDN design methodologies, and noise analysis techniques that are now standard practice in high-speed systems.

Larry Smith

Larry Smith contributes to this ecosystem through modeling and simulation methodologies that allow engineers to predict behavior before fabrication. By applying SPICE-based analysis, IBIS models, and transmission line theory, he helps engineers understand how interconnect structures will behave under real operating conditions. His work enables a shift from reactive debugging to predictive design validation.



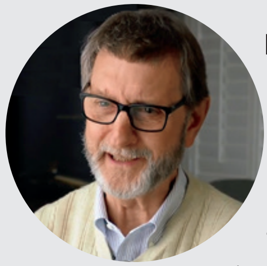
Mike Resso

Mike Resso similarly bridges the gap between theoretical models and physical behavior through advanced measurement techniques. His work with S-parameters, de-embedding, and time-domain analysis allows engineers to extract meaningful insight from complex interconnect systems. By connecting RF measurement rigor with digital design challenges, he ensures that theoretical models remain grounded in physical reality.

These experts pushed SI into the realm of power integrity, measurement, and compliance, especially as data rates and edge speeds accelerated.

Modern High-Speed and Application-Focused Era (2010s–present)

These voices dominate current conferences, real-world design training, and emerging applications. They emphasize practical implementation, layout discipline, EMI control, and translating SI theory into designs that pass the first time, especially in today's dense, high-speed systems.



Rick Hartley

Rick Hartley has contributed another critical layer of understanding by focusing on the relationship between signal integrity and electromagnetic compatibility. His teaching consistently reinforces that signal quality is not defined solely by the trace itself, but by the integrity of the return path. By translating electromagnetic theory into practical layout guidance, Hartley helped engineers understand that current does not simply travel forward, it completes a loop, and that loop defines the system's electromagnetic behavior.

Daniel Beeker

Daniel Beeker adds a more visual and intuitive dimension to this understanding by demonstrating that signal integrity is fundamentally about electromagnetic space. Through live demonstrations, he reinforces that signals do not exist solely in copper traces, but in the fields surrounding them. His perspective helps engineers move beyond schematic thinking into spatial electromagnetic awareness.

Ken Wyatt

Ken Wyatt is a highly respected independent consultant, instructor, and author in the field of electromagnetic compatibility (EMC) and electromagnetic interference (EMI). Often referred to as "The EMC Doctor," he is known for helping engineers diagnose and fix noise problems early in the design process. His work emphasizes hands-on troubleshooting, practical pre-compliance testing, and effective PCB design practices to prevent issues before they reach the lab.

Karen Burnham

As signal integrity matured, validation became as important as design. Karen Burnham represents this shift toward measurement-first engineering. Her work emphasizes that simulation alone cannot guarantee performance, and that confidence in a design must ultimately be earned through measurement and validation. In her view, verification is not a final step but an integral part of the design process itself.

Stepping back, the pattern seems clear:

- **Morrison and Johnson** taught us why signals misbehave
- **Ritchey, Brooks, and Bogatin** taught us how to design around it
- **Novak, Smith, and Resso** taught us you can't ignore power anymore
- **Hartley, Beeker, Wyatt, and Burnham** are showing us how to actually get it right in today's designs

problems are discovered late in the design cycle, making them expensive and time-consuming to resolve. This reality forced our industry to rely heavily on a group of engineers who could explain not just what was happening, but why it was happening at the physics level.

The Emergence of AI-driven SI

AI-SI is not a replacement for engineers, but a compressed, scalable extension of their expertise. It unifies signal integrity, power integrity, EMC, and manufacturability into a single system that delivers real-time design feedback.

Instead of analyzing these domains in isolation, AI-SI evaluates them together, flagging impedance issues, return path disruptions, and stackup risks during design, not after. It also links layout decisions directly to manufacturing outcomes, closing the long-standing gap between design intent and physical reality.

Its evolution is straightforward: assistant, co-designer, optimization engine, and ultimately a digital twin capable of predicting failures before a board is ever built.

Conclusion

Across generations, engineers have clarified how currents truly behave, validated theory through measurement, and translated complex electromagnetics into practical design rules. They also elevated power integrity into a core discipline, forming the foundation for modern high-speed systems.

Now, AI is entering signal integrity, scaling decades of accumulated knowledge into faster analysis and design iteration. But AI didn't invent this body of work. Every model, rule, and insight traces back to engineers who discovered, tested, and refined these principles in the real world. We can automate the knowledge, but not the gratitude. **I-CONNECT007**

Kelly Dack, CIT CID+, specializes in DFx-driven PCB design and applications engineering at Pioneer Circuits, Inc. To read past columns, click here.

BY KRISTIN MOYER, GLOBAL ELECTRONICS ASSOCIATION

Common vs. Differential Mode in Routing and Signal Integrity

In high-speed designs, the distinction between common-mode and differential-mode is becoming increasingly critical in PCB routing. While most designers are familiar with differential routing as a technique for certain signals on the PCB, many may not realize its underlying purpose. Differential routing is used to mitigate differential mode noise in the system. To understand this, we need a bit of electrical engineering background on signal and current flow in a system.

The current that flows from the source (driver) down the positive trace to the load (receiver) flows in a loop, and within that loop, the current is constant. This current must return (RTN) from the load (receiver) back to the source (driver). Because the current flows in one direction from the driver to the receiver and then in the opposite direction from the receiver back to the driver, these two currents are thought to be equal in magnitude and opposite in polarity. This means any noise from the sources is moving in different directions, creating differential noise.

Common-mode noise, on the other hand, occurs when noise (current) from an external source, such as EMI, appears on both the signal line and the return line traveling in the same (common) direction.

Because an external source affects different signals by slightly different amounts, common-mode noise usually manifests as an unwanted voltage in the signal, since the voltage seen at any node with respect to a different node is simply the difference between the two voltages.

For example, if the voltage on node A (V_A) is 15 Vdc and the voltage on node B (V_B) is 10 Vdc, and you are measuring V_A with respect to V_B, then the difference (V_{AB}) is $V_A - V_B$, or 15 Vdc – 10 Vdc for a result of V_{AB} = 5 Vdc. Since common-mode noise is usually generated by external sources, the primary method to mitigate it is shielding, and for wires in a cable, twisted pairs can be helpful.

For differential-mode noise, differential can help mitigate it. Three common routing techniques used in PCB design:

- Single-ended mode is the most common style. It uses a single wire or trace from the driver to the receiver. The signal propagates from the driver to the receiver on this conductor and returns to the driver using the GND/RTN system of the design.
- Differential-mode, more properly called odd-mode, is the next most common style. This uses a pair of wires or traces from the driver to the receiver. One trace carries the positive signal and the other carries the negative signal. The negative is equal in magnitude and opposite polarity to the positive signal. Since signals are equal and opposite, no current flows in the GND/RTN system, creating an ideal case.
- Common-mode is more properly called even-mode, and is the least used style. It still uses two wires/traces, but current flows in the same direction on both conductors. This is typically created by unwanted noise or other variations caused by unintended or unexpected conditions.

When considering differential routing as a noise-reduction solution, there are pros and cons to consider. One major con is that differential routing requires two traces, in addition to the RTN, to route the signal from point A to point B. This means the board area required for differential routing is twice that for single-ended routing.

The pros significantly outweigh the cons:

- In low-voltage/signal-level designs, you effectively get double the signal level. If you have the same voltage (V), one positive (V+), and one negative (V-), then the difference between them is (V+) – (V-) = 2V since V- = -V+. This, in turn, effectively doubles the signal voltage, giving you better immunity to low-voltage noise.
- There is no RTN current (in an ideal system). Since differential signals are by definition equal and opposite, there is no return current through any path other than the two signals of the pair.
- Differential receivers are typically designed to be sensitive to the differential mode but are designed to ignore the common mode.
- Switching timing is usually more precise. This is because the signals are referenced to each other, and the crossover point is tightly controlled. On the other hand, single-ended signals reference some other signal in the design (CLK, EN, etc.) and therefore their crossover/transition points are subject to noise, threshold level shifts, threshold detection, etc.

Since devices and ICs can convert single-ended signals to differential signals, using differential routing instead of traditional single-ended routing is an excellent way to mitigate noise in our system. This is especially true if you need to route your traces a long distance on your PCB. With common-mode noise, converting the two signals to differential to route over any significant distance, then converting back to single-ended at the destination, may help mitigate that noise as well.

Kristin Moyer is an instructor at Sacramento State University and for the Global Electronics Association.

CONTROLLED IMPEDANCE

When 'Connecting the Dots' Stops Working

BY JOHN WATSON, PALOMAR COLLEGE

All designers should be familiar with the 1993 engineering masterpiece, "High-Speed Digital Design: A Handbook of Black Magic", by Howard Johnson and Martin Graham. So, is the discussion on high-speed or signal integrity really talking about black magic? Yes, and at the same time, absolutely not.

I agree that Johnson and Graham nailed the experience every first-time designer goes through: You follow the rules, the schematic looks clean, layout passes checks, and then the signal misbehaves. It reflects, rings, and does things that seem completely disconnected from the lines you just drew. That disconnect is what creates the "black magic" feeling.

But nothing mystical is happening. Signal integrity follows physics that are consistent, predictable, and fully explainable. But those rules don't show up in the schematic. Instead, they live in the electromagnetic fields around the traces, in the stackup, and in the relationship between conductors and their return paths. The authors weren't claiming black magic; they were calling out how it feels until you learn what's going on. The fact that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they said it more than 30 years ago only reinforces how fundamental and enduring these concepts really are.

If it sometimes feels like black magic, we should be asking: How do we make the invisible visible? How do we take something that behaves in fields we can't see and turn it into something intuitive, something we can design with confidence instead of guesswork? Because once you can see it, even conceptually, the mystery disappears, the reflections make sense, the behavior becomes predictable, and what once felt like magic becomes something you can control.

Just the term "controlled impedance" sends shivers down a designer's spine, the kind where a perfectly clean layout suddenly feels haunted. Nothing's broken, but everything's reacting, and for a moment, you understand exactly why it was called "black magic."

Why do so many designers struggle with controlled impedance? It's not because the math is difficult; it's because the concept is counterintuitive. You see, we're taught to think of traces as simple connections. Early on in my career, I was told routing was "connecting the dots," and that worked right up until my first high-speed design, when reality said otherwise. The problem now lies in physics at higher speeds, where traces stop being simple paths and become part of the system itself. You can see a connection, but you can't see the impedance that lives in the relationship between the trace, the plane, and the surrounding material. That ma it harder to grasp.

Additionally, most designers encounter it only when something goes wrong, so it feels like a fix rather than a foundation. The real shift in the quality of my designs came when I stopped thinking of a signal as just voltage and started seeing it as energy moving through a controlled environment. Once that clicks, controlled impedance starts to make sense.

Imagine driving down a highway at a steady speed, with a smooth road, consistent lanes, and everything is predictable. You don't even have to think about moving. Suddenly, the lane narrows, then widens, and the pavement shifts from smooth asphalt to gravel and back again. You're still moving forward, but now you're reacting—slowing down, adjusting, and hesitating.

A properly designed PCB trace is like that smooth highway, providing a consistent environment so the signal moves cleanly from one point to another. But when impedance changes, whether from variations in trace width, distance to the reference plane, or inconsistencies in the surrounding environment, it's like the changing road conditions. The signal doesn't just continue unaffected; it reacts. Part of it keeps moving forward, but part of it reflects, as if the signal momentarily hits the brakes and questions what just changed. Those reflections then interfere with the original signal, distorting its shape and timing. The more inconsistent the path, the more the signal is forced to respond rather than travel. Bottom line: The smoother and more consistent the path, the less you notice it because everything works.

The $64,000 question: How do we make the PCB "road" smoother and more consistent?

You do it by following a few fundamental principles and removing surprises from the signal's path. It's that simple. In PCB terms, that starts with consistency, keeping the trace width uniform, maintaining a solid, continuous reference plane beneath the route, and preserving a constant spacing between the trace and that plane. Each element defines the environment the signal experiences. The moment one of them changes even slightly, the signal notices and hits the brakes hard.

Think about what happens when you neck a trace down to get around a component, let it wander over a split plane, or change layers without providing a clean return path. From a layout perspective, those might feel like small, practical decisions. From the signal's perspective, they are abrupt changes in its environment, and when the environment changes, the signal reacts. Part of it continues forward, and part of it reflects. That's physics doing exactly what it's supposed to do.

Furthermore, the stackup matters because it's not just a manufacturing detail; it's the foundation of your electrical design, the controlled environment for the energy to live. The dielectric thickness, material properties, and copper geometry all contribute to defining the impedance. If you treat the stackup as an afterthought, you're essentially designing a road without knowing its width, surface, or even its makeup. But when you define it intentionally, you're setting the rules of the environment before a single trace is routed.

Most assume this is about perfection. It's not. The goal is predictability. You don't need every trace to be identical, but you do need every critical signal to see a consistent environment along its path. That means minimizing unnecessary width changes, avoiding breaks in the reference plane, controlling layer transitions, and being deliberate about how signals move from one part of the board to another.

When you do that, something interesting happens: The signal stops reacting, reflecting, distorting, and fighting the path you've created. It simply moves and flows.

That's really the point of controlled impedance design: not to perform engineering "black magic," but to create a path so consistent that the signal has no reason to do anything unexpected.

I-CONNECT007

John Watson is a professor at Palomar College, San Marcos, California. To read past columns, click here.

Below the Surface

Looking Ahead to Where Integration Actually Happens

BY CHANDRA GUPTA, REMTEC

Progress in RF rarely arrives and suddenly rewrites the rules. What actually moves performance forward almost always happens in the seams, the interfaces, the choices that determine whether individual parts are allowed to work together, or forced to fight one another.

So, when we look ahead in RF systems—from DC through millimeter-wave—the most important conversations aren't about isolated materials or heroic devices. They're about integration, and more specifically, about how ceramic-based RF packages and module architectures shape system-level behavior long before the signal ever reaches free space.

At high frequencies, the package ceases to be a container. It is a participant.

The Shift From Components to Ecosystems

For much of electronics history, it made sense to think in terms of discrete building blocks. A component had a defined function where a package protected it, and a board connected it. Performance was largely a matter of selecting the right parts and assembling them correctly.

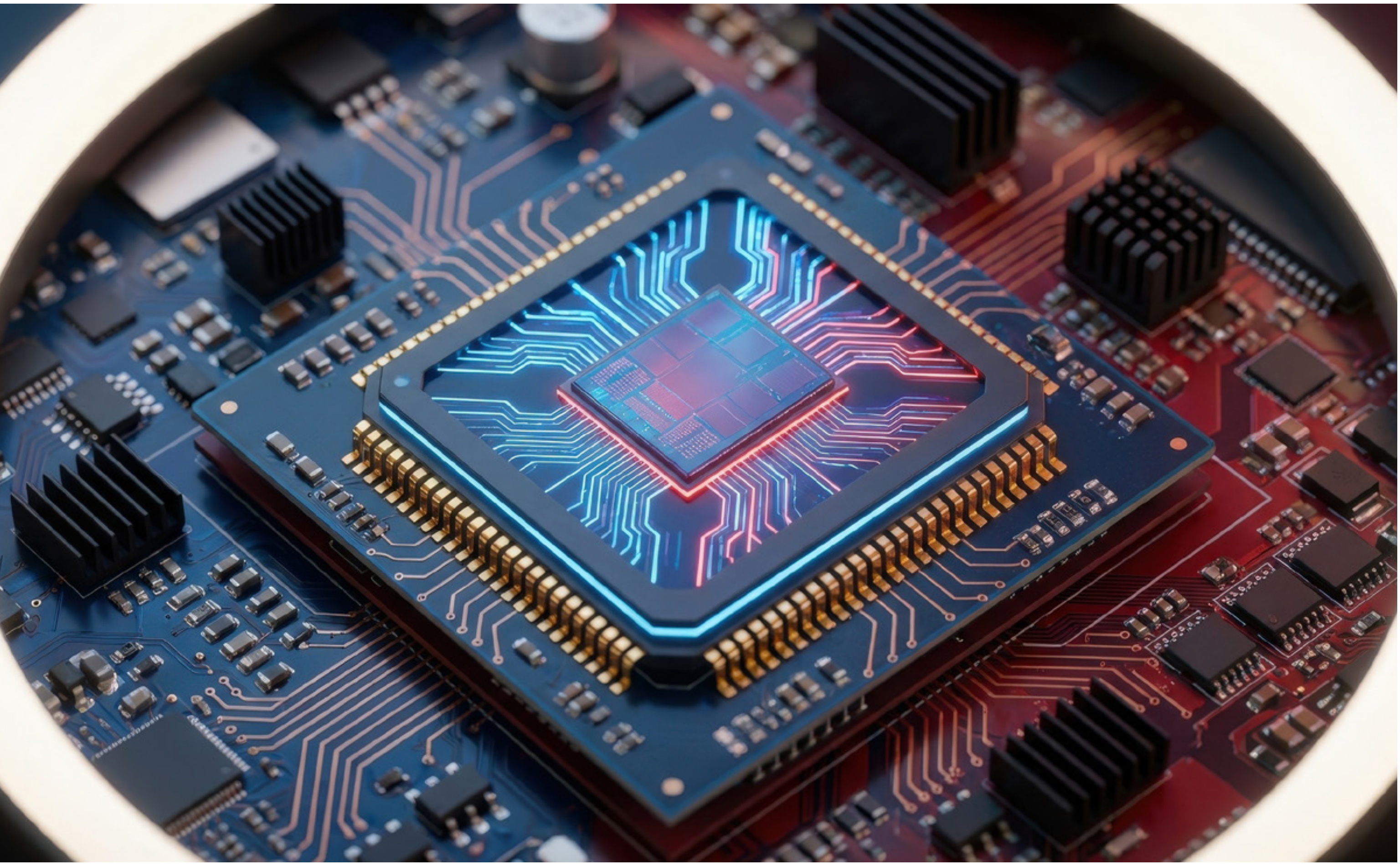
That mental model breaks down as frequency increases. At RF and microwave frequencies, especially as we push into millimeter-wave, the boundaries between components, packages, and systems begin to dissolve. Parasitics stop being second-order effects. Thermal paths become signal integrity decisions. Mechanical tolerances turn into electrical variables.

In this environment, performance is emergent. It arises from interactions, not specifications.

Ceramic-based RF packages sit where materials science, electromagnetic behavior, thermal management, and manufacturability converge. The architectural decisions made here ripple outward, sometimes amplifying system performance, sometimes quietly limiting it.

Click here to read the full column

What Designers Should Know About Non-conductive Via Fill



BY MATT STEVENSON, ASC SUNSTONE CIRCUITS

The rapid advance of technology is driving changes in electronics that require increasingly smaller boards capable of handling higher signal speeds and supporting more robust software applications.

Manufacturers are increasingly called upon to produce ultra high density interconnect (UHDI) PCBs, so it's important to tune our production capabilities and customer service models to this trend. Non-conductive via fill (NCVF) offers a cost-effective, reliable manufacturing method that accommodates the densely packed, fine-pitch ball grid array (BGA) components present in UHDI designs.

Not all PCB manufacturers approach NCVF in the same manner. Designers who thoroughly understand the process will have more confidence that their designs will be manufactured to meet requirements.

Benefits of Non-conductive Via Fill

Primarily used to prevent solder wicking into vias, NCVF is the process of filling drilled holes with a specialized, non-conductive, low-shrinkage epoxy. Boards can have a higher component density because manufacturers use a technique called via-in-pad, plated over (VIPPO). This involves placing a via used to conduct signals between layers into the same real estate as a surface mount pad. VIPPO eliminates the need to route a trace from the component lead to a via nearby, provides a nice flat pad for assembly, and prevents solder from wicking through the via and weakening the solder joint.

The epoxy inside the holes makes the vias more reliable by limiting expansion during heat exposure. It enhances mechanical strength, prevents solder wicking into vias, and enables via-in-pad technology. By filling voids with epoxy, vias are sealed and protected from contaminants. NCVF creates superior structural integrity against stress fractures compared to conductive fills and offers a better coefficient of thermal expansion (CTE) match with the surrounding laminate.

Submitting a Quote: Manufacturer Capability and Process

What do designers need to know? First, can the manufacturer accommodate your needs if you call out NCVF for a design with smaller pitch components? Manufacturers often publish specs that inform designers of their capabilities, making it easier to assess them before submitting a quote.

If a manufacturer does not make it clear, contact them directly to confirm they have experience with NCVF. Manufacturers unable to meet design requirements in-house may still provide a quote, either to engineer NCVF capability on the fly or to farm out production to a subcontractor.

Breaking down the NCVF process

If you've had a chance to read my columns or my book about designing for the reality of PCB manufacturing, you know I think it's important for designers to have a good working knowledge of each stage of the manufacturing process. This knowledge can be quite useful both during design and when it is time to create a quote request for your manufacturer.

Following is a high-level breakdown of the NCVF process:

1. Drill the holes that require via filling.
2. Clean the holes to remove any debris present from the drilling.
3. Plate electroless copper across the entire panel and inside the holes to provide connectivity within the holes for electroplating.
4. Electroplate ~0.5 mils of copper across the panel and into the holes.
5. Laminate photoresist and image for button plating. This exposes just the holes and a little more of a pad on the surface.
6. Button plate. Plate another ~0.5 mils of copper into the holes. Remove the resist.
7. Planarize the buttons off the surface of the panels.
8. Using vacuum filling or screen printing, force non-conductive epoxy into the via holes.
9. Thermal cure the epoxy.
10. Sand the surface of the panels to remove any via fill epoxy and copper buttons on the surface. This surface planarization restores a flat copper surface.
11. Parts from here are returned to drill to have the rest of the holes drilled and panels follow standard manufacturing process.

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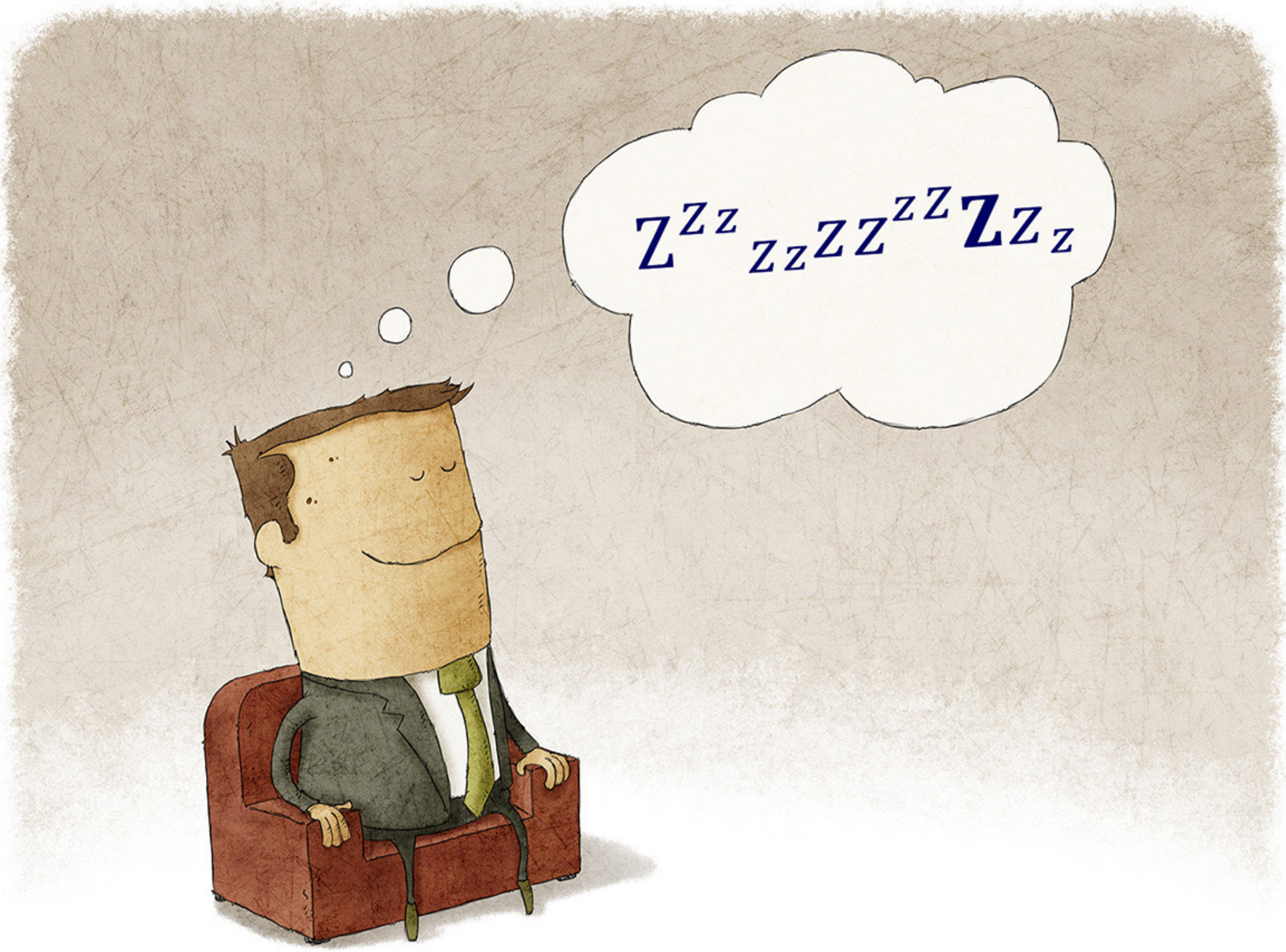

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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This can create challenges with lead times and yield, and potentially jeopardize production of the boards. Designers should clearly define the non-conductive via filling requirement in the Gerber files and confirm the manufacturer has the proven ability to build the PCB to specs.

More information is always better when submitting quotes. We encourage designers to include as many specifics as possible in their quote requests. This can include specifying non-conductive material used for via filling, identifying the type of surface finish needed to ensure a flat pad for assembly, and defining any other key manufacturing considerations.

Working Closely With Your PCB Manufacturer

When designers call out production specifications in detail, manufacturers do not have to guess what the designer wants. Collaboration also serves to minimize ambiguity about expectations during the quote process and before PCB manufacturing takes place. Open communication helps the designer and manufacturer align priorities based on what is required at any given stage of the lifecycle, from early prototyping to final prototype to full production.

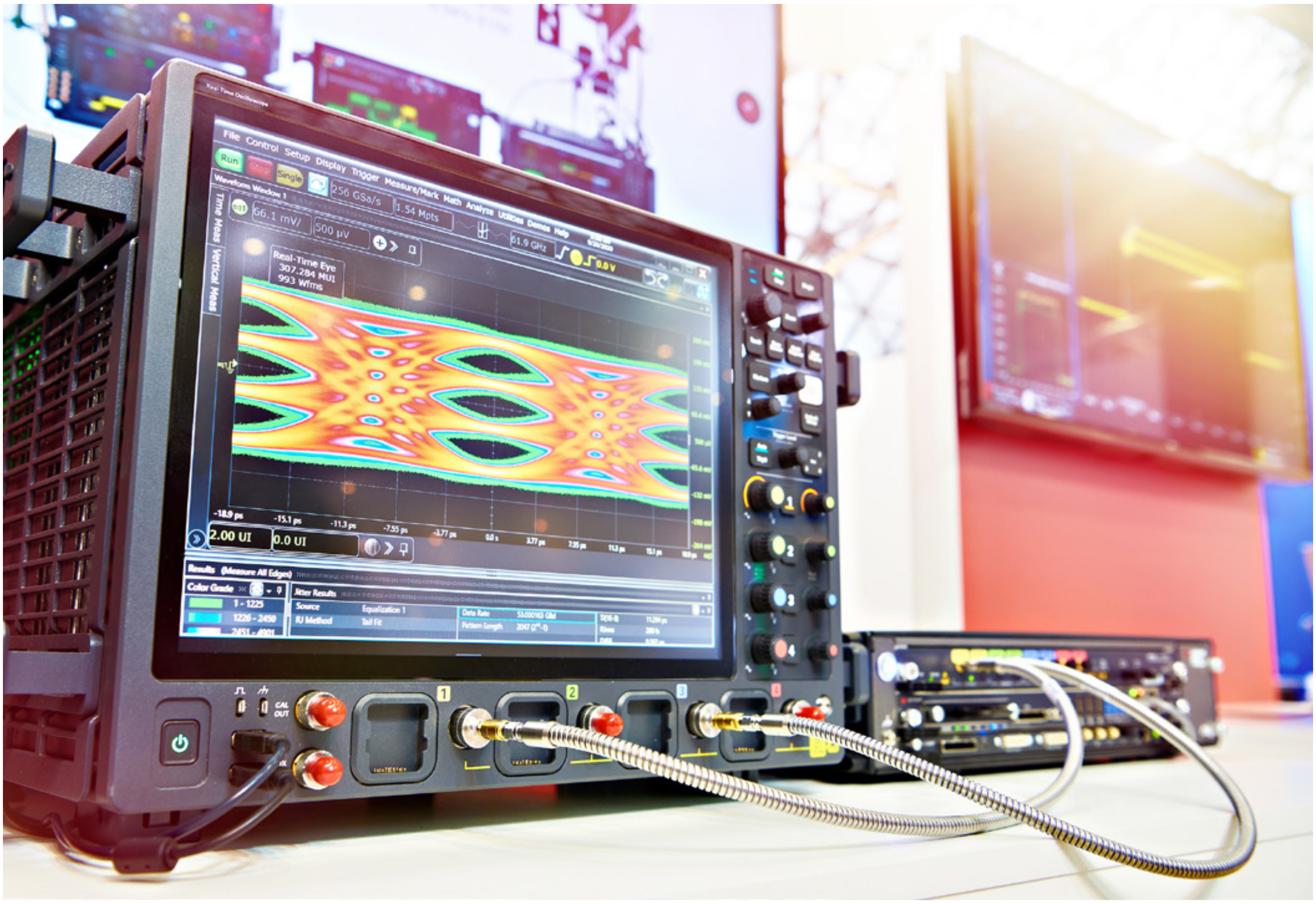
Collaboration also helps the designer understand the experience level and capabilities a manufacturer possesses regarding a capability such as NCVF. Not all manufacturers take the same approach to the process. Don't be afraid to ask to speak to members of the production team. Doing so can help you better understand the manufacturer's approach and align expectations for things like lead time, cost control, and board functionality. Talking to individuals on the production floor, such as engineers or team leaders, will give you more confidence in the manufacturer's ability.

The more designers know about a manufacturing technique like NCVF, the better they can craft quotes that ensure their designs are built to spec.

For a deeper dive into the wide range of surface finish options, listen to the **Designing for Reality: Surface Finish** episode of **On the Line With... .**

Matt Stevenson is vice president and general manager of ASC Sunstone Circuits. Matt is also the author of *The Printed Circuit Designer's Guide to... Designing for Reality* To read past columns, click here.

BY STEPHEN V. CHAVEZ, SIEMENS EDA AND PCEA



Mastering Return Path Discontinuities for Robust Signal Integrity

In the race toward higher bandwidth, tighter form factors, and faster time-to-market, engineering teams focus heavily on device performance, routing density, and advanced materials. Yet one of the most critical determinants of system success remains largely invisible and too often underestimated: the integrity of the return path.

Signal integrity (SI) failures rarely originate solely from the signal trace. More often, they stem from what designers don't see: the disruption of the signal's return path. Return path discontinuities are a leading cause of late-stage failures, unexpected EMI issues, and costly respins. Our challenge is not a lack of awareness, but a lack of visibility, continuity, and enforcement of return path intent across the design lifecycle.

This article reframes return path discontinuities, not as isolated layout mistakes, but as a systemic design risk. I'll also provide practical strategies to eliminate them before they impact performance, compliance, and schedule.

Return Path Reality: Designing the Electromagnetic System

At high speeds, signals do not behave as simple point-to-point connections. They propagate as guided electromagnetic waves. Their behavior is defined not just by the signal conductor, but by the structure formed between the signal and its reference plane.

Signal and return currents are part of the same electromagnetic loop and cannot be separated. The distribution of return current is not arbitrary; it is governed by the electromagnetic fields between the signal and its reference. At high frequencies, these fields concentrate in a way that minimizes loop inductance and stored energy, causing the return current to flow directly beneath the signal trace on a continuous reference plane.

A critical implication follows:

When the reference plane is continuous, fields remain tightly contained, loop inductance is minimized, and signal behavior is predictable

When the reference plane is disrupted by splits, voids, vias, or layer transitions, the fields spread, forcing the return current to redistribute and increasing the loop area

This increase in loop area directly increases loop inductance, which is the primary driver of EMI, voltage noise, and signal integrity degradation.

The relationship between the signal and its return path governs three fundamental aspects of performance:

1. **Impedance stability:** Defined by the geometry of the signal-return structure.
2. **Field containment:** Determines EMI and crosstalk behavior.
3. **Loop inductance:** Drives noise, reflections, and power integrity interactions.

A useful way to think about it is that the signal trace defines intent, but the signal-return loop defines reality. The core principle is that when you control the return path, you control the signal:

- The signal does not define performance; the signal-return loop does
- Discontinuities in the return path create discontinuities in impedance
- Every signal transition is a loop transition, not just a routing event

Designs that preserve return path continuity behave predictably. Those that do not will exhibit instability across SI, PI, and EMI domains.

Return Path Discontinuities: Small Gaps, System-level Consequences

A return path discontinuity occurs when the natural flow of return current is interrupted or forced to redistribute due to a break in the reference structure. While these disruptions may appear minor in layout, their electrical impact is significant.

Return path discontinuities have some common origin points. First is plane splits and voids, where routing across gaps in reference planes forces return current to redistribute around the discontinuity, increasing loop area and inductance. A classic failure mode is high-speed interfaces crossing analog/digital ground splits.

Another origin is in layer transitions without return continuity. When signals change layers without nearby stitching vias, the return path must transition through higher inductance paths, creating localized impedance discontinuities.

In via-induced disruptions, signal vias introduce anti-pads that locally interrupt current flow. In dense via fields, these effects accumulate into measurable discontinuities.

Component-induced blockages, such as large packages, connectors, and mechanical keep-outs, can unintentionally obstruct return current paths, forcing field spreading. Finally, weak plane stitching results in insufficient inter-plane connectivity, increasing inductive impedance between reference regions, and degrading return path continuity.

A Common Failure Scenario

Consider a high-speed SERDES lane routed across a split between digital and analog ground regions. The signal path appears continuous and impedance-controlled, yet the reference plane is not.

The electromagnetic fields can no longer remain tightly coupled to a local return path. Instead, the return current redistributes around the split, significantly increasing loop area and loop inductance. The result is often unexpected EMI radiation, degraded eye margins, and intermittent compliance failures. This occurs despite the signal trace itself appearing "correct."

The System-level Impact: Why Discontinuities Are So Costly

Return path discontinuities trigger cascading effects across multiple domains: Impedance discontinuities lead to reflections, which in turn cause eye closure. Increased loop inductance results in EMI radiation and can ultimately lead to compliance failures. Field spreading contributes to crosstalk, creating a risk of data corruption. Inductive return paths (L·di/dt) generate voltage noise, which can introduce PDN-induced jitter and overall system instability.

These effects are tightly coupled, which is why return path issues are often discovered late, during lab validation, when they are most expensive to fix.

Designing for Continuity: Turning Risk Into Control

Avoiding return path discontinuities requires a shift from reactive debugging to intentional, physics-driven design.

1. **Prioritize Continuous Reference Planes**
   A solid reference plane is the foundation of controlled electromagnetic behavior. Don't ask: Where can I route? Ask: Where can the return current and fields remain contained?

2. **Co-design Signal and Return Paths**
   Every signal transition is a loop transition. Place stitching vias adjacent to signal vias, ensure short, direct return transitions between planes, and maintain symmetry for differential structures.

3. **Avoid Routing Over Discontinuities**
   Try to avoid routing critical signals over plane splits, voids and cutouts, and connector escape regions. If unavoidable, intentionally engineer a return path using stitching vias and adjacent copper.

4. **Optimize Via Structures**
   At high data rates, vias are part of the transmission structure, so minimize unnecessary layer transitions, use back-drilling to remove stubs, and evaluate via fields collectively, not in isolation.

5. **Align Stackup and PDN Strategy**
   A well-designed PDN inherently supports low-inductance return paths. Maintain tight power-ground plane coupling, provide dense stitching between reference regions, and avoid isolated plane islands.

6. **Shift Left with Simulation and Analysis**
   Simulation should guide design decisions, not validate them after the fact. Early identification of return path discontinuities prevents late-stage redesigns, lab debugging cycles, and compliance failures.

Return path discontinuities are not just technical issues. They are indicators of design maturity. Organizations that proactively control return paths achieve faster design convergence, higher first-pass success rates, reduced EMI risk, and more predictable system behavior.

From Layout Issue to Lifecycle Insight: The Digital Thread Advantage

Return path discontinuities are rarely caused by a single mistake. They emerge from disconnected decisions across the design lifecycle, which could look like a plane split defined during stackup planning, a via transition introduced during layout, or a mechanical constraint creating a void in a reference plane. Individually, these decisions may be valid. Collectively, they can disrupt return path continuity.

Connecting Intent to Implementation

A model-based, digital thread approach enables return path requirements to be explicitly defined and enforced by constraint-driven rules for reference plane continuity, signal-class-specific return path requirements, via transition and stitching policies, and stackup-aware coupling definitions. These become active elements of the design process, not passive documentation.

Continuous Verification Across the Flow
Traditional workflows treat SI analysis as a late-stage checkpoint. By then, discontinuities are embedded. A connected design flow enables real-time evaluation of layout decisions, immediate identification of return path disruptions, and cross-domain analysis of SI, PI, and EMI interactions. This shifts SI from validation to design guidance.

Bridging Domains: Electrical, Mechanical, Manufacturing

Many return path issues originate outside electrical design, where mechanical keep-outs create plane voids, connector constraints force routing compromises, and manufacturing limitations affect via structures. A connected workflow makes these interactions visible early, enabling informed trade-offs and preventing unintended discontinuities.

By embedding return path best practices into constraints and reusable methodologies, organizations can:

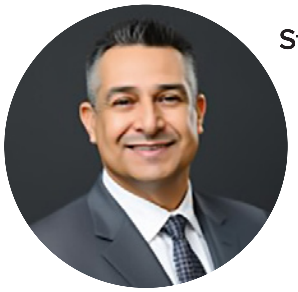
- Standardize high-speed design practices
- Reduce variability across teams
- Accelerate onboarding
- Improve first-pass success rates

This reduces dependence on individual expertise and increases predictability at scale.

Conclusion

In high-speed PCB design, electrical performance is not determined solely by the signal trace, but by the continuity, geometry, and integrity of its return path. The most advanced routing strategies, materials, and components cannot compensate for a broken return path or for a design process that allows those breaks to occur.

By grounding design decisions in electromagnetic principles and reinforcing them through a connected, constraint-driven workflow, engineering teams can move from reactive problem-solving to predictable, scalable design excellence. Because in the end, successful systems are not defined by the paths you route, but by how well you preserve the paths you don't see. **I-CONNECT007**



Stephen V. Chavez is principal technical product marketing manager at Siemens EDA and chair of PCEA.

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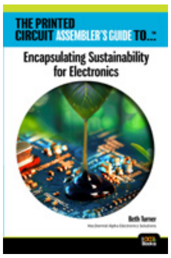

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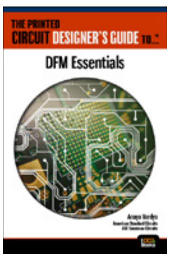

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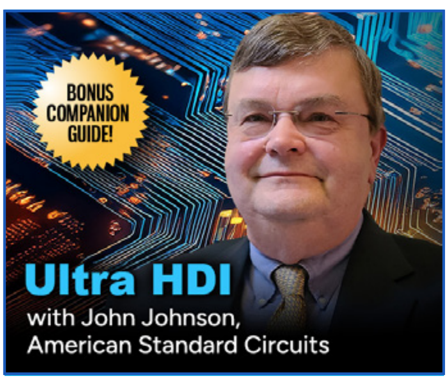

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ADVERTISER INDEX

The Modern Masters of Signal Integrity *and AI-driven Design*

BY KELLY DACK, CIT CID+, PIONEER CIRCUITS, INC.

Signal integrity (SI) in PCB design has moved from a niche engineering concern to the defining factor in whether modern electronics succeed or fail. As data rates push beyond PAM4 (4-level 112G) gigabit territory and SerDes components exhibit edge speeds as fast as 50–100 picoseconds, PCBs behave less like collections of simple traces and more like complex electromagnetic systems.

At these speeds, a trace is no longer just a connection between two points, but a transmission structure governed by field behavior, discontinuities, and propagation delay. Even small imperfections in routing, stackup design, or return path management can lead to timing errors, signal distortion, electromagnetic interference, and, ultimately, system failure.

The Founders of Signal Integrity

I've compiled a list of contributors to the signal integrity evolution (see sidebar). It isn't meant to be comprehensive; it reflects my personal recollec-