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February 2013

the pcb magazine

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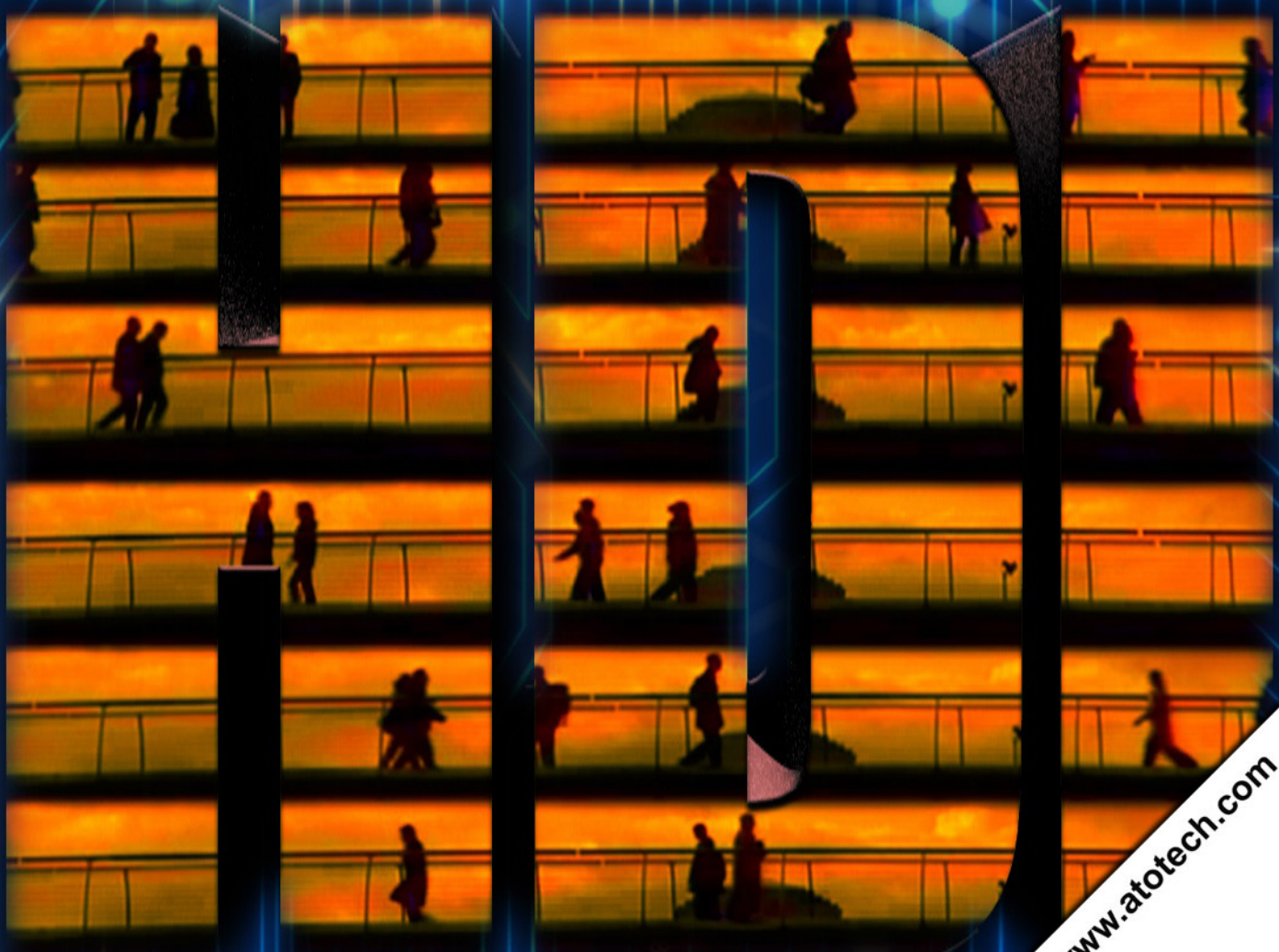

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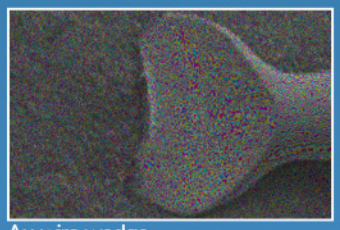
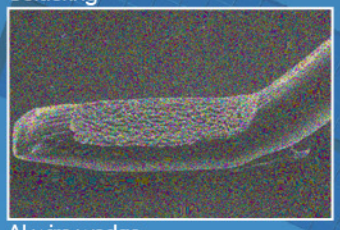
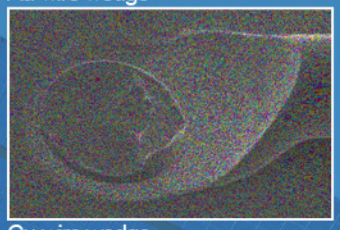
Soldering


Au-wire wedge


Al-wire wedge


Cu-wire wedge

Process Flow

- Cleaner Pro Select UC
- Micro Etch MicroEtch C
- Dip Aurodip (Option)
- Pre Dip
- Activator Aurotech Activator 1000
- Fine Line Post Dip Aurotech FL Plus Post Dip (Option)
- Electroless Ni Aurotech CNN mod.
- Electroless Pd PD-Tech
- Immersion Au Aurotech SF Plus

Pure Pd

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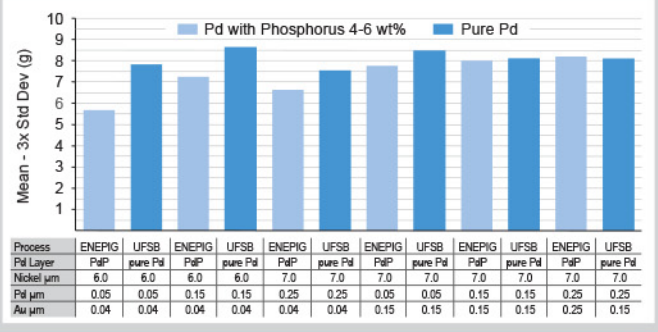
Gold Wire Bond Finish

Copper Wire Bond Finish

Gold Wire Bond Pull Test



Process	ENEPIG	UFSB	ENEPIG	UFSB	ENEPIG	UFSB	ENEPIG	UFSB	ENEPIG	UFSB	ENEPIG	UFSB
Pd Layer	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd
Nickel µm	6.0	6.0	6.0	6.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0
Pd µm	0.05	0.05	0.15	0.15	0.25	0.25	0.05	0.05	0.15	0.15	0.25	0.25
Au µm	0.04	0.04	0.04	0.04	0.04	0.04	0.15	0.15	0.15	0.15	0.25	0.15

Universal Finish SolderBond provides also with low Au-thickness excellent results, as pure Pd is 50% softer than Palladium-Phosphor (4-6wt%).

	NiPdAu (ENEPIG)	NiPd (ENEP)
Deposit Structure		
Electroless Nickel	4.0 µm - 6.0 µm	4.0 µm - 6.0 µm
Electroless Palladium	0.05 µm - 0.3 µm	0.2 µm - 0.3 µm
Immersion Au	0.02 µm - 0.06 µm	--
Functionality		
Soldering		
Eutectic Sn/Pb	Good	Good
Sn-Ag-Cu Alloy	Excellent	Excellent
Contact Switching	Yes	--
Al Wire Bonding	Yes	--
Au Wire Bonding	Yes	--
Cu Wire Bonding	--	Yes

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- ENEP is Cu-wire bondable
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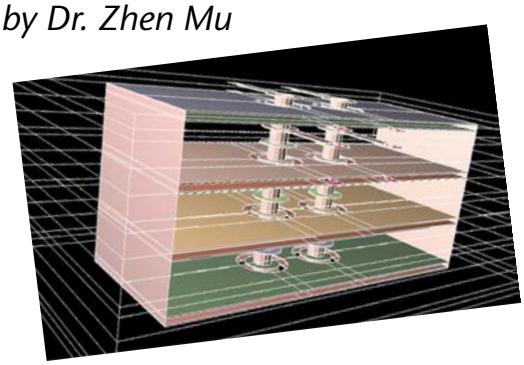
HDI

This month, industry veterans Happy Holden, Mike Carano, Joe Fjelstad and others weigh in on advances in high-density interconnect technology that have become established as enablers for a new generation of mobile devices and high-tech electronics.



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The Next Generation High Speed Product from Isola

- Global Constructions available in all regions
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- Improved Z-axis CTE 2.70%
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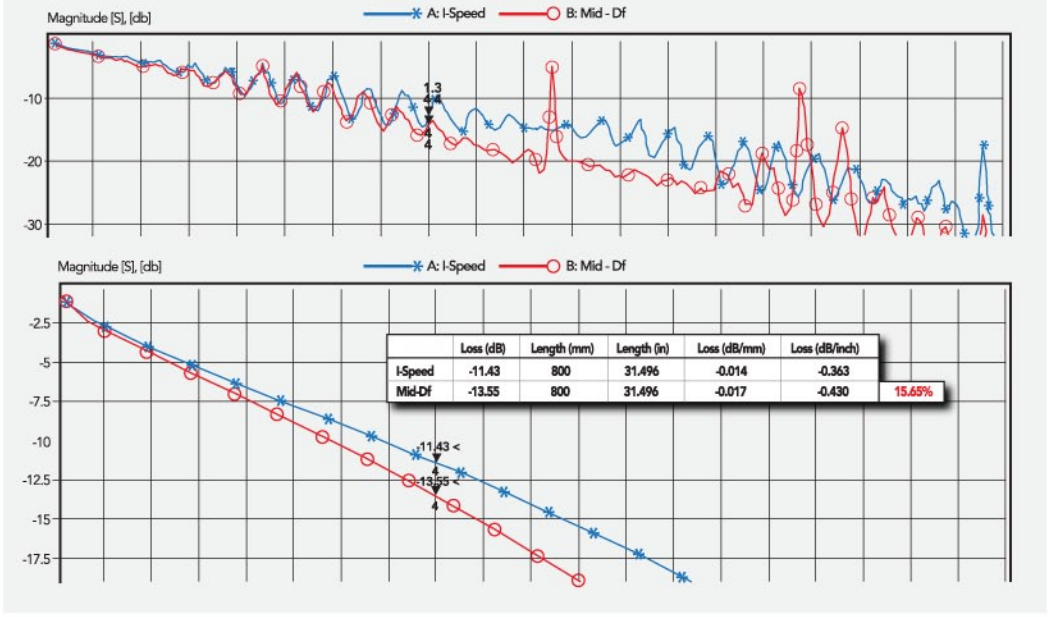
- Offer spread and square weave glass styles (1067, 1086, 3313, etc.) for laminates and prepregs
  - Minimizes micro-Dk effects of glass fabrics
  - Enables the glass to absorb resin better and enhances CAF capabilities
  - Improves yields at laser and mechanical drilling
- A low Df product with a low cost of ownership

Effective Loss @ 4 GHz on a 32 inch line



	Loss (dB)	Length (mm)	Length (in)	Loss (dB/mm)	Loss (dB/inch)	
I-Speed	-11.43	800	31.496	-0.014	-0.363	
Mid-Df	-13.55	800	31.496	-0.017	-0.430	15.65%

I-Speed delivers 15-20% lower insertion loss over competitive low Df products.

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Manufacturing Renaissance: For Show or For Real?

by Ray Rasmussen
I-CONNECT007

SUMMARY: It really never made sense to send most of our manufacturing to China. For some products, China was a no-brainer, but for many others it wasn't the lowest-cost producer. Now, more and more companies are figuring that out.

Apple's recent announcement that they'll be bringing back some manufacturing to the U.S. made headlines around the world. Market experts were quick to point out that the iMac mentioned by Apple CEO Tim Cook represents a very small piece of Apple's product portfolio and not a heck of a lot of volume. Although the comments by Cook caused quite a stir, it wasn't unexpected. Companies like Apple will do the right thing for their businesses. The decision was probably made to reduce shipping costs since some of the heaviest components (like the glass) are already made here, in the U.S. And, I suspect that most iMacs are sold here in the U.S., as well. I'm certain that whatever they do here in the States will likely be highly automated, making labor costs a non-issue. They'll probably save money on the deal so it's not an altruistic, support-American-jobs endeavor. Nor should it be.

Steve Jobs' famous comments to President Obama that the types of jobs created by assembly of the iPhones, iPads, iPods, etc., are never coming back is spot-on (although "never" is a long time). They won't come back and we don't want them. They aren't good for the economy or for American workers. If this type of manufacturing does return to North America we'll see factories filled with Foxconn's robots building them. And, as we've read over the last year or so, that will happen even in low-cost regions. Automation will be the great geographic playing-field leveler. It's going to remove labor from the equation.

Geography, Oil, and the Fukushima Effect

With labor becoming less and less of an issue, it's going to ultimately come down to the cost of moving components and then the final product to the assembly locations and end-markets. As factories around the

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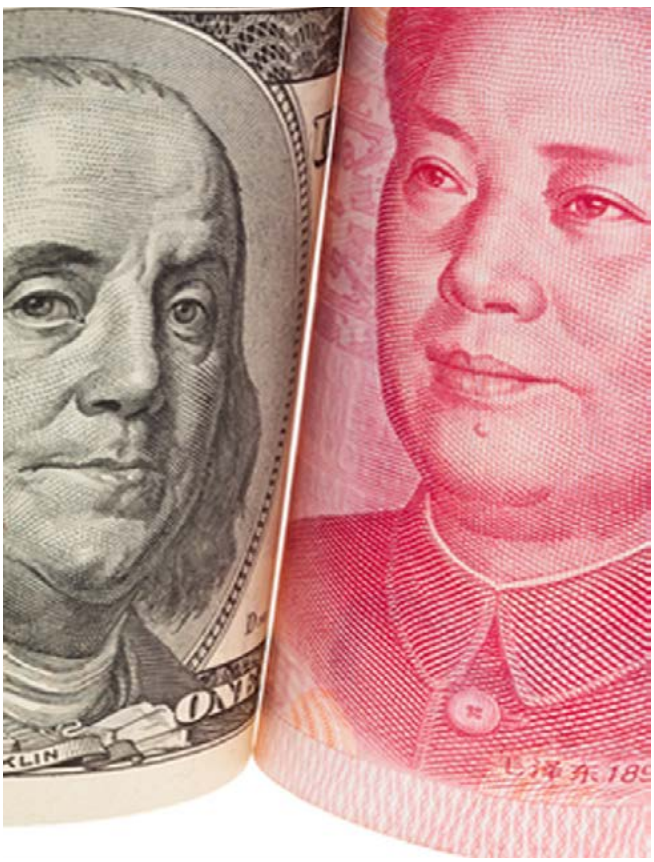
world continue to drive the cost of labor out of their products, the location of final product assembly will ultimately come down to the cost and time associated with shipping. As supply chains relocate to support their OEM/EMS customers and to diversify their operations to avert the effects of disasters like Fukushima and the floods in Thailand, both of which disrupted the global supply chain, the supply base's location won't be a huge issue since all facets will be represented in all major geographical regions.

Flextronics CEO Mike McNamara said this recently about onshoring: "I think moving production back to the U.S. is a process, or it is a journey, almost. As our costs become pressured, it makes other choices more interesting. So, what that is going to do is probably push more work into Mexico. And, over time, as those costs continue to go up, you'll probably see more things get pushed back into the USA."

IPC's recent report about EMS companies returning to North America echoed McNamara's comments, mostly. The comments aren't reflective of some great renaissance of buy or build American; it's really just the markets doing their stuff. As the vacuum created by China fills (extremely low wages, costs and currency exchange rates giving way to normalized manufacturing costs), markets will tend to seek out balance. That balance is simply the market's way of leveling out and finding the lowest overall costs. For instance, much of the manufacturing in China will, more and more, service the Chinese and regional Asian markets just as European manufacturing will mostly serve the European market. The need for more secure, diversified supply chains will help move this along. Still, in regional markets, as we're seeing, manufacturing will flow into the lowest cost areas, i.e., Mexico for North America, Eastern Europe for Europe, South Asian countries for Asia, etc. The nice thing about being a global EMS provider is that they can turn on or off manufacturing as needed to take advantage of logistical or geographic opportunities to support their customers.



More Markets

As countries develop, they become targets for low-cost, regional manufacturing. The development of these markets creates many more consumers for the products we build. Just think about it. If we hadn't had the Chinese entry into the market in such a big way, there would be hundreds of millions of fewer consumers for electronic products. From Boeing, which predicts the need for 34,000 (not a typo) new planes over the next 20 years (7,400 in N.A. and the rest overseas) to Apple, sales would be dramatically less, leaving far fewer good paying jobs in the U.S. The World Bank said this about China's progress:

China's dramatic progress in reducing poverty over the past three decades is well known. More than 600 million people were lifted out of poverty as China's poverty rate fell from 84% in 1981 to 13% in 2008, as measured by the percentage of people living on the equivalent of US $1.25 or less per day, in 2005 purchasing price parity terms.

Those 600 million consumers are having quite an impact on the global economy and on the economy of the United States and Europe.

And, China is lifting most of Asia. I thought these comments, again, from the same World Bank report, were quite interesting:

Rapid economic ascendance has brought on many challenges as well, including high inequality; rapid urbanization; challenges to environmental sustainability; and external imbalances. China also faces demographic pressures related to an aging population and the internal migration of labor.

Significant policy adjustments are required in order for China's growth to be sustainable. Experience shows that transitioning from middle-income to high-income status can be more difficult than moving up from low to middle income.

Now, think beyond China. South Asia's countries have a population of about one billion and India has another billion. Those 2 billion people along with China's billion+ represent quite a few consumers for the sophisticated goods coming out of the developed world. The more cell phones they buy, the more cell towers and communications infrastructure they'll need along with medical services, banking, cars, computers, and more.

Another article in MIT's Technology Review, "Manufacturing in the Balance," talks about the future of manufacturing belonging to technology, leaving the decade of inexpensive labor behind. The article starts out with GE's expansion of their appliance manufacturing facility in Kentucky last year and repatriating their manufacturing from China and South Korea. GE's CEO Jeffrey Immelt addresses the major driver for their decision: "At a time when speed to market is everything, separating design and development from manufacturing didn't make sense. Outsourcing based only on labor costs is yesterday's model."

What blows me away is that a company the size of GE didn't get this until now. Hell, I could be their CEO. I wouldn't have made that mistake. Before shifting manufacturing to China I certainly would have carefully considered all my costs of product development and manufacturing.

We don't have to bring anything back to the U.S. It will come on its own, when it makes the most sense or when these companies come to their senses. It really never made sense to send most of our manufacturing to China. There were scores of articles over the last decade by very competent groups trying to open the eyes of those rushing to China. Sure, for some products China was a no-brainer, but for many others they weren't the lowest cost producer. Now, we're seeing more and more companies figuring that out.

> ***"There were scores of articles over the last decade by very competent groups trying to open the eyes of those rushing to China. Sure, for some products China was no-brainer, but for many others they weren't the lowest cost producer."***

I do believe that the longer low-cost manufacturing stays overseas and helps developing countries, employing future consumers, pulling people out of poverty, the better it is, ultimately, for us all. Leave the stuff that makes sense in those countries and bring the rest back.

I know not everyone agrees with me on this, but if you're thinking short-term you'll miss the tremendous opportunity this affords the developed world. Look at the big picture, and position your business accordingly. If you don't, you'll spend most of your time complaining about low-cost competition instead of reaping the rewards of an expanding global market. **PCB**

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine*. Contact Rasmussen here.

Multilayer Thickness Reduction: Adapting to Lead-Free Assembly

by Happy Holden
GENTEX CORPORATION
and Michael Carano
OMG ELECTRONIC CHEMICALS, LLC.

Abstract

One of the most difficult printed circuit boards to adapt to Pb-free assembly processes is the high-layer count multilayer. Often, these multilayers have through-hole and hand-soldered components, and requirements for two or more rework cycles. The higher reflow temperatures and slower wetting of lead-free solders place an enormous strain on the laminate and copper-plated hole barrel. In many cases, the boards cannot be assembled reliably even with newer, higher thermal performance FR-4s.

One solution to this problem is to redesign the multilayer using current design rules and newer innovative fabrication technologies. This paper will review four of these new and enabling technologies:

- Laser-drilled microvias
- Routing BGA using channels
- Contribution of new SMT connectors
- Layer assignment changes (architectures)

Microvias offer the most significant opportunity to reduce not only the layers and thicknesses of multilayers, but also their cost while improving their electrical performance and density. Several examples will illustrate these new opportunities. Since blind vias are surface phenomena, to get the maximum benefit from them, layer assignment for signal, ground and power need to be reviewed and alternative constructions considered. These blind vias, by reducing the number of through-holes, contribute to increase routing density that allows the lower layer usage. Finally, by replacing through-hole connectors with surface mount connectors, higher connector density and improved electrical performance can be realized.

The resulting new multilayers are not only thinner, cheaper, and easier to design, but are less costly and suitable for lead-free assembly.

Challenges of Lead Free

Environmental regulations are placing increased requirements upon printed circuits. The European Restriction of Hazardous Substances (RoHS) and Waste Electrical and Electronic Equipment (WEEE) directives will significantly affect the requirements placed upon base materials. Among other elements, RoHS restricts the use of lead (Pb). Tin/lead (Sn/Pb) alloys have been used for many years in the assembly of printed circuits. Eutectic Sn/Pb has a melting point of 183ºC and temperatures during assembly commonly reach 230°C. The primary alternatives to Sn/Pb are tin/silver/copper (Sn/Ag/Cu or "SAC") alloys. These alloys have melting points near 217°C with typical peak assembly temperatures reaching 255-260°C. This

increase in assembly temperature coupled with the possibility of multiple exposures to these temperatures requires the base materials to have improved thermal stability. Recent technical papers have illustrated important data on the effect of Pb-free assembly on base materials[1,2]. While there are many important properties to consider, there are a few that deserve special attention in light of current trends and the resulting need for improved thermal performance. These include:

- The glass transition temperature (T_g),
- Coefficients of thermal expansion (CTEs),
- Decomposition temperature (T_d)

Effect on Laminates

As the temperatures to which printed circuits are exposed to increases, as in Pb-free assembly processes, the decomposition temperature of the material becomes a much more critical property to understand[4]. The decomposition temperature is a measure of actual chemical and physical degradation of the resin system. This test uses thermogravimetric analysis (TGA), which measures the mass of a sample versus temperature. The decomposition temperature is reported as the temperature at which 5% of the mass of the sample is lost to decomposition. Experience is showing that the decomposition temperature is a critical property, and appears to be at least as important, if not more important than the glass transition temperature when planning for Pb-free assembly conversion. While the definition of the decomposition temperature uses a weight loss value of 5%, it is very important to understand the point at which 2-3% weight loss occurs, or where the onset of decomposition begins. In examining soldering reflow profiles, traditional Sn/Pb assembly processes can reach peak temperatures of 210°C to 245°C, with 230°C a very common value. In this range, most FR-4s do not exhibits significant levels of decomposition. However, if you examine the temperature range where Pb-free assembly processes are operating, you can see that the traditional FR-4 materials exhibit a 2-3% weight loss. Severe levels of degradation can result from multiple exposures to these temperatures. This problem is increased when there are 20+ layers, resulting in thicker boards, and many are power or ground planes.

Consequences for Multilayers

While the simplest steps to comply with Pb-free assembly may be changing the base laminate and replacing the tin-lead finish, this may not be suffiecient for thick, complex, high-layer-count multilayers. These multilayers have a much higher thermal mass as well as increased through-hole parts and copper planes. With the possible increased need for rework of complex parts and hand-soldering, the total thermal environment may exceed what any FR-4 is capable of. When this occurs, the remedy is to reduce the thermal mass by reducing the mulitlayer's layers. Four main alternatives that can be used are:

> ***"With the possible increased need for rework of complex parts and hand-soldering, the total thermal environment may exceed what any FR-4 is capable of."***

1. Laser-drilled microvias
2. Layer assignment changes (architectures)
3. Routing BGA using channels
4. Contribution of new SMT connectors

Moving to Microvias

Microvias are nearly 30 years old now, having been used in high-volume by OEMs like Hewlett-Packard for their first 32-bit computer—the FOCUS chip—in their HP9000 m845 desktop computer starting in 1983. They employed laser drilling of blind vias in an 8-layer PTFE dielectric with copper used as the core layers for cooling (termed "finstrate" for this feature). Other OEMs like IBM and Siemens also developed microvias technologies for their computers, but the technology did not really take off until the need for miniturization in portable products like cellular phones increased. Today it is the fasting growing segment of inter-

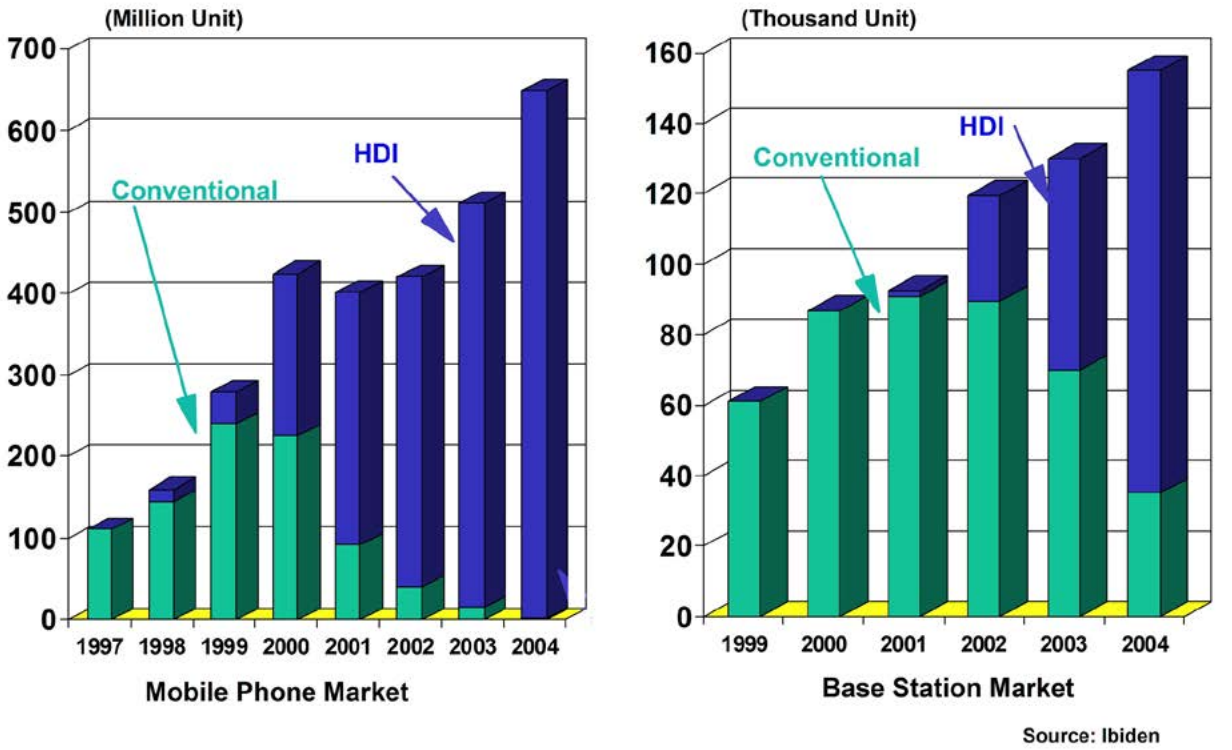


Figure 1: The rapid increased use of microvias has been fuelled by the popularity of cellular phones and the need to make them as small and as light as possible. Now, all products use microvias.

connect packaging, used in portable products, IC and ASIC packaging and in large complex multilayers for telecom and servers. Figure 1 shows the rapid growth of microvias during the early 2000s.

Multilayer Cost-Density Tradeoffs

In designing classical PWBs, there is a wiring barrier created by the size of component lands, traces and vias. If you look at a square inch of PCB real estate, there are only so many SMT land patterns, traces connected to the land and vias connected to the trace that you can put in that one square inch before it is full. Depending on the SMT land size, this barrier is called the TH wiring barrier[3].

HDI-microvias provide the opportunity to reduce the number of layers of traditional through-hole boards. Typically, microvias are 6 mil with 12-mil pads, while TH vias are 13 mils with 24-mil pads. This obvious increase in space is multiplied by the fact that a blind via only goes from the surface down to the second or third layer. This opens up additional channels on the rest of the innerlayer to route additional traces. The other opportunity with HDI is the reduction of trace widths to go along with the reduction in dielectric thicknesses. Three mil (0.003") are not uncommon as well as 3.5-mil lines and spaces. This provides the opportunity to route 80 to 100 traces per square inch.

This increase in density is illustrated in the cost-density tradeoff chart (Figure 2). The first column (A) is traditional TH boards from 4 to 40 layers. The prices (RCI) have all been adjusted to a basis of the cost of an 8-layer TH board from China. The DEN is the average density of the stackup in pins per square inch. To find the equivalent of a particular TH board, move diagonally, following the dashed lines.

For example, if you had a 22-layer TH multilayer (RCI=6.67), the HDI type II (D) would be a 14-layer board (RCI=3.32); the type III (E) would be a 10-layer, RCI=2.30. These all have approximately the equivalent DENsity, but the HDI boards are less costly by 50% for the type II and 65.5% for the type III.

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Layer Assignment (Architecture)

Blind microvias are a surface feature. In order to help reduce the number of layers of a traditional multilayer with microvias, more work needs to be performed on the three surface layers of each side of the board. What this looks like is illustrated in Figure 3.

First priority is to reduce and eliminate through-vias. These block routing channels on the innerlayers. By eliminating 25% of the TH, two to three times as many traces can be routed on the innerlayers. One way to do this is to move the ground-plane (usually on layer 2) to the surface and use the microvias as via-in-pad (VIP) or near-via-in-pad (NVIP). This eliminates the most abundant vias on the boards—the ones to ground. In non-critical areas, this surface ground pour can be connected to other ground layers. The second most abundant vias are to power, so by moving this plane to layer 2, a blind via can connect SMT pads to this plane and not be very deep. Signals will start on layer 3, and depending on line-width, these skip-vias will not be very deep and will have a conventional aspect ratio and land size.

If higher wiring density is required, then layer 2 and 3 should be signals. If fine lines are used (~3 mil), then skip vias will allow X-Y connections, otherwise, buried vias (type II) or buried microvias (type III) are required to connect the two signal layers.

THRU-HOLE VS. STAGGERED MICROVIA HDI: COST & PIN DENSITY

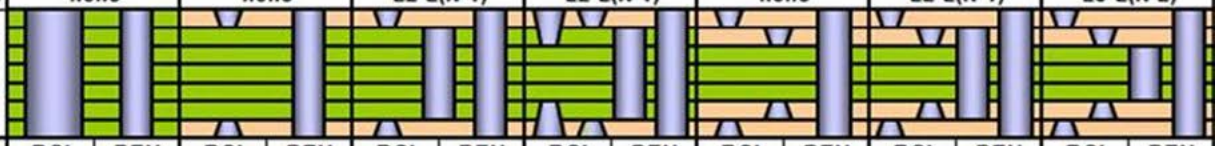
ID	A		B		C		D		E		F		G	
Type	THRU-HOLE		1 BUILD-UP Blind		1 BUILD-UP Blind & Buried		1 BUILD-UP Blind & Buried		2 BUILD-UP Blind		2 BUILD-UP Blind & Buried		2 BUILD-UP Blind & Buried	
Stackup	N		1+N+1		1+bN+1		1+bN+1		2+N+2		2+bN+2		2+bN+2	
Micro Vias	none		L1-L2		L1-L2		skip via L1-L3 stagger L1-L2, L2-L3		stagger L1-L2, L2-L3		stagger L1-L2, L2-L3		stagger L1-L2, L2-L3	
Buried Vias	none		none		L2-L(N-1)		L2-L(N-1)		none		L2-L(N-1)		L3-L(N-2)	
Stackup & Via Models														
Signal Layers	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.6	20	0.8	40	1.1	40	1.3	40	1.4	135	--	--	--	--
6L	0.8	20	1.0	60	1.2	60	1.5	60	1.6	180	1.7	220	1.9	240
8L	1.0	30	1.2	100	1.5	100	1.7	100	1.9	240	2.1	240	2.3	300
10L	1.3	40	1.5	200	1.8	180	2.1	180	2.3	300	2.5	300	2.7	400
12L	1.7	60	1.9	210	2.3	220	2.6	220	3	350	3	500	3	500
14L	2.2	70	2.5	220	3	250	3	260	4	400	4	600	4	600
16L	3	80	3	260	4	300	4	300	5	500	5	800	5	800
18L	4	100	4	300	5	330	5	350	6	600	6	1000	7	1000
20L	5	105	5	360	6	380	7	400	8	700	8	1200	9	1200
22L	7	110	7	400	8	425	9	450	10	800	10	1300	11	1300
24L	9	125	9	460	10	480	11	500	12	1000	13	1400	14	1400
26L	11	130	11	500	13	550	14	600	15	1200	16	1500	17	1600
28L	13	135	14	540	16	620	17	700	18	1300	19	1600	29	1800
30L	16	140	17	580	18	690	20	800	21	1400	22	1650	23	2000
32L	18	145	19	620	21	770	23	900	24	1450	25	1700		
34L	21	150	22	660	24	900	26	1200	26	1500	27	1800		
36L	23	160	24	700	26	1000					30	2000		
38L	25	180	26	740	RCI = Relative Cost Index									
40L	26	200			DEN = Density: Pins/Square Inch						© Happy Holden 2006-2011			

Figure 2: The price-density matrix compares the relative prices (RCI) of through-hole (TH) boards to their equivalent HDI-microvias boards, along with average density (DEN) of pins per square inch[3].

Routing BGAs Using Channels

Noting the importance of using the blind microvias to eliminate TH, a second important function, especially on large boards that have high I/O BGAs, is where the microvias are placed. Historically, the blind vias were placed around the perimeter of the BGA. This works well for BGAs with <400 pins, but for the new BGAs, like FPGAs, which contain 300 to more than 1700 pins, the blind vias are placed differently. In theory, take a 1153 pin (34x34) BGA. It will have 132 possible routing escapes per layer (one trace between vias) plus 20 traces in the channel (five traces). This means that eight layers would be required (plus five plane layers) to connect this BGA to the rest of the circuit. The TH vias create a "fence" that makes routing very layer- intensive.

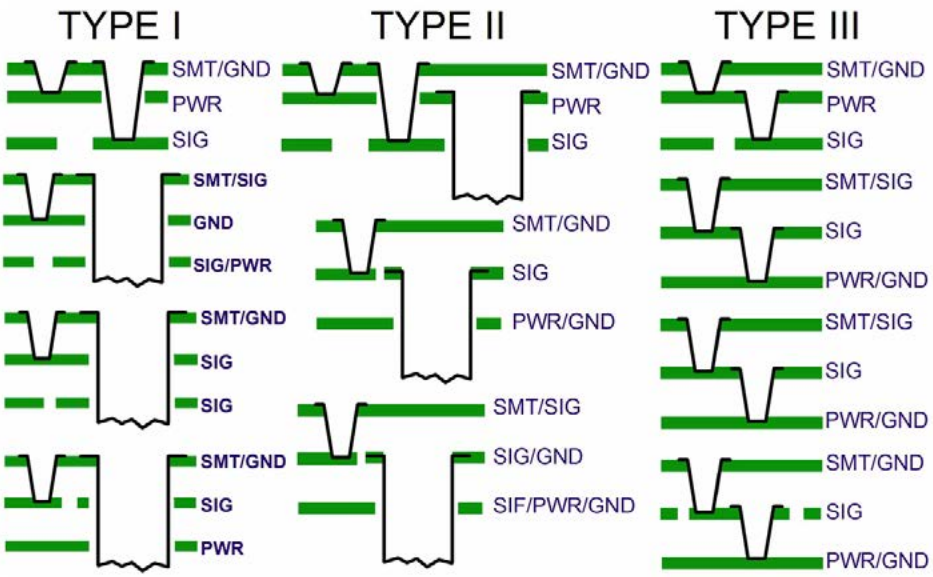


Figure 3: Various layer assignments available when using HDI and microvias. The goal is to remove as many TH as possible to free up routing space on the innerlayers.

If we create more routing channels on the innerlayers by placing the blind vias on the surface, we connect more traces per layer and reduce the total layers. Channel routing uses blind microvias to form four or more additional cross-shaped, L-shaped or diagonal channels in a BGA fanout pattern. These new channels allow up to 48 extra connections per layers for this BGA (8x6 traces). Four routing layers and four plane layers can be eliminated in this example.

In some cases, the channel is not to escape the inner-pins of a BGA but to allow access to an adjacent BGA. The blind vias can be via-in-pad, near-via-in-pad or traditional dogbones. If working with a FPGA where pin swapping is possible, then the channels should be assigned to ground and power first.

Contribution of New SMT Connectors

Press-fit connectors require the use of through-holes. For thick boards, this might necessitate the use of back-drilling (Figure 4a) to reduce the inductance of these vias. Because of the sensitivity of high-speed circuits to parasitic inductance, even SMT connections might require their through-holes to be reduced to blind-via stubs (Figure 4b). But by using microvias, either in pad or off-pad, the need for larger through-holes is reduced as well as the resulting parasitic inductance, as seen in Figure 4c. Figure 5 shows the reduction in overall insertion loss due to the use of BGA connectors and blind-microvias instead of through-holes. If BGA connectors are used on the backplane or midplane, a 33% reduction is possible. If blind-microvias are used, then a 67% reduction can be realized. This also facilitates higher-density routing and fewer signal layers and their reference layers.

High-frequency, controlled-impedance SMT matrix-connectors are now becoming available. These are BGA-type. Typical is the header for a backplane or midplane daughter card. These are remarkable for helping to reduce the thickness of multilayers.

The Role of Reliable Blind Vias

At the end of the day, one must develop core competencies at the fabrication side of the supply chain, for the process chemistry side. Keeping in mind one is ultimately working to

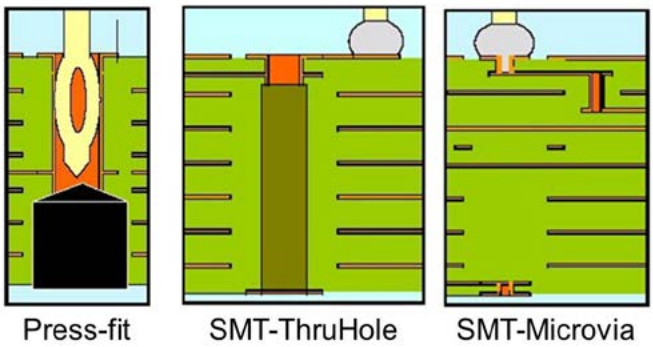


Figure 4: Press-fit connectors create a need for thick boards that require higher reflow temperatures and durations. (a) Many times, the increased inductance require backdrilling. (b) Even with surface-mounting, the through-hole plating may have to be eliminated. (c) Microvias increase density, reduce thickness and reduce inductance.[5]

build long-term reliability in the printed wiring board. While many of those competencies have been discussed in this paper, it would be wise to expound on the critical success factors and process competencies required to build reliaibility into the microvia.

Key Processes

Several processes must be implemented in order to ensure success with blind vias and the overall goal of reducing the number of layers in the package. These are:

- Desmear
- Metalization
- Electrodeposition

This issue becomes increasingly complicated as HDI migrates into designs containing both through-holes and blind vias.

Desmear

Consider the need to ensure a clean and active capture pad and its importance on via reliability. Any residue remains on the capture pad will at the very least impact plating adhesion (Figure 6).

The residues could be from incomplete ablation with the laser or inadequate performance from the desmear chemistry (either alkaline permanganate or plasma). It is wise to ensure that the alkaline permanganate (if used) must be optimzed for the type of resin in the particular HDI build-up. Care must be talken to avoid aggressive attack of the resin at the interface of the via wall and capture pad.

When processing resin materials that formulated for lead-free assembly, the engineer must be cognizant of the fact that these Pb-free designed resins are more resistant to alkaline permanganate chemistry than the lower T_g resins. It would be wise to consider alternative desmear protocols such as combinations of plasma desmear and alkaline permanganate. A second options is to use newer generation solvent swell chemistry, which is better designed to effect penetration into the resin-polymer matrix.

Metalization

After the desmear process, the task now is to insure a continuous, conductive and void-free deposit on the via walls and capture pad. Today, there are several processes that can be utilized to render vias conductive, including:

- Conventional electroless copper
- Palladium based direct metallization
- Graphite
- Carbon black
- Conductive polymer

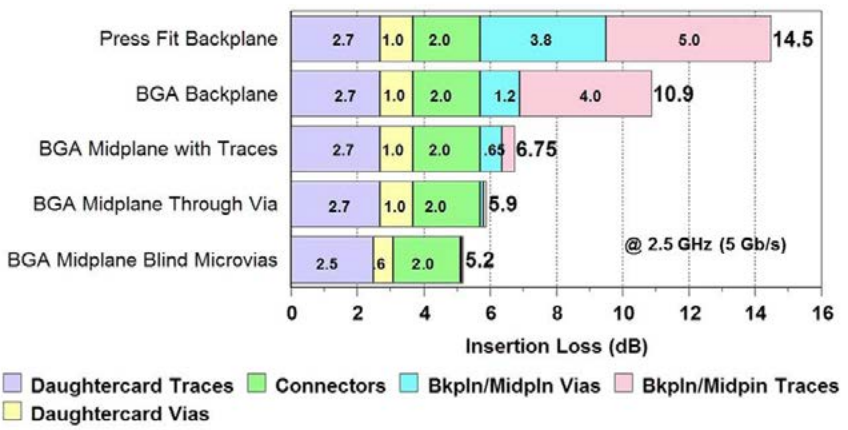


Figure 5: Total insertion loss from backplane-daughter cards' architecture from various contributors like traces, connector and vias[6].

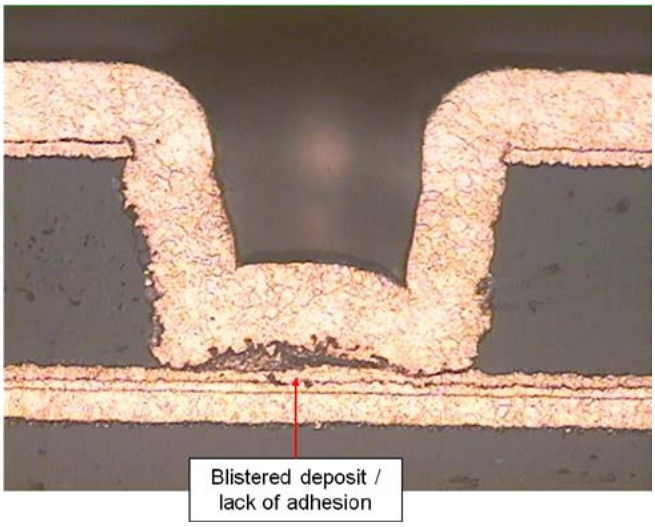


Figure 6: Debris on capture pad preventing adhesion of plated copper.

These metalization processes (also known collectively as "making holes conductive" or MHC) are well developed for both plated through-hole and blind-via metallization. Direct metalization in particular is applicable to horizontal processing, although vertical systems can also be used. These processes typically involve the deposition of a conductive coating (palladium, conductive polymer, graphite, carbon black). This step is then followed by electrolytic copper. Thus, the actual electroless copper step is eliminated.

These processes have been presented and thoroughly discussed elsewhere[7], while direct metalization processes may reach certain limitations for use with very high-aspect ratio rigid circuit boards, these processes are highly efficient and effective for HDI. Direct metalization systems primarily function by coating the substrate, as opposed to a true chemical reaction type process such as electroless copper. Contrarians of direct metalization point to sheet resistance measurements of the direct metalization coatings versus electroless copper. Yet while the DM films are somewhat less conducitve, most of the DM processess have resistances in the neighborhood of 5-25 ohms square. This is more than sufficient to promote electroplating propagation in blind vias and mid- to high-aspect ratio plated through-holes.

Another advantage that DM processess have over conventional electroless copper is the ability of these DM films to render higher-performance material conductive without overly aggressive desmear tactics. It is well known that electroless copper requires sufficient roughening of the resin to promote palladium adsorption and to ensure adhesion of the subsequent copper deposit. However, most direct metalization processess require only minimal resin roughening to promote adhesion. This is because the more popular systems commercially available today rely on coating technology. And with the use of special polymers, these DM materials bond and adhere to a wide variety of resin materials with relative ease[8].

Electrodeposition of Copper

After the vias are rendered conductive, the subsequent acid copper depostion step is required to further enhance the conductvity of the vias and to build reliability into the package. With respect to HDI and blind vias, the fabricator has two plating options available. The first involves what is known as conformal plating (Figure 7). The second option is known as superfilling of the vias with electroplated copper (Figure 8). In the former, the plated copper simply conforms to the via wall and capture pad. Ideally, one strives to minimize any overplating on the surface while ensuring good throwing power into the blind via. When HDI designs require via stacking, generally complete filling of the blind via is indicated. Even if there are no stacked vias, it is usually necessary to completely fill the blind vias either with copper plate or a via fill plugging paste[9]. Copper is more thermally conductive than these polymeric pastes and thus provides an excellent means to transfer heat through the package. There are several other reasons to superfill blind vias. These are:

- To increase the density and frequency for PCB
- To minimize signal delays and avoid effects of electron migration
- To make a smooth surface layer and avoid indentations
- To enhance the I/O number of package substrates

- To avoid incomplete fill of microvia hole filled by dielectric or conductive materials
- To solve the differences in coefficient of expansion of metal and resin
- To improve fine line design, via-on-via and interconnect reliability

As high-density designs depend on the maintenance of of fine lines and spaces, concern arises over the loss of circuit conformity due to overetching of the circuit pattern. One way to prevent this situation is to minimize plated copper on the surface while enhancing throwing power into the via. This can be accomplished with either DC (direct current) or PPR (periodic reverse plating).

However, with recent developments in new pulse plating rectifiers, special organic addition agents and analytical control methods, PPR plating is becoming the method of choice for HDI. PPR plating tends to produce better throw into small holes and blind vias at higher current density than is practical with DC plating. As with DC, the current density used may need to be reduced as the work becomes more difficult, but there is usually a significant advantage for PPR, particularly when plating very small blind vias (e.g., less than 6 mil/150 micron diameter). PPR with proper plating parameters is able to increase the plating thickness in blind vias and high aspect ratio through-holes while helping to reduce the plated thickness on the surface. This aids in reducing undercut of the fine circuit traces during the etching operation. For maximum advantage in throw, the current density, pulse waveform and brightener concentration used should be optimized for the individual application, but "middle ground parameters" can often be found where most types of work will give acceptable results.

Superfilling of Blind Vias

While a conformal copper plating technique works well for blind via HDI applications, many fabricators have migrated towards the superfilling of the blind vias. This is especially useful if stacked via designs are employed.

This type of design is benefical in that the designer gains significant routing space and increased wiring density. A key requirement

Figure 7: Example of conformal acid copper plating in a blind via.

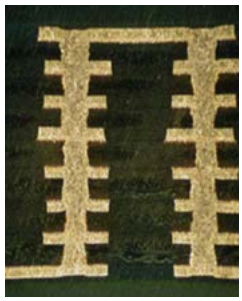


Figure 8: Superfilled and stacked vias.

of superfilling or bottom-up filling as it is often referred to is to deposit copper at a faster rate from the bottom, as opposed to the surface. This is referred to as the RDR or relative deposition ratio. A critical aspect of this process is the interaction of the various components of the organic addition agent. In this scenario, the brightener componet of the additive package selectively accerlates the deposition of the copper from the bottom, up, while the carrier and leveler componets of the addition agent package work to minimize overplating on the surface. Certainly, other parameters play a role in this as well. Generally, higher copper/lower acid ratios of the electrolyte benefit bottom-up filling, as does direct impingement solution movement as opposed to air agitiation. Secondly, several fabricators have enjoyed improved RDR results by using a dual step DC plating current density. As an example, plate the first 45 minutes of the cycle at 10-12 amps per suqare foot (ASF), then ramp up to 20-25 ASF[9].

Example of Telecom Redesign

A major telecommunication company recently experimented with this concept. They took a recent 22-layer, TH optical-input board (0.127" thick) and redesigned it to a 14-layer HDI board of 0.063" thickness (1+12+1), without moving or changing any part locations. Figure 9 shows the old 22-layer stackup compared to the new 14-layer HDI stackup. The boards were 8.50" by 14.34" with 702 parts (mostly BGAs and actives), having 8,759 pins on the PRI side and 2,036 parts (mostly passives) having 4,206 pins on the SEC side. There were ori-

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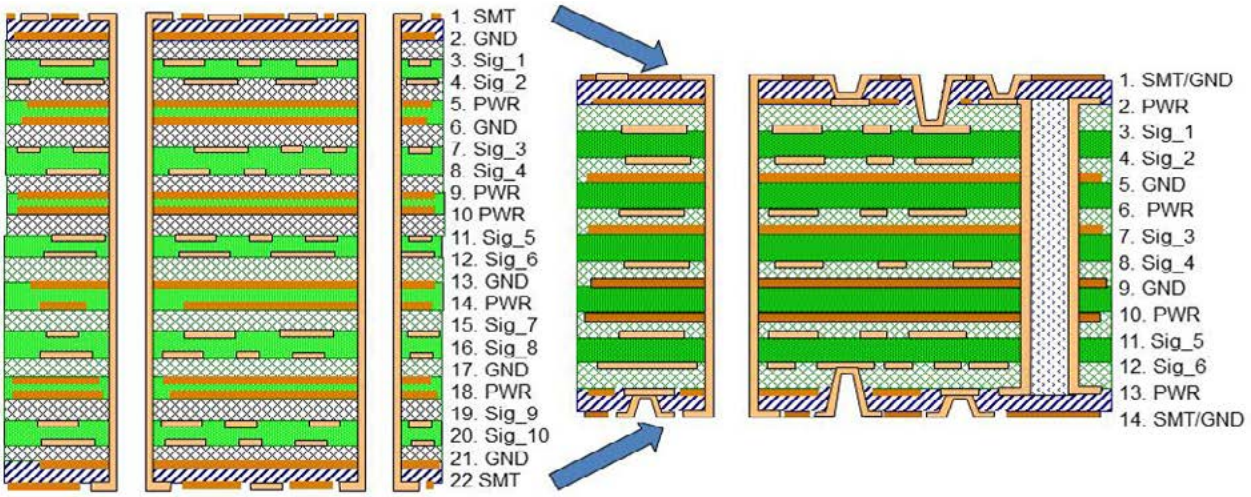

Figure 9: Conversion of a 22-layer TH multilayer to a 14-layer HDI (1+12+1) in order to reduce its thickness from 0.127" to 0.063" to gain reliability in LF SMT assembly.

gnally 12,610 drilled TH in the original version, but only 3,887 in the HDI version; the rest were laser-drilled microvias.

Conclusion

One of the more difficult type of multilayer to get to accept a lead-free assembly process is the thick, high-layer count with through-hole parts and multiple PWR/GND planes. HDI techniques can help in the reduction of thickness and number of layers for these types of boards, resulting in thinner multilayers, but also reducing the costs by 50% and improving the high-frequency performance and reliability. Further, the fabricator can enhance the overall relaibility and manufacturability of HDI substrates by adopting direct metalizaton and new technologies in electroplating such as copper super fill and periodic reverse copper plating (PPR). These processess aid in building reliability into the vias that lead-free assembly requires. **PCB**

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A Perspective on High-Density Interconnection Technology

by Joe Fjelstad
VERDANT ELECTRONICS

SUMMARY: High-density interconnection technologies perform a vital service to the broader electronics interconnection industry by providing a reliable platform that can support the interconnection needs of today's highly integrated and component-dense electronic assemblies.

For technology history buffs, tracing the evolution of printed circuit technology is a fascinating field of interest and study. While there have been many different methodologies employed over the last seven decades to create what is arguably the foundation of all electronic products, there are really but two fundamental constants which have served as "genetic markers," allowing the observer to track technological change over time. Those two fundamental constants are conductor width and via (or hole) diameter.

Early printed circuits were quite crude by today's standards, with circuit conductor features that are commonly run to widths of a few tens of mils. When this writer first entered the printed circuit industry more than four decades ago, 20 mil line and space was mainstream and 10 mil line and space was considered fine line. Over the course of four decades, those features have dropped by more than an order of magnitude for many advanced circuits such as those used in many of today's advanced handheld devices. The progression from 10 mil line and space fine line circuitry of the 1970s down to one mil line and space circuit features employed today has been slow but steady over time. Interestingly, however, there was advanced work being done in the 1980s which presaged the technology that we now call high-density interconnection. The catalyst for change was the introduction and early-stage adoption of surface mount technology, which opened floodgates of opportunity to electronic designers and gave birth to the rallying cry of "smaller, faster, cheaper and better" that remains a mantra for electronic product developers even to today.

One of the major advantages of surface mount technology was that component lead terminations could be provided on much smaller pitches than through-hole technology. This allowed for greater functionality in a smaller space and also allowed components to be placed closer to one another, giving rise to improved

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performance by reducing time of flight for signals from component to component. The elimination of the need for plated through holes to connect components to circuit boards also returned large amounts of real estate to the designer. In fact, one of the ironies of through-hole interconnection technology is that a substantial amount of board real estate was consumed by holes that are by definition the absence of material; or put another way, holes are nothing, and yet were one of the more expensive features of a traditional printed circuit. Thus it was with the introduction of surface mount technology, and especially peripherally leaded components such as the SOP, TSOP and PQFP that the seeds of high-density interconnection technologies were first planted and began to take root as first plated through vias and then blind and buried vias began to replace the more traditional plated through-hole technology.

However, one must fast-forward another 10 years to the late 1980s and early 1990s and the introduction and early adoption of, first, area array packaging technologies in the form of BGAs, and later CSPs, to see that there would truly be need for advanced printed circuit manufacturing technologies to meet the demands that were being foisted upon the industry by these attractive, but challenging new integrated circuit packaging formats. Area array packaging technologies in BGA and CSP form allowed package developers and circuit designers to provide much more function on a much smaller footprint and do so without having to deal with the long delicate leads of fine pitch QFPs, whose poor assembly yield and less than ideal electrical characteristics make them an increasing liability to the manufacturing process.

What followed in the wake of the introduction of these new high-density area array packaging formats was the need for much more advanced ways of manufacturing interconnection substrates to serve them. Thus, from the mid-1990s to the end of the decade, there was a flurry of development work creating a host of new ways to manufacture circuit boards capable of meeting the challenge and satisfying the demand. As it presently stands, HDI technologies can be segmented into two broad categories: those which rely on sequential building up of layers and plating and those which employ specially constructed materials to make interconnections between layers during the lamination process as illustrated in Figure 1. With that rather extended preamble, we can now examine some of the many different HDI technologies that were explored to meet those needs.

Microvias are arguably the linchpin technology of HDI circuits; however, they are without value if they are not paired with suitable circuit imaging and manufacturing technologies, both of which are required to and capable of making interconnection between them. Circuit formation processes will be discussed later as we turn our attention first to via formation options.

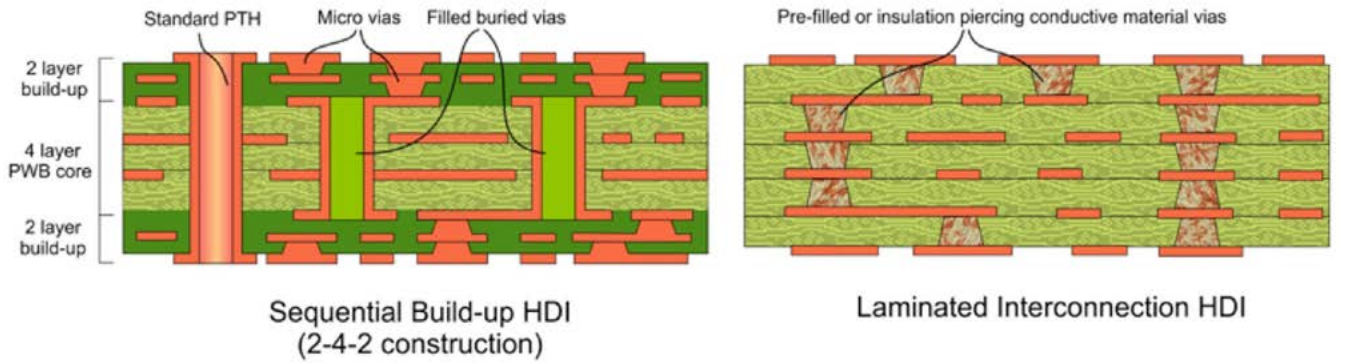


Figure 1: High-density interconnection technology can arguably be divided into two broad categories, that which employs buildup methods to make sequential interconnections between circuit layers and that which employs specialty materials and the lamination process to achieve that same end, as illustrated above.

When tasked with making holes in a substrate, not surprisingly, most technologists default in their thinking to mechanical drilling because it is one of the oldest methods used in industry. Punching or chiseling holes in material can be done with very simple tools and is arguably the oldest in human history when it comes to hole making. That aside, mechanical drilling, while it is extremely versatile, it is also limited in terms of its productivity potential compared to some of today's more advanced methods such as laser drilling. Presently, laser drilling technologies dominate the manufacturing scene when it comes to making microvias for high-density circuit boards. Among the lasers' advantages is their ability to produce extremely small holes (less than 50 µm) with precision and do so at high speed. Mechanical drilling is no match. Moreover with lasers there is no concern about drill wear or drill breakage. There is typically a cleanup step required to assure reliable interconnection to the copper lands which the via serves, however the same can be said for mechanical drilled holes.

Circling back, it is worth noting that punching remains a viable technology and can be quite useful with certain types of high-density substrate constructions such as those used in the manufacture of integrated circuit packages, especially in roll-to-roll format. Tools can be specially developed having multiple punch pins in a predetermined pattern allowing the manufacturer to punch tens or even hundreds of holes per second. Punches have been used with a great deal of success with flexible substrates with hole diameters ranging from 50 µm up to 200 mm and punching rates of up to 1800 holes per minute. Moreover, punched features can be round, oblong, square or rectangular. Current generation equipment can service areas from 150 mm up to 600 mm, making it potentially useful for applications within rigid laminates.

Tools can be specially developed having multiple punch pins in a predetermined pattern allowing the manufacturer to punch tens or even hundreds of holes per second. Punches have been used with a great deal of success with flexible substrates with hole diameters ranging from 50 µm up to 200 mm and punching rates of up to 1800 holes per minute.

Other interesting and less common ways of creating high-density microvias include photo forming and embossing. Photo forming is in many ways indistinguishable from solder mask technology and offers potential for extreme productivity that can be unmatched even by lasers because it is based on exposure and development. Thus it is possible to make either one hole or a million holes in in a simple exposure and development step. This method received a fair amount of attention early on in HDI development; however, the lack of adequate peel strength to support surface mounted components relegated the technology to the shelf. That said, photo-imaging-based hole forming technologies appear to have attractive potential in the manufacture of wholly embedded component circuit assemblies such as have been described for Occam/SAFE structures because such assemblies do not require circuits or circuit features to support component weight. Instead, components rest on a carrier plate such as a piece of aluminum and interconnections are made directly to component terminations using microvias and plating. Thus, instead of putting components on a circuit board, circuits are built up onto component board. Because termination pads are not required layer counts can be reduced. This is illustrated in Figure 2.

Embossing technology is another promising option for making microvias en masse; moreover, as has been pointed out in a recent article, it is possible to make both the via and the circuit path in a single step. The method requires the creation of a circuit master which can be manufactured using a chemical milling process to form raised circuit and hole features of different elevations on a planar metal embossing tool. The technology is similar to that which has been used for nearly a century to make long playing recordings from a master disk.

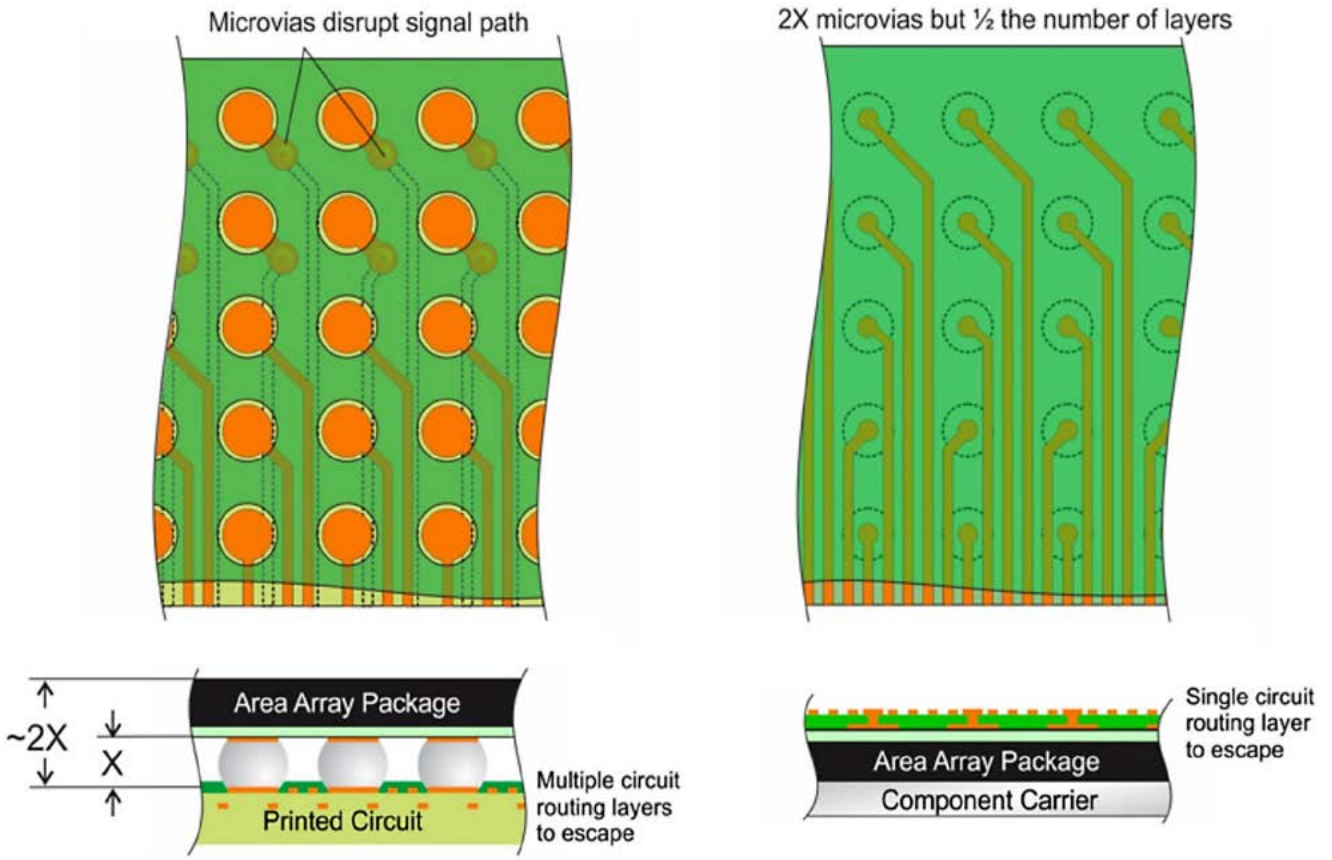


Figure 2: Microvias perform a vital role in high density interconnection allowing the designer to interconnect to terminations several rows deep on area array package devices (left). However, if the designer chooses to, it is possible to reduce layer count by building up circuits on components using high-density interconnection technologies rather than attaching components to circuit boards. The technique has the added advantage of allowing the designer to more effectively address potential thermal problems at the beginning of the design process rather than at the end. This is because no high-temp assembly process is required, allowing components to be placed on a thermal spreading material with their terminations facing away from the carrier (right).

Yet another method for making high-density interconnections, which was developed in Japan, is buried bump interconnection technology (BBIT) and actually bypasses the via hole formation step entirely. The method involves the formation of raised conductive features on a metallic sheet. The conductive features can be formed by multipass stenciling of a polymer filled with a conductive material to create can-like features which can pierce the insulation layers used to laminate one circuit layer to another. This general type of high-density interconnection structure is illustrated in Figure 1.

Circuit lines and spaces are the other important factors required to complete the high-density interconnection equation. As mentioned earlier, lines and spaces have been on the steady downward trend since the earliest days of circuit manufacturing. Efforts to reduce circuit features sizes actually predate the arrival of surface mount technology as manufacturers were compelled to make circuits that would fit between the lands of the through-hole devices they served. This actually has remained a major manufacturing challenge for printed circuit purveyors ever since, and with the ever-increasing interest in higher pin count, finer-pitch IC

components, it is unlikely to abate.

There are two basic challenges that face circuit designers in that regard. First, is to route as many circuits as possible between pads on any given pitch and the second is to assure that those circuit features are as precise as possible. With ever-increasing onboard circuit operating frequencies, tolerance for small imperfections in circuit features is in very short supply if not nonexistent. Small nicks or protrusions on circuit features in the 50 µm range can have deleterious effect on overall circuit performance so control of the manufacturing process for such features is of the utmost importance. While we will review in brief form and graphically the many different ways one can produce circuits, this writer must humbly defer to the myriad technical articles and commentaries written by Dr. Karl Dietz over the last two decades, in this magazine and many others on detailed ways to achieve precise circuit features by control of imaging, plating and etching processes.

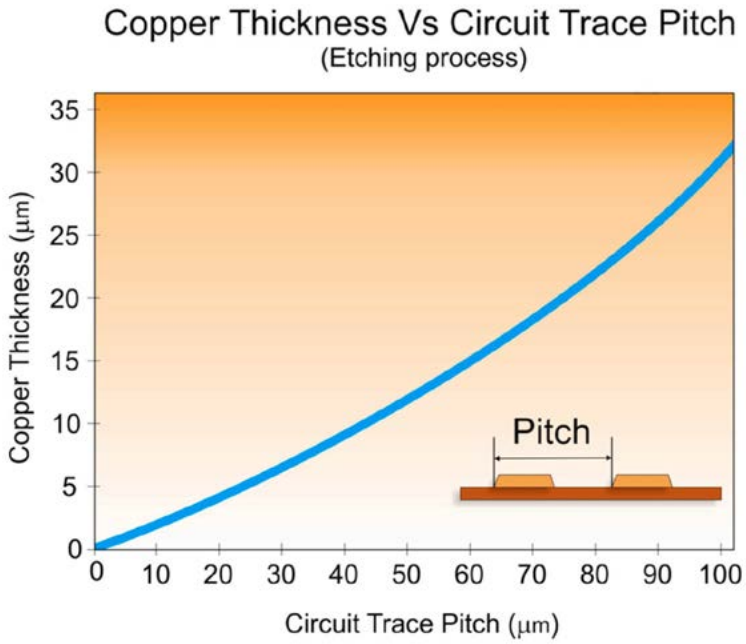


Figure 3: Because etching is an isotropic process wherein chemical solutions attack the target patterned metal both vertically and laterally, orthogonally shaped traces are not possible to achieve and trapezoid shaped circuit cross-sections are generally the norm. Extremely thin copper can produce very fine circuit features that are for all purposes and intentions square-walled; however, they are of little practical use for most applications.

Just as there are many ways of creating microvias, there are also many ways of creating circuit features. In general, circuit feature manufacturing methods can be broken into two main branches, subtractive and additive. There is as well somewhat of a gray area between the two, wherein semi-subtractive and semi-additive methods reside. When it comes to circuit resolution using subtractive technology there is a well-defined correlation between copper thickness and the feature sizes that can be resolved assuming that the copper is uniform and that the imaging and etching processes are in control, operating efficiently and with precision. Figure 3 illustrates the relationship between copper thickness and trace width for subtractive technology using etching. In contrast, additive technologies have proven themselves capable of producing far finer features as evidenced by the nanometer size features currently being produced in copper in the manufacture of integrated circuits. Significant strides have been made over the last couple of decades to vastly improve copper plating technologies allowing manufacturers to reliably plate into resist defined channels while simultaneously filling the tiny micro-vias required to interconnect them from layer to layer.

As previously mentioned in the discussion of microvias above, embossing or imprint patterning of circuit patterns into polymer materials by injection molding or heat stamping provides precise and highly repeatable recessed features which can be subsequently plated into or filled with conductive material.

Figure 4 provides a greatly abbreviated synopsis of circuit manufacturing processes that have been used to a greater or lesser extent over the course of circuit manufacturing history. All of the methods illustrated offer potential value to the designer, manufacturer and user depending on the end application. For high-density interconnection circuits, however, semi-additive processes are generally best suited to the task.

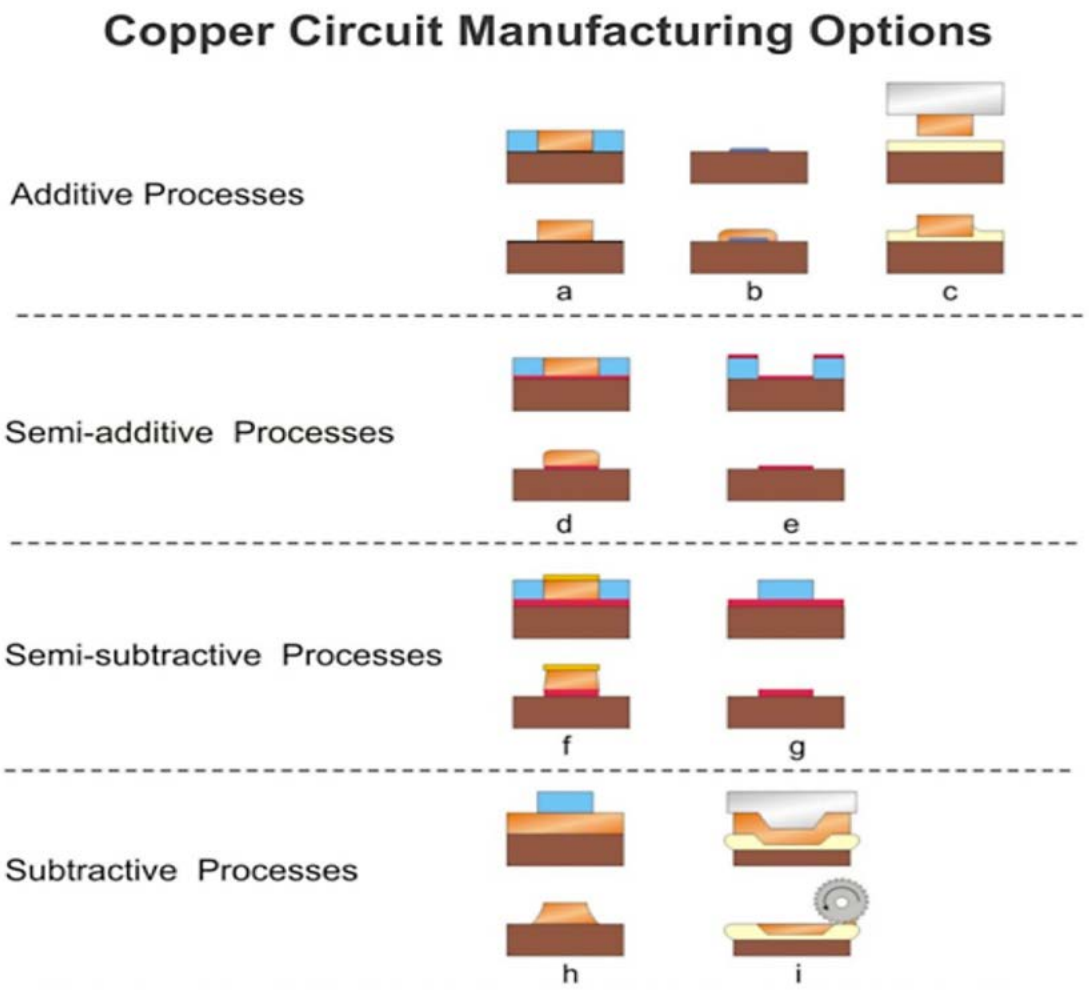


Figure 4: Examples of various processing methods for single conductor layer circuits. a) imaged catalytic substrate electrolessly plated with copper; b) printed catalytic circuit pattern electrolessly plated with copper; c) transfer laminated circuit patterns; d) pattern plated and differentially etched circuit; e) sputtering with circuit pattern formed using lift off resist process; f) thin copper pattern plated with permanent or temporary metal etch resist; g) print and etch circuit with thin copper; h) print and etch with thick copper; i) embossed copper-clad circuit finished with a fly cutter (this method can be used with imprinted and plated versions as well). Note: The red layers are thin conductive films that can be produced by any one of several different methods and of many different metals, though copper is most common.

In summary, high-density interconnection technologies perform a vital service to the broader electronics interconnection industry by providing a platform that can reliably support the interconnection needs of today's highly integrated and component-dense electronic assemblies. As has been illustrated, there are myriad ways to provide those high-density interconnections, and which one is best for any particular application will depend on the application's technical needs. **PCB**

Verdant Electronics Founder and President Joseph (Joe) Fjelstad is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies. Fjelstad has more than 250 U.S. and international patents issued or pending and is the author of Flexible Circuit Technology.

Most-Read Flex007 News Highlights This Month

Super Thin Flex in Headphone Teardown
This week, flex designer Tom Woznicki tears down a set of high-end audio headphones to reveal the flexible circuitry inside. "This flex is as delicate as a wisp of smoke," says Woznicki. This etched flex is the creation of Q Flex.

All Flex Acquires Part of TRI-C Design
All Flex, a manufacturer of flexible circuits and heaters, has purchased the CAD and panelization portion of TRI-C Design Inc. TRI-C provides computer aided-design, panelization, and automation for flexible and PCB manufacturers. This service group performs the precision work of design and setup for new parts manufactured at All Flex.

MFLEX Reports Record Revenues in Fiscal 1Q13
Reza Meshgin, CEO, commented, "We generated record revenues during the first quarter reflecting strong demand from both our existing and new customers. Sales to new customers more than doubled sequentially."

Meiko, Schweizer Team Up for PCB Production in Vietnam
Both companies will build a common production line for production of PCBs dedicated to European customers in the automotive and industry segments. The facility will produce standard PCBs, as well as solutions to reduce the overall cost of a system, such as FR-4, flex, and power electronics solutions, including the inlay board.

Global FPCB Market Rises 15.2% in 2012
2012 is a bumper year for FPCB manufacturers, since FPCB is used in almost all popular electronic products, especially tablet PC and smartphones, which have strongly promoted the FPCB market. The global FPCB market scale reached $10,680M in 2012, an increase of 15.2% compared with 2011.

The Future is Bendable, Stretchable
The future of electronics is bendable and stretchable. Moving beyond traditional consumer electronics such as mobile devices, laptops and tablets, stretchable electronics are also poised to change the biomedical, wearable, portable, and implantable device application fields.

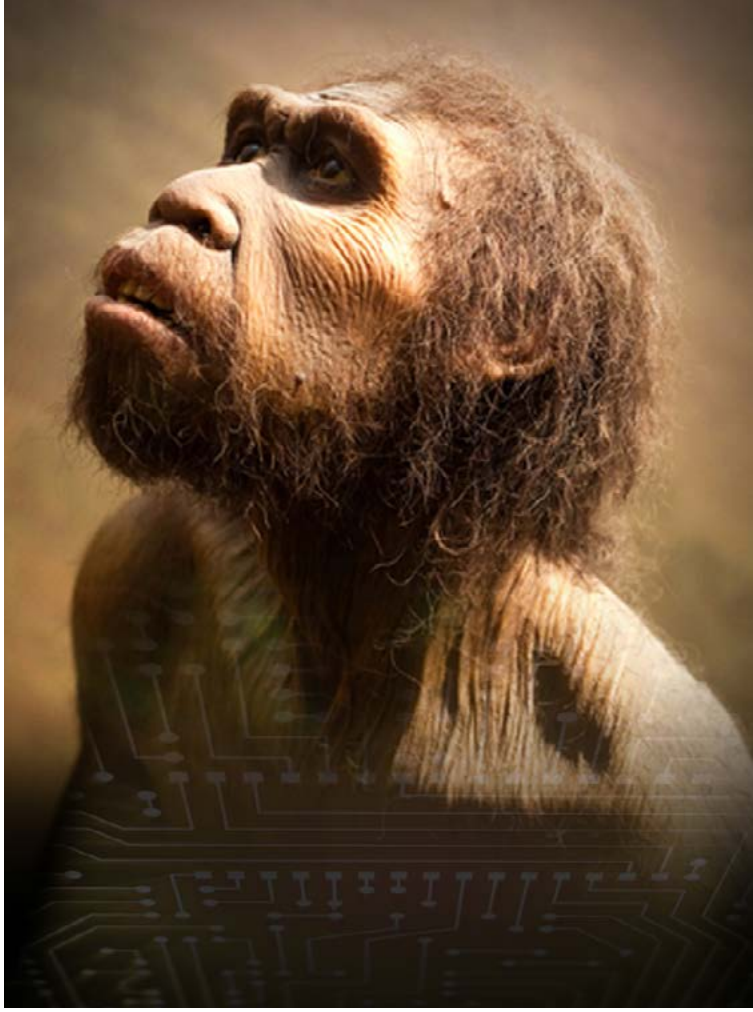
FlexTech Alliance Partners with 4D Technology
FlexTech Alliance is awarding 4D Technology of Tucson, Arizona, a contract to develop an optical system capable of high-resolution mapping of surface topography and defects on a moving, flexible web. Funding development of the in situ metrology system addresses a current shortcoming in roll-to-roll (R2R) electronics manufacturing and will enable new, real time levels of process control and yield enhancement.

Cirexx Enhances Production Capabilities
Flex and rigid-flex printed circuits maker Cirexx International Inc. has enhanced its production capabilities by acquiring an ATG A5 Neo flying probe test system for their rapidly growing fabrication division. The A5 Neo has eight high-speed test heads (four top, four bottom) equipped with four cameras for extremely fast and intelligent board scanning.

PCB Solutions Delivers Complex Flex Circuits to Intel
"This project came to us with open arms," said Greg Engstrom, president of PCB Solutions. "We have been hoping for a project like this to showcase our proficiency and organization with complex flex circuit fabrication and assembly for a while now. This project was the perfect opportunity to prove our processes for a large, multinational corporation."

Power Sources for Flexible, Stretchable Electronics
Electronic devices become smaller, lighter, faster, and more powerful with each passing year. Currently, however, electronics such as cell phones, tablets, laptops, etc., are rigid. But what if they could be made bendable or stretchy?

Evolving HDI Beyond Microvias



by James W. Fuller, Jr.
ENDICOTT INTERCONNECT TECHNOLOGIES

SUMMARY: The advent of HDI through the use of microvias was a critical development in extending the utility of copper interconnect systems. Evolving HDI beyond microvias will be equally important in continuing this extension.

As the electronics industry continues to move forward in providing increasingly greater interconnect capability, a few basic truths continue to be reinforced. The first is that future interconnect schemes will more greatly depend upon optical interconnect in order to make the breakthrough performance metrics that will be required. The second is that the electronic interconnect industry will strive to utilize the existing copper-based infrastructure for as long as possible, delaying the inevitable large-scale investment in optical interconnect. Indeed, we are already seeing the continued proliferation of optically-based systems, but these tend to be at the ultra-high end of the performance scale. The overwhelming majority of system development continues to depend upon copper-based interconnect schemes and continued evolution of these copper structures. The advent of high-density interconnect (HDI) through the use of microvias was a critical development in extending the utility of copper interconnect systems. Evolving HDI beyond microvias will be equally important in continuing this extension.

Throughout the lifespan of electronics, the world has been almost singularly focused on Moore's Law as the directional beacon for how performance improvements would be measured. Semiconductor speed and capability has been the focus for decades, as a result of both the massive capital costs required to build and maintain a semiconductor fab and the equally intimidating intellectual property barrier. Many other areas of the electronics food chain have seen more evolutionary progress. This includes advances in processes and equipment for printed wiring board (PWB) fabrication, PWB assembly, flex circuit and substrate fabrication, and module assembly. As a result, semiconductor capability has outpaced interconnect capability, leaving a performance gap that will need to be addressed before these become the gating performance factors in new systems.

The evolutionary advancement of the PWB has been most recently slowed by massive industry consolidation and the continual financial pressure that has left, by many accounts, only a few hundred PWB fabrication shops in the U.S., a tenfold decrease over the past 10-12 years. This dynamic leads investment to be more reactive than proactive. When this is coupled with the continuing steady loss of PWB design and fab expertise at the end customer, and the overall reduction in operating technical talent, the need for a breakthrough technology is even more crucial.

Historically, the PWB industry has always responded with its share of significant technological progression. The migration from through-hole to SMT, shrinking BGA pitches, smaller via diameters and higher aspect ratios, as well as very unique structures incorporating subcomposites, ledges, back drilling and mixed materials, have all enabled the organic portion of the interconnect supply chain to remain relevant. Included in this technical progression are buried and blind microvias. Although laser blind vias and mechanical microvias have been in use since the early 1980s, the explosion of microvias really took hold in the mid-1990s. One of the more well-known methods involved the use of photo-imaged microvias in a process known as surface laminar circuitry (SLC), most often credited to IBM's Yasu facility for use in the ThinkPad series of laptops. Material and process improvements continued, and eventually the laser-formed microvia overtook the photo-imaged method. Simultaneously, an explosion in demand, driven by consumer devices, took microvia manufacturing from an exception to mainstream.

Since that time, microvias have been used in the most creative of manners. Multiple build-up layers in conjunction with subcomposite structures and mixed materials have grown in popularity. Several of these are shown in Figures 1 through 3.

These structures pose a variety of different challenges. Yields will be markedly lower due to the intrinsically finer features coupled with the exponential scrap due to sequential processing. Costs will be higher due to finer drill bits, hit life limitations, plating challenges and the labor associated with the long cycle time sequential process flow. Electrical performance is also suboptimal due to the consumption of precious wiring channels and the presence of stubs, even

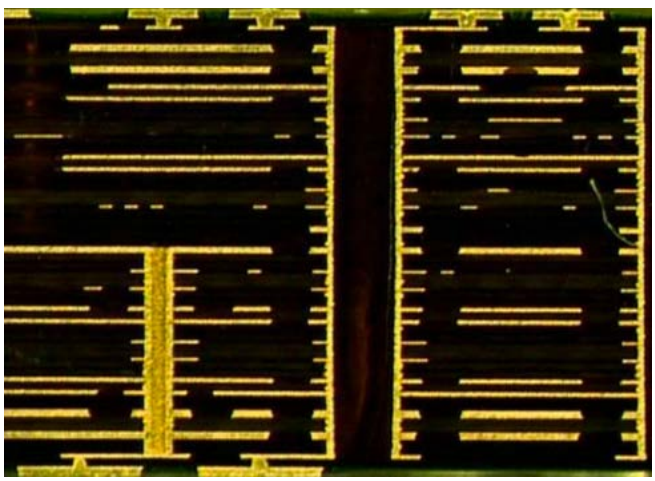


Figure 1: Multilayer PWB with subcomposites and microvias.

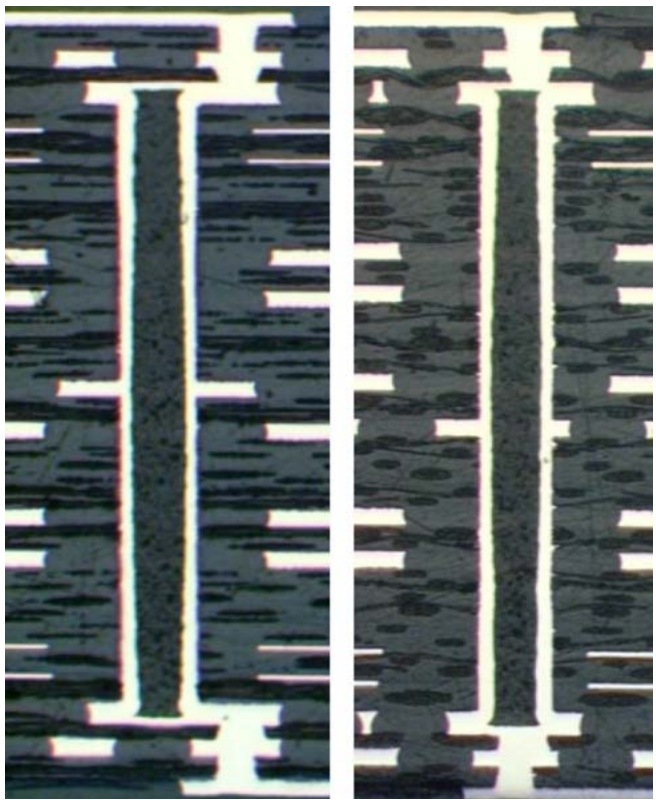


Figure 2: Staggered and unstaggered microvia structures with filled and cap plated PTHs.

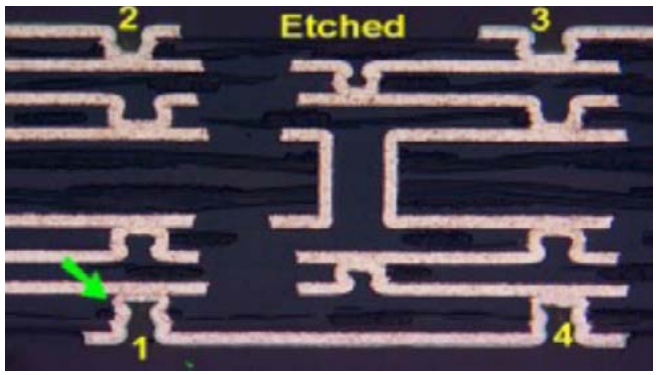


Figure 3: Three-layer buildup panel used as a substrate.

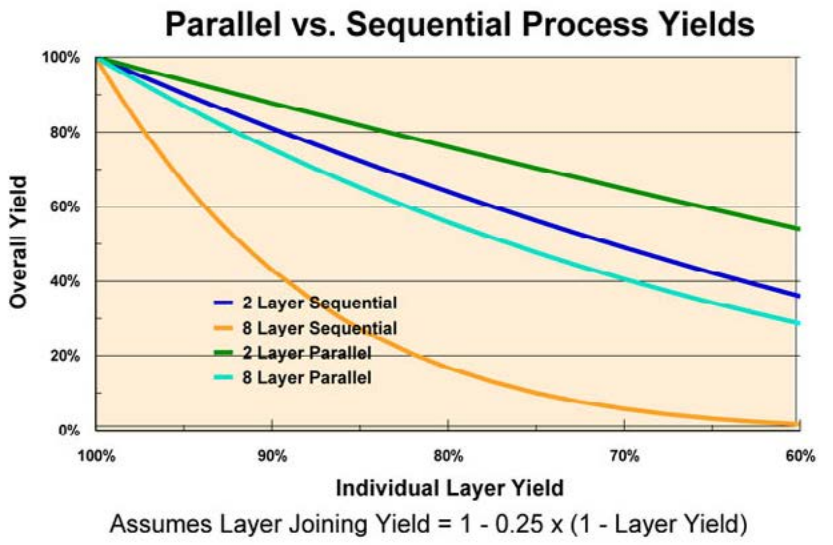


Figure 4: Yield model comparing parallel and sequential process flows.

if the product is back drilled.

What, then, would be the "holy grail" of packaging? It would be based upon a robust set of design rules that provided electrical superiority. It would provide lower cost through improved yields and the reduction of operational costs like labor and materials. It would be highly reliable. Lastly, it would have markedly reduced manufacturing cycle time. The use of Z-interconnect technology can accomplish all of these objectives, and allow HDI to evolve beyond the traditional use of microvias.

The electrical advantages of Z-interconnect have been previously discussed at length[1], and include the total elimination of stubs, increased wiring density, minimized via sizes and reduced cross talk, to name a few. A Z-interconnect structure will always allow for lower layer counts and higher wiring density for equivalent designs due to the significantly increased wiring capability.

In addition to wiring benefits, the Z-axis interconnect/parallel lamination technique explained here affords many manufacturing advantages over traditional sequential build-up processes currently employed in organic packaging. The ability to test and match defect-free subcomposite cores in high layer-count structures results in improved overall yields than can be achieved with buildup technologies (Figure 4). Because each subcomposite core can be built simultaneously, shorter build cycles are also able to be achieved with this process and are somewhat independent of the number of wiring layers required. These advantages allow the Z-interconnect technology to provide a solution to applications with very demanding wiring requirements, not only by reducing feature sizes (vias, lines/spaces) in the X-Y plane, but also by adding more layers without the cumulative yield impact facing traditional sequential processes.

In addition to the wireability, electrical performance and yield advantages that have been described, it should be reinforced that the use of Z-interconnect technology has also allowed the realization of PWB structures that were impossible to build using traditional manufacturing techniques and structures. One example is demonstrated

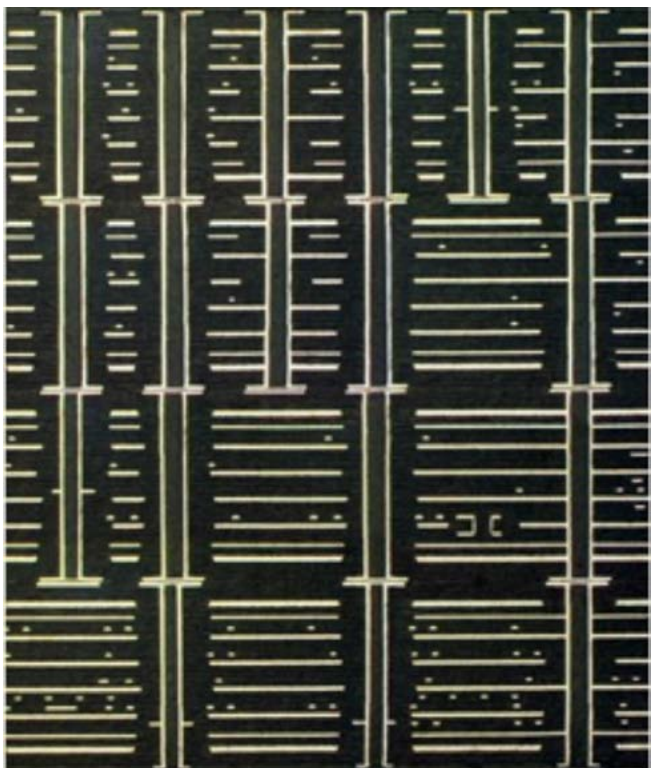


Figure 5: A subcomposite-based 72-layer, Z-interconnect PWB.

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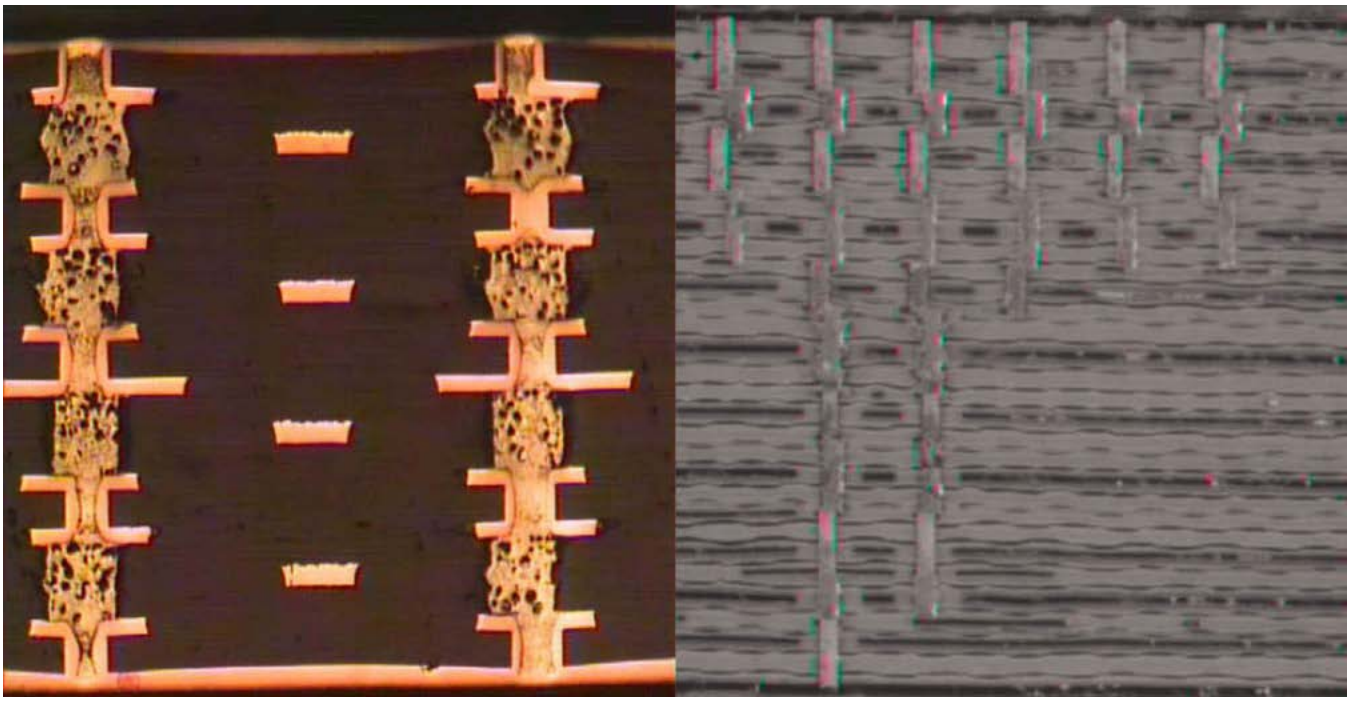

Figure 6: Ultimate Z-interconnect product with a 2s0p or 2s1p building blocks.

in Figure 5. The via diameters that would have been required to build this board resulted in an unmanufacturable aspect ratio. Resizing the vias to a manageable diameter would have consumed a tremendous amount of wiring real estate, forcing the PWB size to grow, resulting in an interconnect system that did not meet the functional requirements. By exploiting the power of Z-interconnect, this board was broken into four subcomposites, smaller via diameters resulted in manufacturable aspect ratios at the subcomposite level, and the PWB structure and performance were satisfied.

While this product utilizes Z-interconnect in a stackup of four subcomposite building blocks, the full power of Z-interconnect can be realized when the smallest possible building block is used. This product, shown in Figure 6, would utilize a 2s0p or 2s1p structure replicated throughout the entire package. Highly parallel processing would minimize cycle time and maximize yields. Manufacturing efficiency would increase dramatically due to the consistent nature of every product: They all use the same building block, with an identical process flow.

In summary, Z-interconnect product provides the highest level of interconnect flexibility and density of any packaging technology, with outstanding electrical characteristics while allowing for superior manufacturability due to higher yields and reduced cycle time. All of this is accomplished while offering highly reliable structures as evidence by successful thermal cycle testing. It is an HDI structure in the truest sense of the word that drives PWB evolution beyond the singular use of microvias, making what is likely the last step before the broad usage of optical interconnect. **PCB**

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1. R. Das, F. Egitto, V. Markovich, J. Fuller, "Z-Axis Interconnection in Organic Packaging," The PCB Magazine, June 2012.

Jim Fuller is currently vice president and general manager of fabrication for Endicott Interconnect Technologies, Inc. He may be contacted at jfuller@eitny.com.

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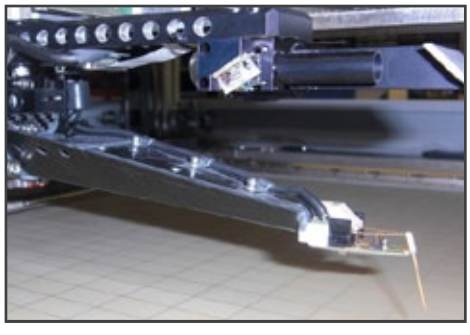

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FEATURE

Understanding Via Effects

by Dr. Zhen Mu
MENTOR GRAPHICS

SUMMARY: The old beliefs about ignoring discontinuity effects from vias on a signal path or using a simple model to estimate the effects are no longer acceptable. Designers need to understand the contributions from different parts of a via and the severity of their impact on signal quality.

As the demand for fast computation and information transmission has increased dramatically in recent years, many designs have boards carrying signals operating at multiple Gbps range in majority; advanced memory designs are targeting over 10Gbps data rates while SERDES standard is moving toward 25-28Gbps. With signal speed changes come the new challenges of solving design issues never seen before. The components of signal path on boards, interconnects, present problems, such as significant dielectric loss, or impedance discontinuity from non-trace portion, that used to be ignored at lower signal speed.

For a typical SERDES channel (Figure 1), the discontinuity contribution comes from the vias

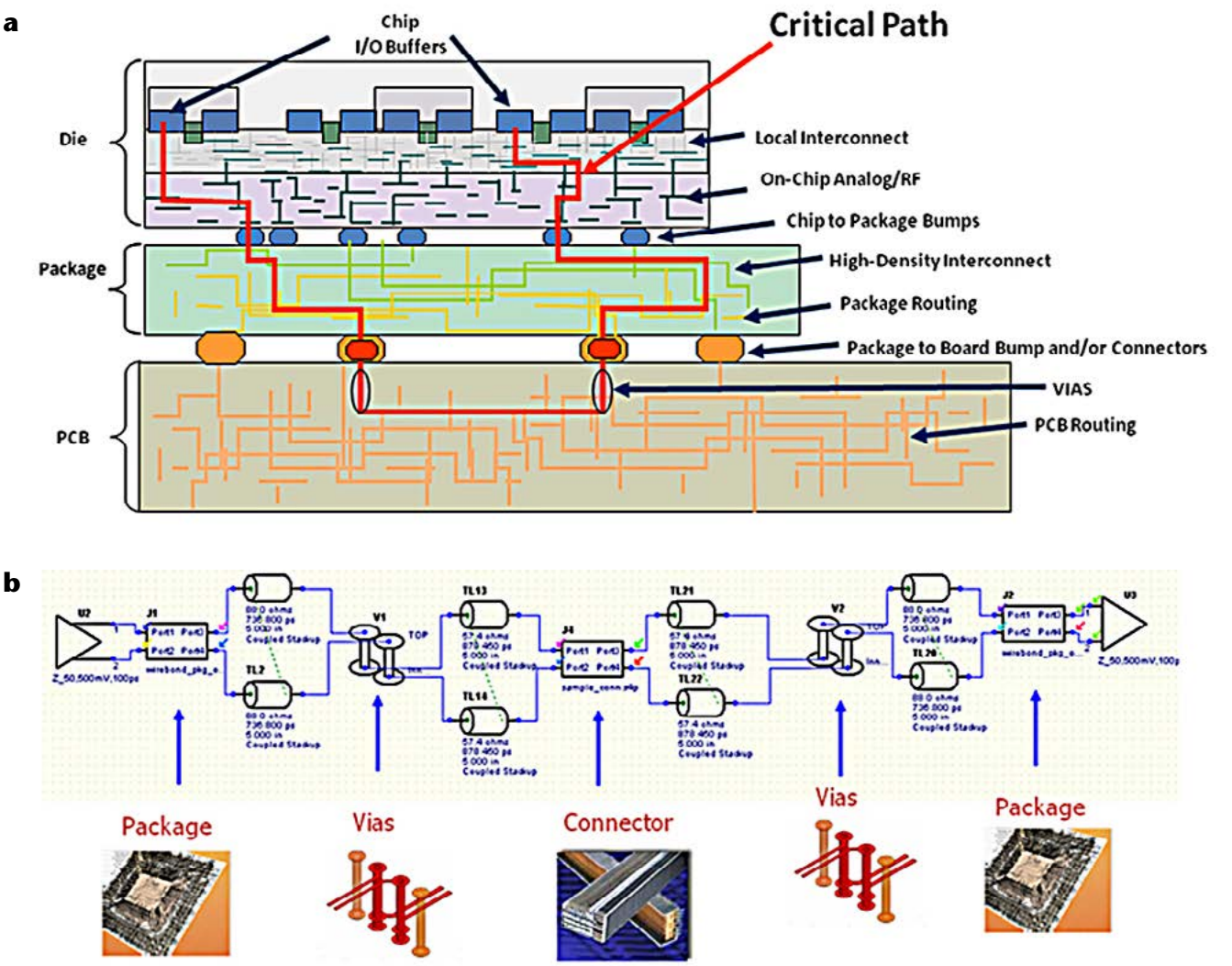

Figure 1: (a) General signal path from chip to chip; (b) Typical channel representation for simulation.

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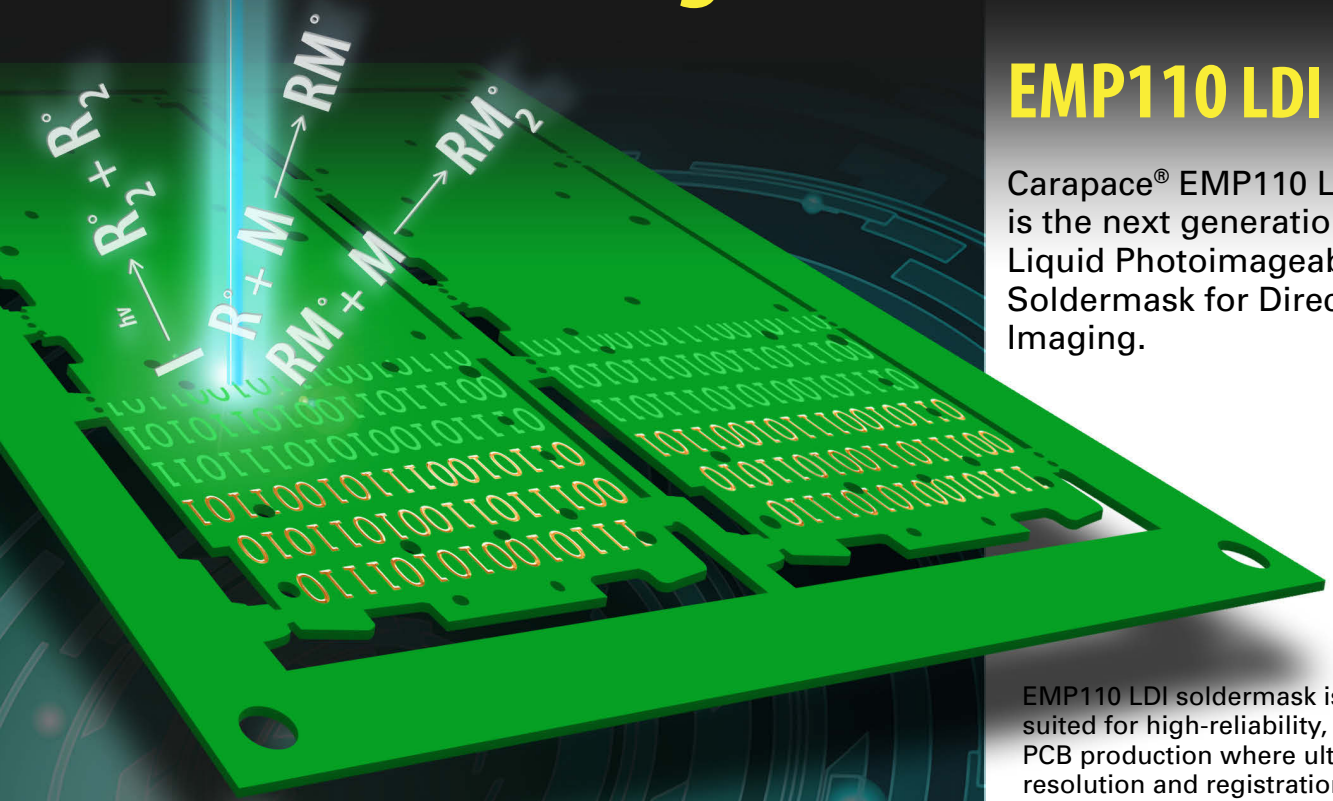

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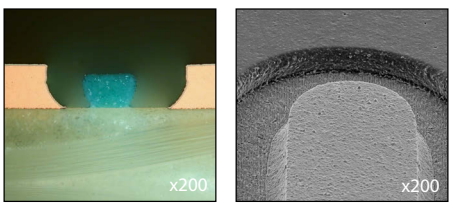

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for a signal's switching layers, connectors enabling multi-board connections, and packages. To PCB designers, only via configurations are under their control in these discontinuity contributors.

Let's take a look at a single via through a standard PCB stackup. When the signal going through the via has lower speed (more precisely, with longer rise/fall times), via effects are not significant at all. However, when we have a faster signal edge rate (rise-fall time is reduced to about 100ps), the via causes noticeable delay and signal degradation (Figure 2). These are the typical discontinuity effects on signal integrity (SI) from a true 3D structure.

For channels analysis, differential vias are used on signal paths. They also cause signal degradation because of how they are configured. The most important part are the via stubs. Long via stubs can interrupt signal transmis-

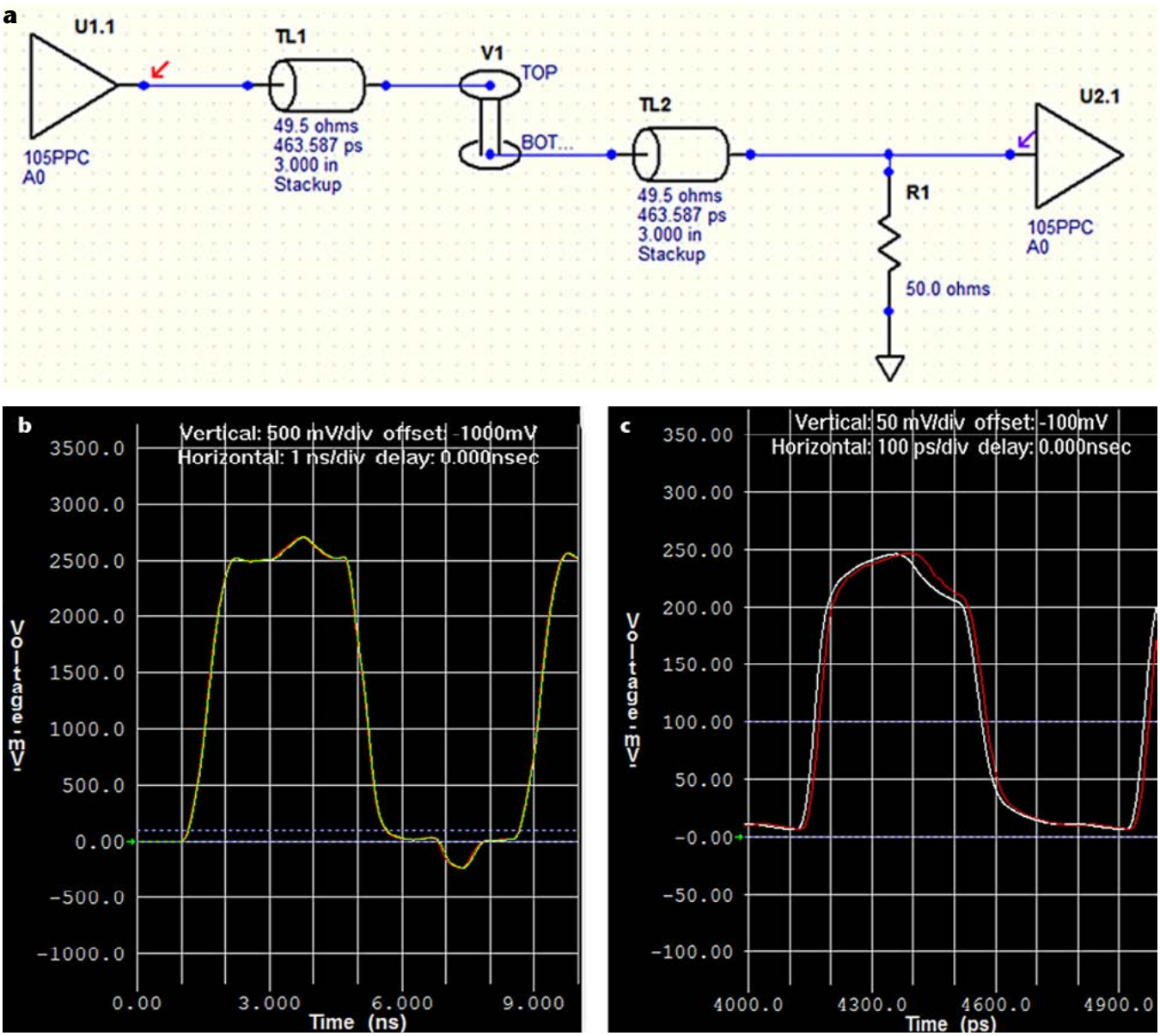


Figure 2: (a) A simple net topology with single signal via; (b) Via effect ignorable with lower signal speed; (c) Via effect cannot be ignored with higher signal speed (data rates of multi-Gbps).

sion completely at certain frequencies. Figure 3 shows a pair of differential vias on a 16-layer board. It compares the S-parameters of the configurations with and without stubs. Clearly, via stubs create unwanted resonance peaks (around 8GHz in this example); at those particular frequencies, signal component of the spectrum cannot be transmitted. Therefore, smaller eye opening in the eye diagram of the case with stubs is observed at receiving end.

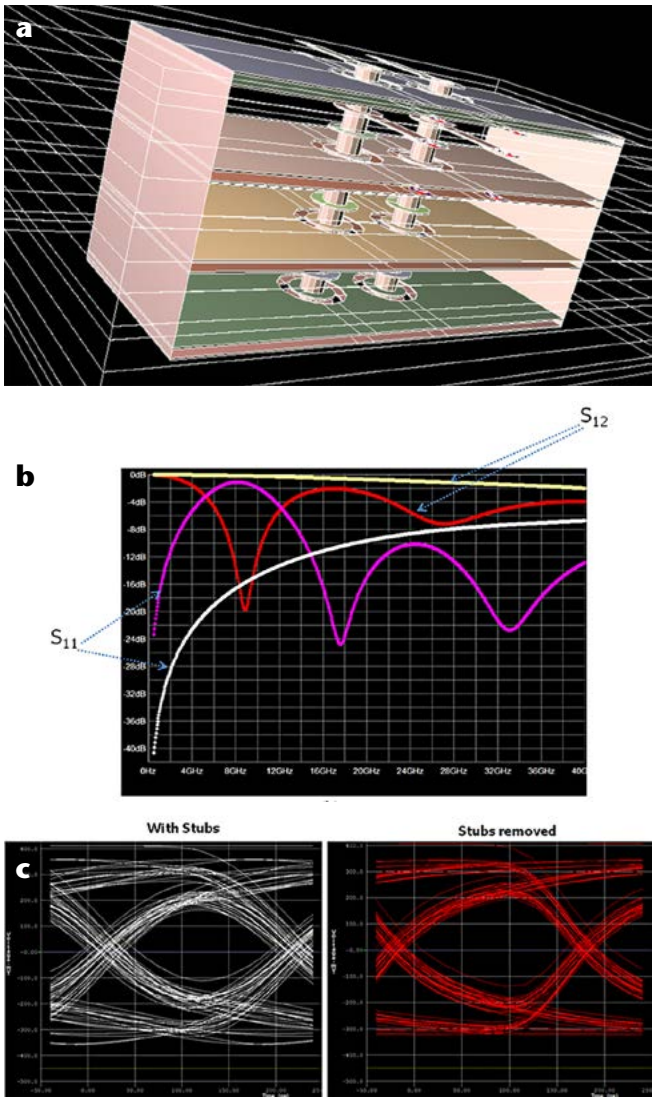


Figure 3: (a) A pair of differential vias with long stubs; (b) Comparing S-parameters with and without via stubs (pink and red: with stubs; yellow and white: stubs removed); (c) Comparing eye diagrams with and without via stubs.

Considering that differential signals on a channel normally have one entering layer and one exiting layer, there would be many via pads left unused. Those pads also can cause SI problems. Figure 4 shows the configuration of a pair of vias going through a board stackup of 26 layers. If a designer leaves all these non-functional pads on, he can get big resonance peak at lower frequency. Removing those pads helps pushing such peaks toward higher-frequency range, therefore benefiting signal transmission. This design method is useful when it is not practical to remove long via stubs through back-drilling techniques.

The via is the means of signal routing changing layers. The return current path a reference plane provides to traces will be interrupted when layer switching occurs. As a result, the trace impedance will be affected. To avoid the reflection caused by the impedance change (or discontinuity) at vias, stitching (or ground) vias are recommended in multi-Gbps designs to keep the current return path for signals. Considering that these extra vias take up precious space on board, designers often need to know when stitching vias are absolutely necessary, and when a design still works without using

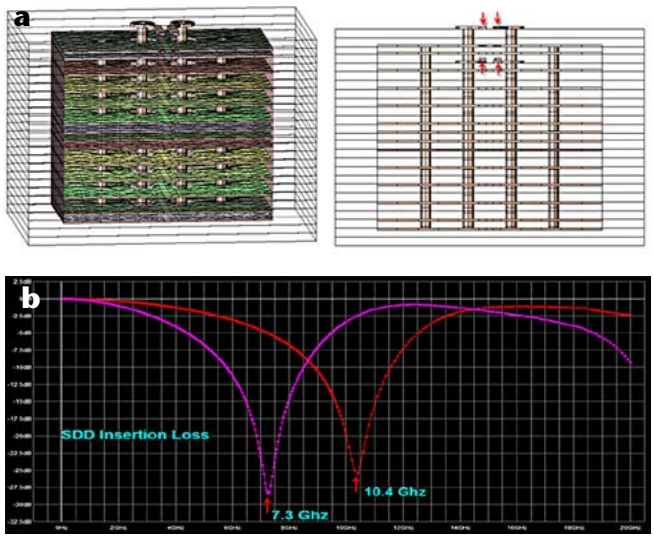


Figure 4: (a) A pair of differential vias with unused pads; (b) Comparing S-parameters with and without un-used pads (pink: with pads; red: unused pads removed).

stitching vias. Simulating and understanding the stitching via effect help make such decisions. Figure 5 shows the results of via configurations with and without stitching vias, and the distance changes from the signal vias. Designers can learn in this case that stitching vias need to be placed closer to the signal vias; if the budget allows a 0.5dB loss from the via discontinuity, they do not need to use stitching vias here.

When the routing space is restricted, designers will also need to know the exact number of stitching vias required. The selection depends on the frequency range designers are interested in. Figure 6 gives another example on effects with different numbers of stitching vias. In this 6-layer design, the number of stitching vias does not matter, up to about 14Ghz; while the difference of insertion loss is 0.3dB at 20GHz between placing four stitching vias and one stitching via around the single via. Again, designers should choose the right number of stitching vias based on noise budget, or the design tolerance.

So far, we have discussed single via (or pair) behavior. Vias can also create coupling noise to signal net through plane cavities if two signal vias go through the same plane pair. Let us ex-

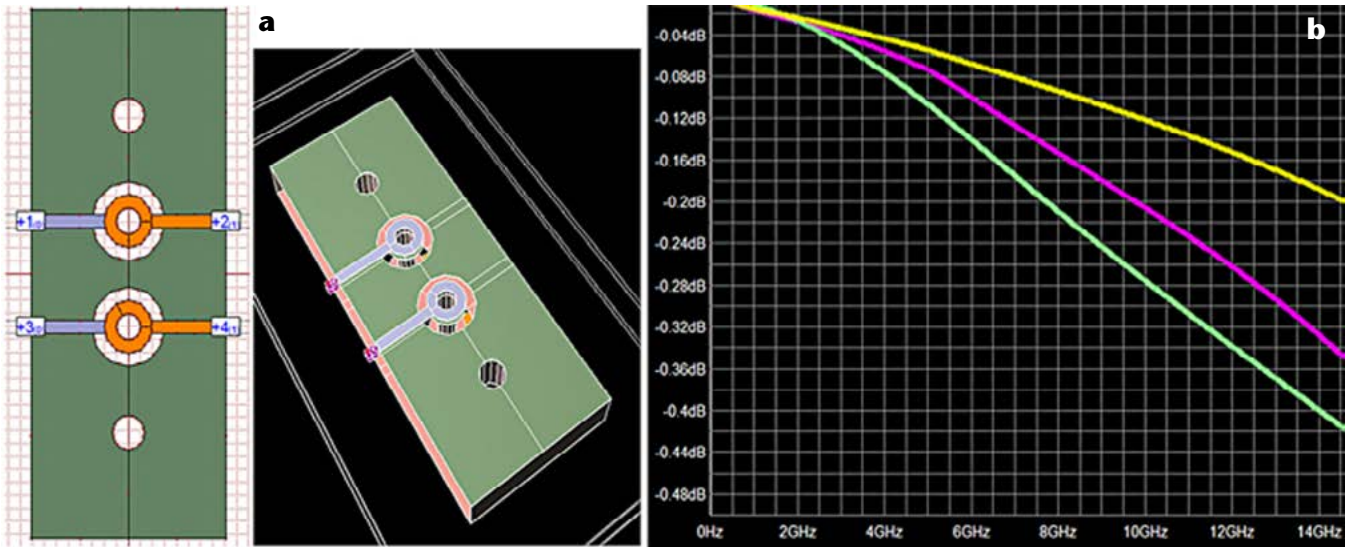


Figure 5: (a) A pair of differential vias with 2 stitching vias; (b) Comparing insertion loss of S-parameters (yellow: with stitching vias closely placed; pink: with stitching vias placed far away green: without stitching vias).

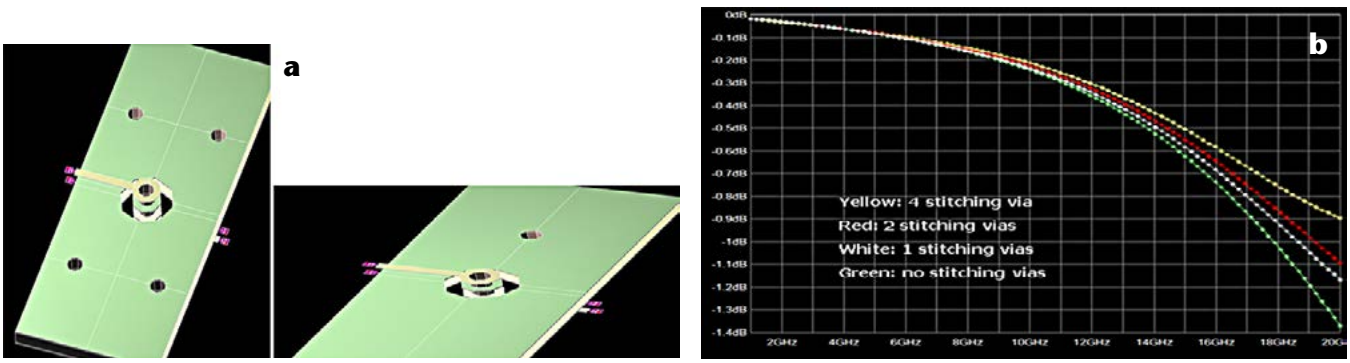
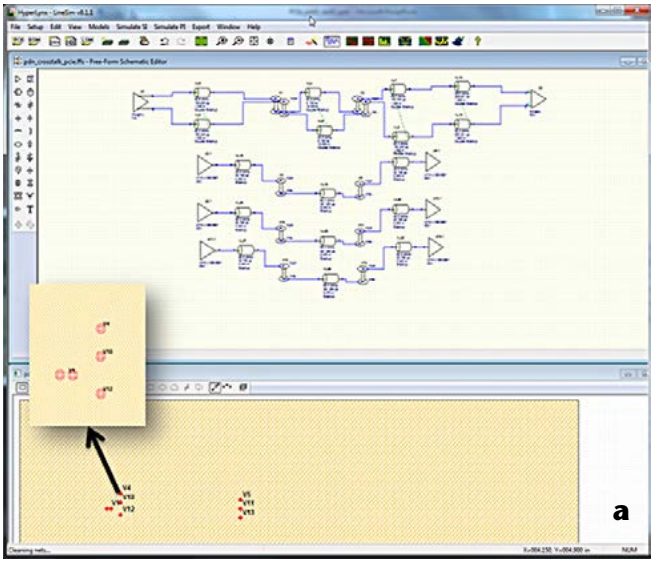
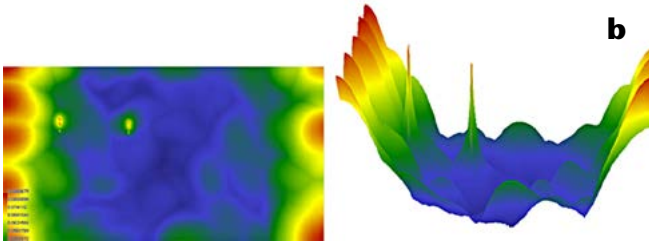


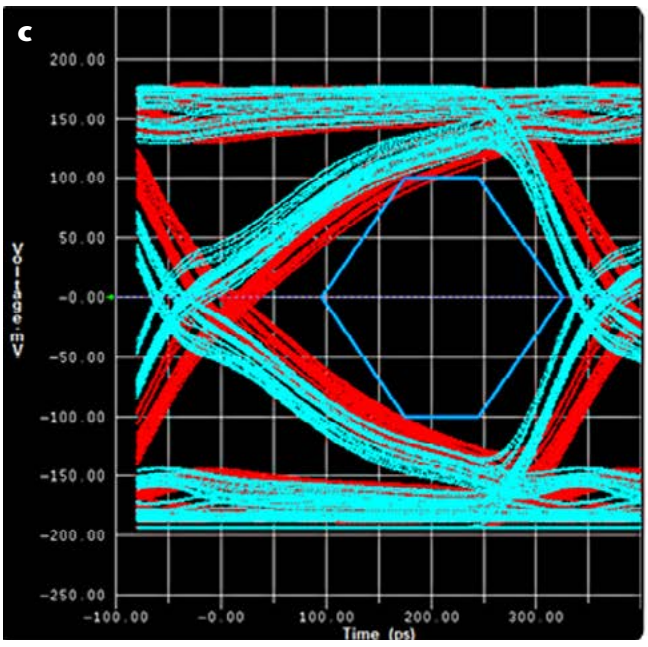
Figure 6: (a) A design example; (b) Comparing insertion loss with different number of stitching vias.

amine the example in Figure 7. The channel under testing carries PCIExpress signal. There are several DDR2 signal routed on the same board. Though the DDR signals are far from the PCIExpress channel (no trace coupling), the vias on both signals pass through the same plane layers. When the DQ net of the DDR bus switches, noise is generated in the plane cavity and travels towards the vias on the PCIExpress channel and is picked up. It then shows in the eye diagram at the receiving end. The eye opening is reduced because of the via coupling noise.

In summary, the discontinuity effects from vias on signal path can cause significant degradation on eye diagrams of a multi-Gbps channel. The old assumption to ignore those effects or to use a simple model estimating the effects is no longer acceptable. Designers need to understand the contributions from different parts of a via and the severity of their impact on signal quality. Then, they can use 3D modeling and analysis functions in an SI tool to determine how a design should be modified. **PCB**







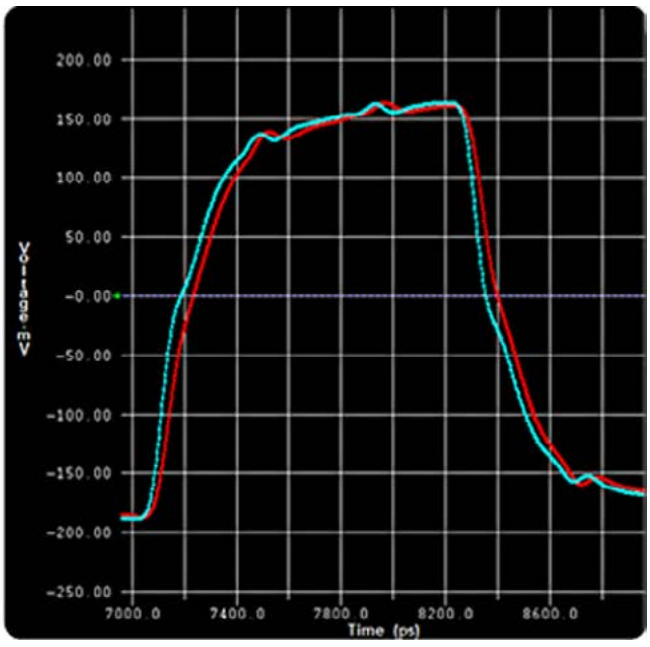


Figure 7: (a) A design example; (b) Plane noise induced by via coupling when DQ signal switches: 86mV; (c) Comparing eye diagrams and time domain waveforms (blue: no via crosstalk; red: with via crosstalk).

Dr. Zhen Mu is a product market manager at Mentor Graphics and responsible for signal integrity and power integrity products for PCB and package analysis.

Metal in the Board: Applying HDI to Digital Power

by Bill Burr and Nick Pearne
BPA CONSULTING

SUMMARY: As detailed in BPA Consulting's just-released report "Metal in the Board," conventional board technologies—from print and etch to HDI—can be recombined using established materials and processes to form innovative structural types capable of meeting the challenges of digital power.

What It's All About

New generations of semiconductors are providing opportunities for expansion of the role of the circuit board beyond mounting and interconnection towards actuation—making things happen. The combination of power and intelligence made possible by the digitalization of power supply, conversion, and control is becoming an enabling factor for an expanding range of new and existing opportunities.

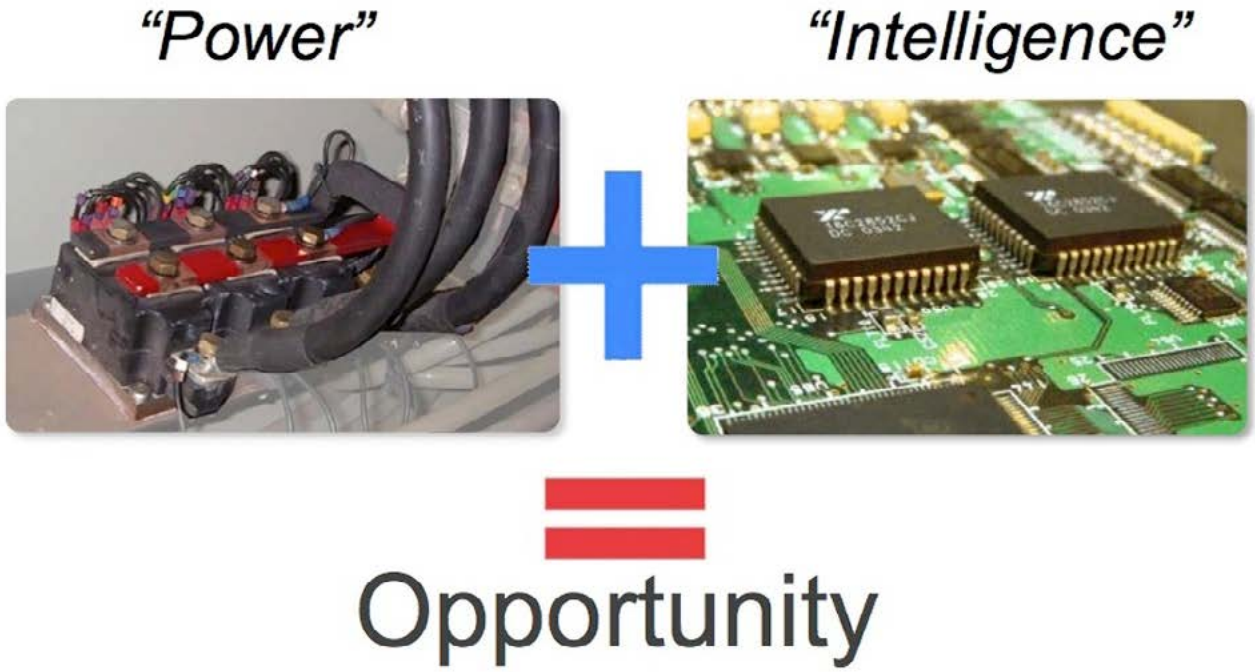


Figure 1: Concept: Andus Electronic.

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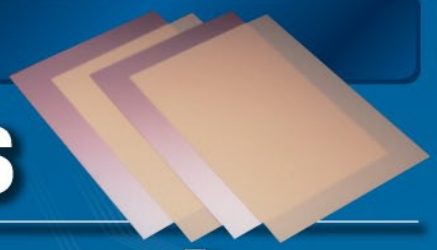

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Semiconductor technology is also driving another entirely new opportunity: solid state lighting. In comparison to incandescent, where a white-hot filament is the source of light, an LED doesn't need to be hot to work. Indeed, the junction temperature needs to be kept below 110˚C while the device dissipates some 80% of input power in the form of heat. The heat (watts) produced is much less than for the incandescent, but nonetheless, the few watts involved have to be extracted from a very small volume of the LED or loss of intensity and premature failure are guaranteed.

In a recent report, "Metal in the Board—Opportunities for Printed Circuit Boards Providing Enhanced Thermal and Power Management, " BPA Consulting provides a unique window on the business of MiB. The report identifies and profiles a number of board level solutions for the management of heat and power, the applications for which these are suitable, and the market opportunities represented by the applications themselves. These solutions employ both conventional and enhanced printed circuit fabrication techniques and materials to create metallic structures in the circuit board, supporting power densities up through 20W/cm2 and currents as high as 1000 amperes in combination with the level of interconnect that is currently available from PCBs—ranging from simple, single-layer circuits up to complex HDI multilayers using low-loss dielectrics.

To simplify the analysis of this important new area, the BPA report divides MiB technologies into 12 types, segregated by the following criteria:

- Thermal management technology—heat pipes, inlays, dissipation planes, etc.
- Current management—copper planes, embedded bus bars, discrete wiring or strips
- Board layup—number of layers, use of internal/external dissipator planes

Performance characteristics are analysed for each in terms of thermal resistance in X-, Y-, and Z-axes and current handling capacity. On the commercial side, the report forecasts the market opportunity for each of these 12 MiB types through 2020. Although forecasting farther out than about two years becomes problematic, BPA's models are "bottom-up," driven by respected industry data sources ranging from the International Energy Agency through the Cisco Visual Networking Index and numerous industry correspondents. The range of inputs has enabled a detailed assessment of end use markets and applications, focusing on opportunities for MiB in automotive, solid state lighting, digital power, RF power, domestic appliances and distributed energy harvesting (primarily solar and wind power systems), subdivided by MiB technology and regional focus.

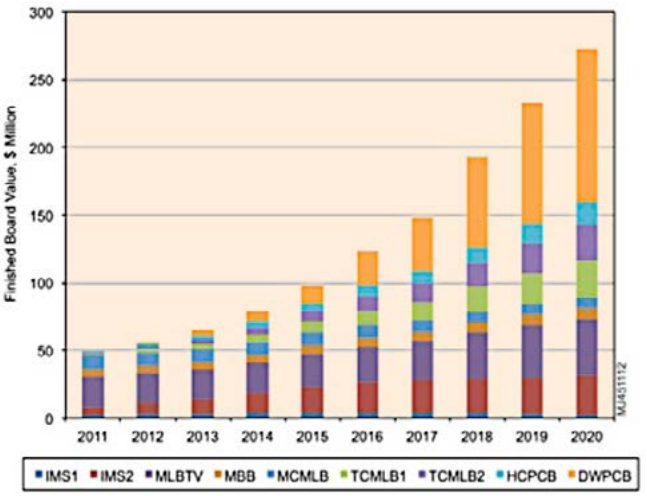

Figure 2: Application growth for MiB types.

HDI—Aligning Heat and Power

HDI, primarily in the form of blind microvias, represents an important component in the MiB toolkit. Although the combination of microvias and high power doesn't seem to fit with the image of heavy cabling and massive heatsinks associated with power management, new generations of power semiconductors are housed in surface mount packages. This means the primary thermal path is now down, into the board, and not up and out to ambient through a heatsink.

All semiconductors generate heat during operation due to resistive losses across the junction at the heart of the device. For example, LEDs may consume less power than incandescent, but only 20% of this power actually

drives the state change, which causes photon emission. The rest turns into heat and must be drawn away from the device to maintain recommended junction temperatures. For surface mounted devices, this means providing a pathway through the substrate.

Getting the Heat Out

The problem is that FR-4 and other dielectrics are not only good electrical insulators—they are also good thermal insulators. The thermal conductivity of FR-4 is about 0.25 W/m-K; that is, 1/4 watt of thermal energy across an area of one square meter will cause a temperature rise of 1°K in the material. In contrast, copper will handle almost 400 watts.

There are three basic modes for heat transfer: conduction, convection, and radiation. All of these are driven by temperature gradients: heat moves from hot to cold, just as electrons move from high potential (voltage) to low potential. The dominant modes for electronics and MiB in particular are:

• ***Conduction***—movement of heat through solids due to atomic excitation and free movement of electrons through metals following Fourier's Law. The rate at which heat is transferred depends on the thermal gradient, the thermal conductivity of the materials involved, the length of the thermal pathway, and the thermal capacity of the cool body that is absorbing the heat. This end of the line is ambient—usually the air surrounding the assembly.

• ***Convection***—transfer of heat between a solid surface and a fluid flowing over this surface due to random molecular motion and bulk motion of a fluid. Depends on the area of the surface and a heat transfer coefficient which quantifies the rate at which heat will pass across the interface.

Radiative effects are negligible at the operating temperatures of electronics, and are usually not considered in thermal modeling.

Fourier's Law describes the transfer rate of thermal energy expressed in watts between two points:

$$(1)\ P_D\ (W) = (k \times A/L) \times (T_1 - T_2)$$

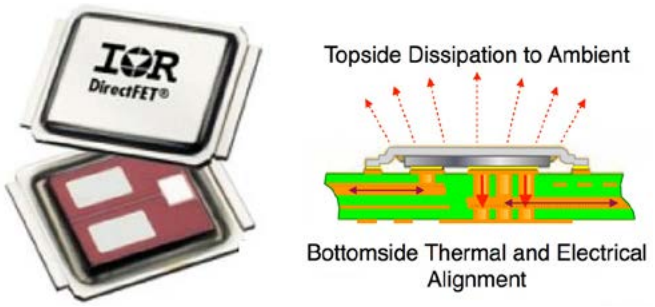

Figure 3: Thermal and electrical alignment—IR DirectFET®.

where:

k: thermal conductivity coefficient (W°C/cm)
A: cross-sectional area perpendicular to heat flux vector (cm^2)
L: length of thermal path (cm)
T_1: temperature of heat source (°C)
T_2: temperature of heat drain (°C)

The concept of thermal resistance provides an alternative to Fourier's Law that is useful during board design because of similarities to Ohm's Law. Rewriting (1):

$$(2)\ P_D = (T_1 - T_2) \div (L/k \times A) = -(1/R_\theta) \times (T_2 - T_1)$$

We can derive the inverse of conductivity, or thermal resistance, where:

$$(3)\ R_\theta = l/(k \times A)$$

in which:

l = length of conductive section in microns
k = thermal conductivity in W/m-K
A = cross sectional area of conductor in mm2

and the obtained result is expressed in terms of temperature rise per watt (°C/W).

This conversion is very useful in board design because thermal resistances can then be calculated in series or in parallel as required by the board structure and thermal pathways. The power dissipation of the device (or devices) is modeled as a current source, the thermal resistances are modeled as resistors in series, and the

ambient temperature is considered as a voltage source. To maximize the useful ambient temperature range for a given power dissipation in watts, the total thermal resistance from junction to ambient must be minimized.

Getting the heat away from the junction means either going down into the board using MiB or spreading the heat out over a wide enough area so that it can pass into the "ambient fluid," usually the air surrounding the assembly. Using the equivalent circuit analytical method for convective transfer, a typical power component dissipating 2 watts with a maximum ambient temperature of 50°C and a junction temperature limit of 125°C would require a copper surface are of about 80cm^2 (12.5 sq in) to stay within defined operational limits. This is clearly not an option in most digital power designs today.

HDI + MiB = Increased Power Density

One of the most cost-effective methods for increasing the bandwidth available for heatsinking SMD devices is to create low thermal resistance pathways into and through the board using MiB techniques. BPA have identified a number of methods to do this, and several use thermal vias, either in combination with internal dissipation planes, backside dissipation planes, or bottomside thermal wells such as heatsinks or chassis elements.

However, while an array of thermal vias within the thermal pad provided on the board layout will increase the Z-axis conductivity from about 0.3 to around 20W/m-K, this also means that the thermal pad will become honeycombed with holes. Unless the vias are very small, or filled and/or capped, there is the probability that solder will wick into the hole, leaving voids under the component as shown in Figure 4. This will cause a dramatic increase in thermal resistance between the component case and the board due to the very low thermal conductivity of air (about 0.02 W/m-K).

Another risk factor associated with open vias is process residue entrapment. While solder may not wick down into very small holes, the holes remain open and, when plugged partially by solder, form very high aspect ratio blind vias which are almost impossible to clean unless full immersion in cleaning solution and ultrasonics are used. Even then, cleaning residues may remain in the holes! The common industry practice of tenting using soldermask is also not recommended, as isolated tents formed with LPISM do not offer the same reliability as tents formed in a continuous soldermask layer.

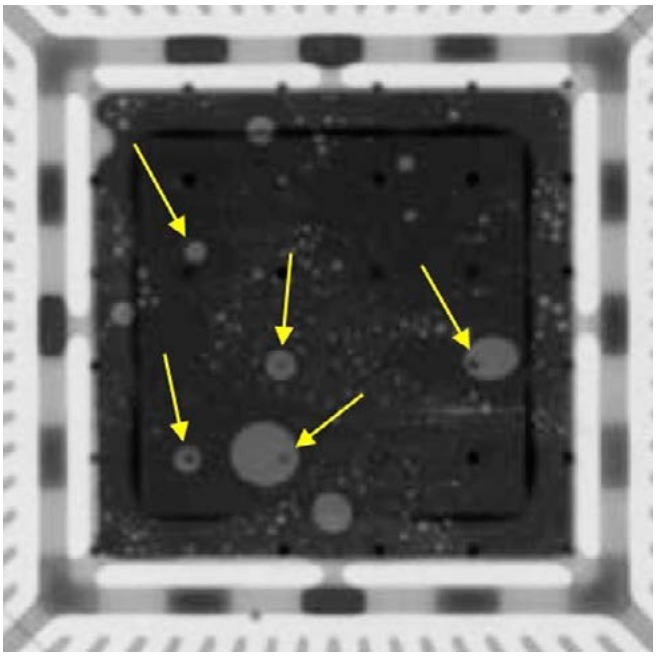

Figure 4: Thermal via voids under QFN package. (source: Indium Corporation)

Although wiring densities typical of digital power may not require HDI, blind via techniques are being increasingly used by technology leaders in this field to get around the problems of open holes in thermal pads.

Häusermann GmbH use both controlled Z-axis drilling and lasers to form blind holes providing thermal pathways to embedded copper profiles in their proprietary HSMtec© process. Although laser vias are typically 100µ in diameter or less, what counts in an MiB application is the length of the conductive element (in this case, depth of the via) and cross-sectional area of copper available as a thermal pathway.

The copper area can be determined by the difference in surface area between the two circles formed by the via-drilled diameter and inside plated diameter, or by multiplying the circumference times the deposited copper thickness.

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Using the first method, the thermal resistance of the array is determined by:

$$(4)\ R_{\theta\ array} = I / k \times (N_{vias} \times \{\pi \times [(D_1/2)^2 - (D_2/2)^2]\})$$

And, since laser microvias are very small and are drilled at effective hit rates well in excess of 10,000 per minute (for CO_2 "copper direct" process), a lot of them can be placed in a thermal pad. An array of 1296 microvias in a 100mm² thermal pad will present a thermal resistance of about 0.01 W/°C: about the same as the solder joint used to bond the device's thermal slug to the pad!

Of course, this very low R_θ pathway isn't much good unless there's somewhere for the heat to go. The HSMtec process provides onward conduction in the form of embedded copper "profiles" which may be used as heat spreaders or as conductive pathways to chassis elements or discrete heatsinks as shown in Figure 6. Alternative embedding techniques such as Wirelaid© as supplied by Schweizer Electronic and others provide similar capabilities, forming what BPA has defined as the DWPCB type: boards incorporating discrete MiB elements which provide enhanced conductivity pathways for heat and power. This approach presents a number of advantages:

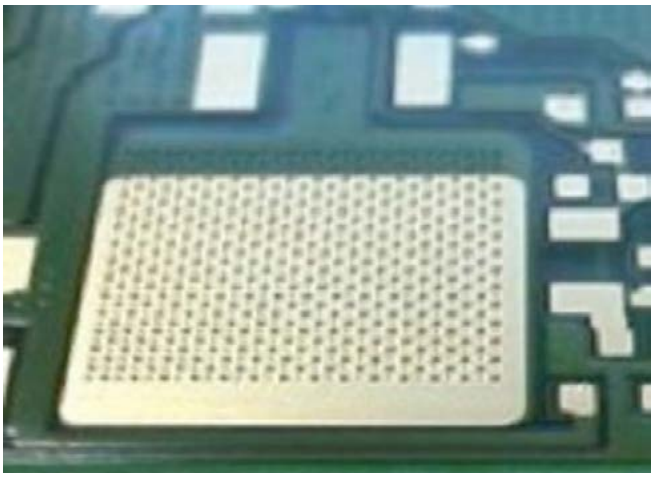

Figure 5: Microthermal via array. (source: Würth Electronics)

- Thermal and current pathways only where needed
- Cost of MiB limited to those nets needing MiB
- 3D capability: form to assemble
- Selective MiB enables wide range of PCB design rules including HDI
- Logic wiring rules are independent of digital power: HDI over embedded bus bars/profiles

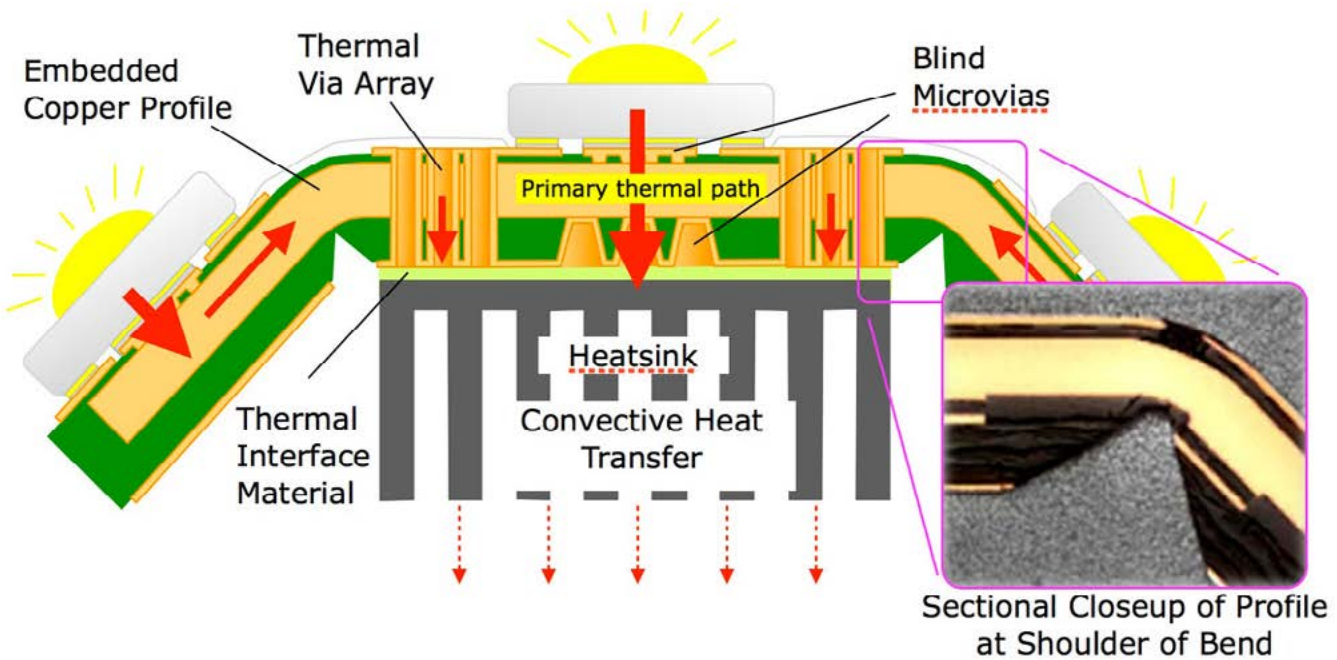

Figure 6: HSMtec substrate for HB LED. (source: Häusermann GmbH)

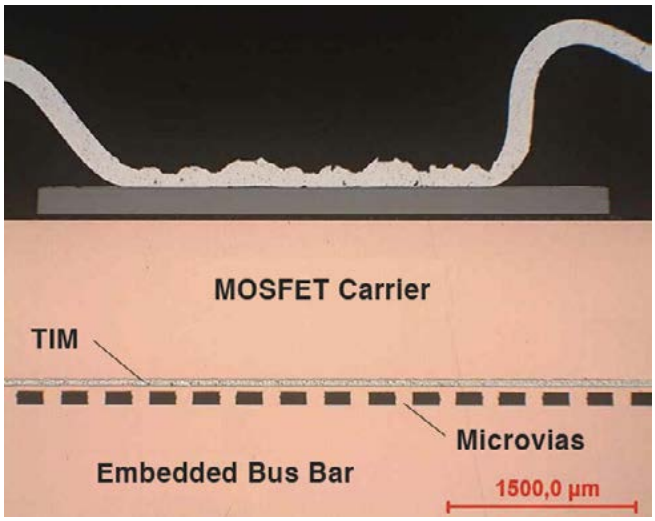

Figure 7: Embedded bus connection using microvias. (source: Andus Electronic)

Making a short connection to a solid block of embedded copper provides not only a low-resistance thermal pathway, but also a low-resistance electrical connection. For high-current applications, microvias are lased to an embedded power bus, and plated using viafill technologies to form solid pillars as shown in Figure 7. Andus Electronic specializes in this type of high-current construction which is generating considerable interest for H/EV automotive applications. As with the thermal array seen earlier, although the vias are very small the current carrying capacity of the array is determined by the depth of the vias and the total cross-sectional copper area. Therefore, an assessment as to whether the vias should be filled or not can be made based on the anticipated current load and the copper cross-section available to carry it. This determination can be based on either the calculated resistivity of the via array or a conductor cross-section equivalent from the IPC-2152 charts. Another very useful source for determining current carrying capacity is Circuitcalculator.com's javascript calculator. Skin effect is not an issue at the switching frequencies typical of digital power, so the bulk cross-sectional area can be used as a basis for calculation.

Embedded Power Devices

Another area covered by BPA's new report within the automotive section is the growing interest in embedding technologies. Although known-good-die issues have dogged embedding approaches for years, the simplicity of MOSFET and IGBT semiconductors make them a promising candidate. Embedding offers a number of advantages:

- Elimination of "junction to case" thermal resistance, because there is no more "case"
- Increase in thermal pathway interface from die bottom/wirebonds to entire die surface
- Decrease in length of thermal pathway to high-k dissipator
- Low inductance
- 3D packaging
- Reliability issues due to wirebond stress fatigue cracks eliminated

The key to this technique is the use of HDI buildup techniques and blind microvias to access bond pads for power semiconductors. This photo from the EU-"Hiding Dies" Project (Fraunhofer IZM, 2012) shows the grey power MOSFET die bonded onto a dissipator plane and accessed by an array of lased blind vias which have been filled by copper plating. The completed package may then be soldered onto a motherboard. Other variations on this stackup provide electrical isolation using high-k prepregs and additional copper layers.

The improved thermal dissipation characteristics of embedding technology have been quantified by Hoffman Electronics in a recent presentation at the EIPC Summer Meeting in Milan. As shown in Figure 9, the hot spots typical of discrete packaged devices on low-k substrates such as FR-4 were significantly reduced when the packages were removed and the devices were embedded in the substrate.

A further level of integration is being demonstrated by the Project Hi-Level Consortium, coordinated by Continental and including a number of top players in the European technology industry. The demonstrator substitutes a 10kW motor controller assembly using die bonded to a DBC substrate with a power PCB incorporating thick copper inlays, embedded MOSFETs, and a surface mounted control mod-

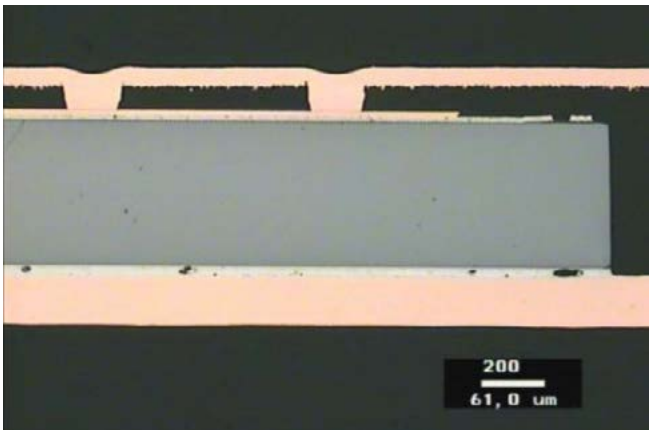

Figure 8: Microvia connection to embedded MOSFET. (source: Fraunhofer IZM)

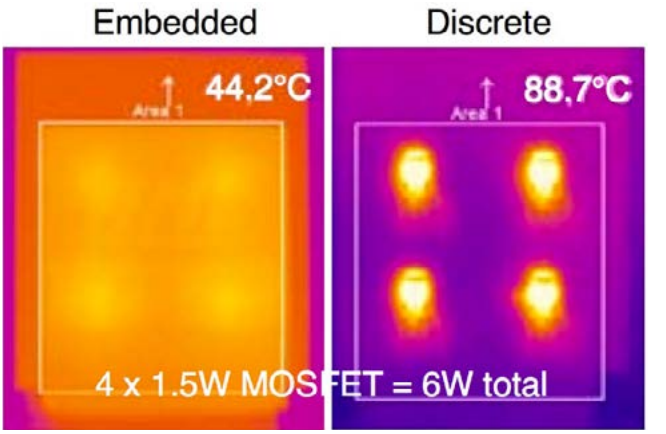

Figure 9: Heat buildup in FR4: Embedded vs. Discrete. (source: Hoffman Electronic)

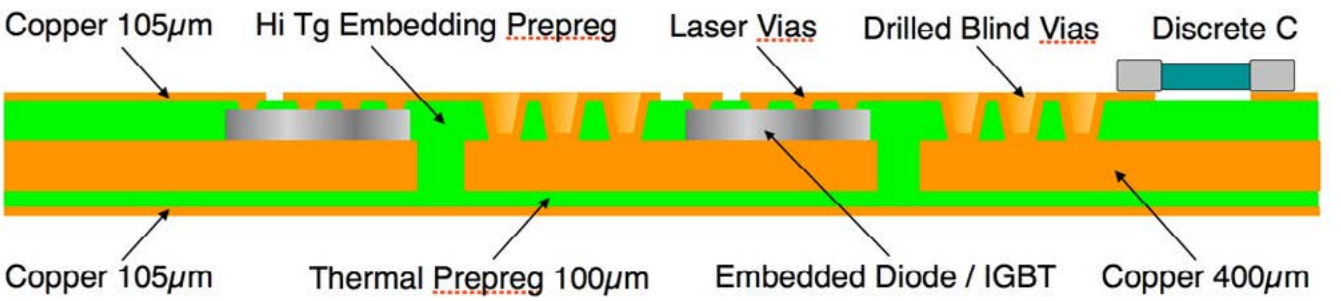

Figure 10: 10kW motor controller concept. (source: Fraunhofer IZM)

ule. As with the earlier examples, DWPCB techniques include HDI buildup processes and microvias for direct wiring to the embedded die.

MiB—Opportunities for Value Recapture

The emergence of surface mount packaging for power devices ranging from MOSFET switches to RF power amplifiers is driving the development of an expanding toolkit for providing enhanced thermal and current management in the board. Conventional board technologies—from print and etch to HDI—can be recombined using established materials and processes to form innovative structural types capable of meeting the challenges of digital power. In the process, this "recombinational" approach offers opportunities for value recapture as outboard power management features become integrated into the board itself. **PCB**

Formerly CTO of one of Europe's top 10 PCB companies and past president of the EIPC, William (Bill) Burr is owner and principal of LPC Ltd, and collaborates with BPA as a senior consultant. He may be contacted at w.burr@bpaconsulting.com.

Nick Pearne is co-founder of BPA, which focuses on microelectronic packaging and interconnections, and the director of several companies primarily involved in technology marketing and business development. He may be contacted at n.pearne@bpaconsulting.com

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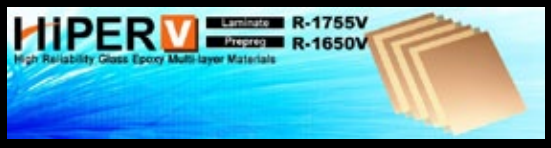

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Just a few highlights of what attendees may expect include:

- FREE! More than 400 exhibitors showing equipment, materials and services for printed boards and electronics manufacturing—plus printed electronics! There's no better place to see and compare

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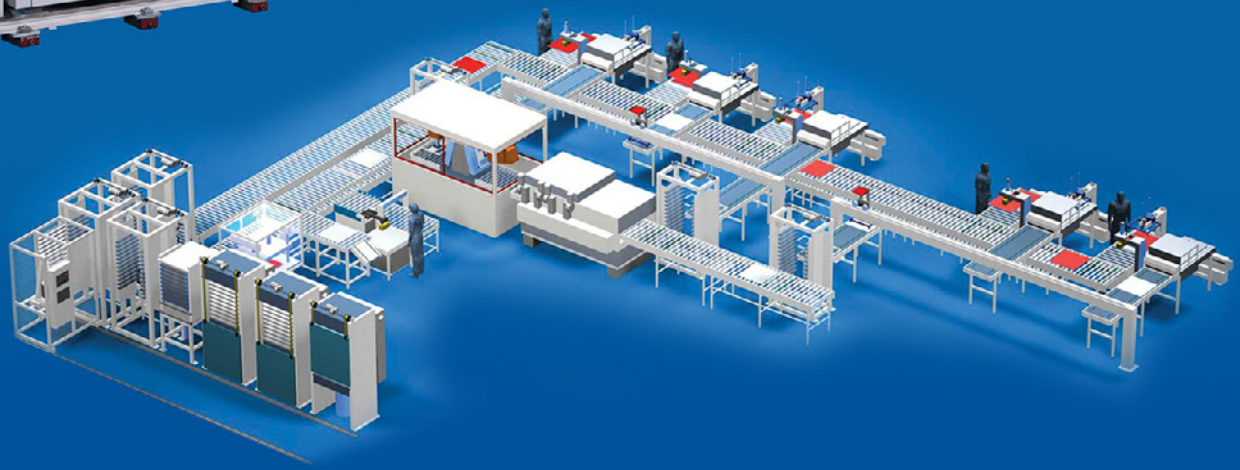

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IPC APEX EXPO Free Keynote Addresses—*All Three Days!*

Opening Keynote Address:
Tuesday, February 19, 8:30-9:30 a.m.

Michio Kaku, Ph.D.
Imagine, and Create, the Future

Join theoretical physicist, best-selling author and futurist Dr. Michio Kaku for an awe-inspiring look at the future! Dr. Kaku is an internationally recognized authority on Einstein's unified field theory and known for using science to predict trends affecting business, commerce and finance.

Dr. Kaku's keynote will present a vision of life in the year 2100, culled from ideas of 300 of the country's most influential scientists. He will explore revolutionary advancements in medicine, energy production, artificial intelligence and aeronautics that will forever change our way of life.

"Electronics has completely revolutionized our world over the past 50 years. Your industry is a critical building block for future advancement, and it is my great pleasure to share my research and predictions with you."

Let yourself be drawn into a future where innovations like Internet-enabled contact lenses let you surf the Web with the blink of an eye… where your commute to work is stress-free, because your car drives itself while you relax…and where tiny brain sensors let you move objects using only the power of your mind. Don't miss this wild and inspirational ride into the future with Dr. Kaku!

Dr. Kaku is one of the world's most widely recognized figures in science. His television documentaries for the BBC, and Science and Discovery channels, as well as his radio shows, such as Science Fantastic, and his New York Times best-selling books like Physics of the Future have popularized science and roused the interest of millions of followers around the globe. A prolific writer, Dr. Kaku has also authored articles for scores of publications ranging from major-market newspapers to popular business, computer and science magazines.

Following his keynote, Dr. Kaku will sign copies of his latest book, Physics of the Future, which will be available for purchase on-site.

Day Two Keynote Address:
Wednesday, February 20, 8:00-9:00 a.m.

Dr. Larry Burns
Reinventing the Automobile

Can you imagine driverless cars?

According to Dr. Burns, former corporate vice president of research & development and strategic planning at General Motors, some of the transformational technology needed is only five to ten years away from being mass-produced. Speaking from 30 years of experience with GM, along with his new pursuits as a director of the Program on Sustainable Mobility for The Earth Institute at Columbia University; a consultant for Google's pioneering self-driving car program; a contractor with National Renewable Energy Laboratory; and a professor of engineering practice, industrial and operations engineering at the University of Michigan, Dr. Burns will

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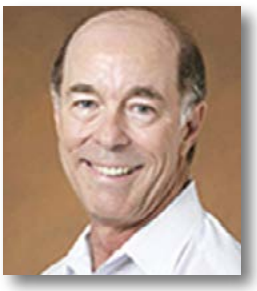
share his compelling vision of the design and technology innovations that will drive a new, very different future of personal transportation.

Day Three Keynote:
Thursday, February 21, 8:00-9:00 a.m.

B. Gentry Lee

Journey to Mars: Curiosity Rover Mission



On August 6, 2012, a mobile laboratory known as the Curiosity rover made an amazing landing on Mars. Curiosity boasts the biggest, most advanced payload of scientific instruments ever sent to the Martian surface. Its mission: to assess whether Earth's neighbor has ever had conditions favorable to life.

B. Gentry Lee, chief engineer for the Solar System Exploration Directorate at the Jet Propulsion Laboratory (JPL) in Pasadena, Calif., is responsible for the engineering integrity of the robotic planetary missions managed by JPL for NASA — including the wildly popular Curiosity rover mission. Join Lee for a fascinating inside look at the mission to Mars that has captured the imaginations of millions and learn about the feats of engineering that brought the Curiosity itself into existence.

IPC APEX EXPO Technical Conference

Tuesday-Thursday, February 19-21

The IPC APEX EXPO technical conference is known worldwide as one of the finest and most selective in the world. Learn about new research and innovations from key industry players in the areas of board fabrication and design and electronics assembly.

Sign up for one day, the full conference or get the most of your money with the Maximum Value Package. To register for the 2013 IPC APEX EXPO, click here.

Click here to search a complete listing of approximately 250 technical conference sessions by topic, category, speaker name, company, etc.

Education and Standards

The 2013 IPC APEX EXPO promises to deliver an impressive slate of educational programs and the largest technical conference for printed boards and electronics manufacturing in the world!

- Contribute to the discussions on the industry standards at more than 80 standards development meetings
- 52 half-day courses taught by experts will offer insights and strategies on the latest innovations and valuable tools
- International Academic Paper Competition — building stronger ties between academia and companies in electronics assembly, PCB manufacturing and design
- Certification programs will provide valuable credentials for EMS program managers and printed board designers
- The Designers Forum will focus on design education and networking with the option to add on an educational course in the afternoon

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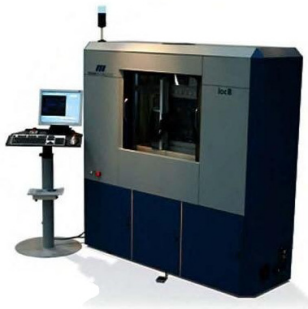

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Professional Development Courses

February 17–18 and February 21, 2013

50 Professional Development course covering issues in design, lead-free technology, materials, process improvement, solder joint reliability and more will be offered at the 2013 IPC APEX EXPO. Going beyond theory, the courses will provide practical solutions to industry issues and challenges. Each course is led by a subject-matter expert, runs for three hours and will include an instruction handbook.

Industry experts such as Mike Carano of OMG, Happy Holden of Gentex, Cheryl Tulkoff of DfR, Bob Wetterman of BEST and Phil Zarrow of ITM will offer one or more courses. Course highlights include:

- Design for Manufacturing (DFM): Best Practices (PD08)
- Extreme HDI: Designing for Maximum Density (PD10)
- Best Practices in Electronics Assembly Processes (PD13 and 17)
- Tin Whiskers: Failure Risk and Mitigation Strategies (PD21)
- Ball Grid Array: Principle and Practice (PD30)
- Package on Package: Design, Assembly, Rework and Inspection (PD44)

"The courses at IPC APEX EXPO will enable engineering and management staff to work smarter in an era of increasing product sophistication," says Susan Filz, IPC director of industry programs. "Attendees will bring home new insights and solutions to boost their productivity."

Engineers like Rigo Garcia, Sr. Quality Assurance Engineer, NASA Goddard Space Flight Center agree, "The conference and courses offer a great opportunity to increase my value as a professional … and having the chance to talk to the technical experts and see equipment being used today is incredibly valuable."

Click here for a complete list of professional development courses along with full descriptions and instructor biographies.

Free IPC APEX EXPO BUZZ sessions

Seven free BUZZ sessions will be offered at IPC APEX EXPO this year. The industry's top technical experts on subjects ranging from automotive and new technologies to conflict minerals, export controls and technology roadmaps will provide insights into timely issues. Admission to the BUZZ sessions and the exhibit hall is free to pre-registrants, a savings of $25 on-site. For BUZZ session times and a complete schedule, click here.

Tuesday, February 19

Addressing "New Technologies," Jasbir Bath, IPC principal engineer for assembly technology, will lead off the BUZZ sessions. Bath will chair a discussion on new and emerging component technologies. Advancements in state-of-the-art electronic component interconnections will be one of the central themes. Then, C. Don Dupriest, Lockheed Martin Missiles & Fire Control, will moderate a panel featuring a "Who's who in electronics," during which IPC Hall of Fame Award recipients will take audience questions on technology and trends and share the wisdom earned from a collective 300-plus years of experience.

Wednesday, February 20

Chris Mitchell, Prime Policy, will moderate a panel on "Export Controls: Understanding ITAR and IT Reform." The panel of experts will provide

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BUZZ sessions *continues*

an overview of International Traffic in Arms Regulations' (ITAR's) application to printed boards.

Later that morning, Fern Abrams, IPC director of government relations and environmental policy, will moderate a session on conflict minerals, which will provide an overview of conflict minerals disclosure and reporting regulation finalized by the U.S. Securities and Exchange Commission last August. A panel of experts will discuss tools for regulatory compliance and customers' requirements. And later that day, a session dedicated to "Automotive Technologies" will provide a current and future view of electronics technology used within the automotive electronics industry.

Thursday, February 21

The final two BUZZ sessions are on the reclassification of FR-4 composite materials and technology roadmaps. Crystal Vanderpan, UL LLC, will discuss UL initiatives and provide an update on UL recognition for laminate and printed board materials. In addition, Marc Carter, IPC director of technology transfer, will take session attendees on a tour of technology roadmapping efforts for printed circuit cards and electronics assemblies. He will highlight the major trends in the evolution of technology across multiple disciplines during the "IPC/iNEMI Technology Roadmap" session.

Designers Forum

Monday, February 18 • 7:30 a.m. – 1:30 p.m.

This program of education and networking is for all individuals with an interest in design. Designers Forum registration includes a networking boxed lunch following the program.

To view all design-related activities at IPC APEX EXPO, click here.

Designers Forum Agenda

7:30 a.m.	Check-in and Networking Breakfast
8:00 a.m.	Roadmapping for Design—Dieter Bergman, IPC Director of Technology Transfer
8:30 a.m.	Efficient Design Data Transfer to Manufacturing Using IPC-258—Edward Acheson, Principal Product Engineer, Cadence Design Systems Inc.
9:15 a.m.	Designing for High-Reliability Applications—Daniel DiTuro, Principal, DiTuro Consulting
10:00 a.m.	Break
10:15 a.m.	The Increasing Complexity of PCB Designs—Happy Holden, Director of Electronics Technologies, GENTEX Corporation
11:00 a.m.	Ask the Flexperts: Mark Finstad, Senior Applications Engineer, Flexible Circuit Technologies Mark Verbrugge, Program Manager, Pica Manufacturing Solutions
11:45 a.m.	Embedded Circuits: New Design Guidelines, Material Selection Variations, Termination Methodologies, Process Information—Vern Solberg, Consultant, Solberg Technical Consulting
12:15 p.m.	Professional Design: Technology and Technique—Rick Hartley, Sr. Principal Engineer, L-3 Avionics Systems
12:45 p.m.	Lunch
1:30 p.m.	Adjourn

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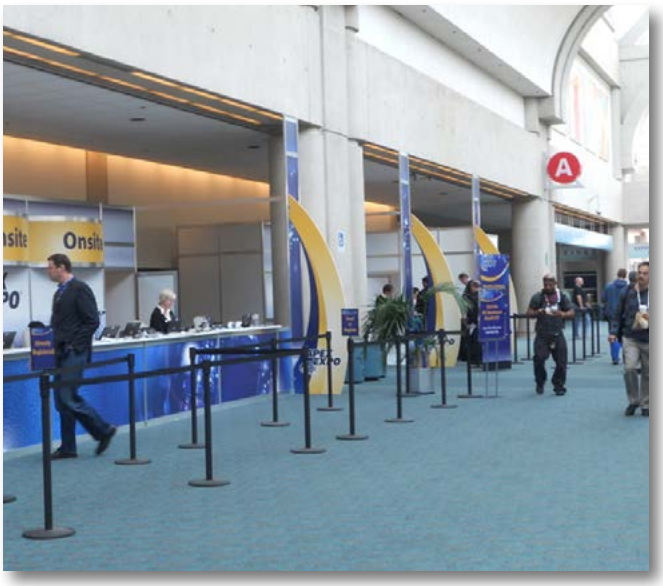
Programs for Executives

NEW! IPC PCB Supply Chain Leadership Meeting (View agenda)

Monday, February 18: 8:00 a.m. - 5:00 p.m.
Networking Breakfast: 7:30 - 8:00 a.m.
Networking Reception and Dinner: 6:00 - 9:00 p.m.



A new learning and networking forum for senior-level executives of PCB manufacturers and supplier companies, this meeting focuses on critical strategic and management topics, such as market trends, customer requirements and the economy. Hear from noted industry experts and find out how your peers are addressing common challenges.

- Disruptive Environmental Regulations
- Business Outlook — The Global Electronics Industry
- Distributive Technologies: What the Executive Needs to Know About
  - Conductive Pastes
  - Embedded Components
  - 3-D Circuits
  - Printed Electronics
  - Laser Drilling
- How Environmental Regulations will Impact Materials Availability
- The PCB Roadmap: An OEM Point of View
- PCB Fabrication in India: Market Status and Opportunities for Cooperation
- Roundtable Discussions

The PCB List —

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Brought to you by PCB007, The PCB List is the world's most comprehensive online directory of printed circuit manufacturers, anywhere. Buyers, specifiers, designers and others looking for a PCB fabricator will appreciate the intuitive navigation, detailed search capability, and global reach of The PCB List. With a Showcase listing, a PCB fabricator can create a neat, organized presentation that puts all pertinent information at a potential customer's fingertips.

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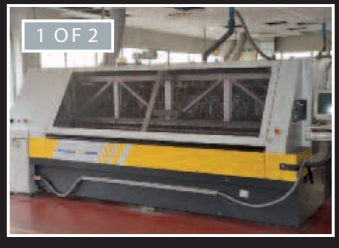
Preview: February 12th or earlier by appointment

Location: Trezzo Sull'Adda (Milan) Italy





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- 2004 ATG A6 Flying probe Tester
- 2003 ATG Exaline Double-Sided Grid Tester
- Luther Maelzar Picomat Tester
- 2006 Pluritec EVO Multistation, 2-Pod CNC Drilling Machine, 180k
- 2006 Pluritec Golden 8888 CNC Drilling Machine, 180k
- (2) 2003 Posalux UltraSpeed 6000 CNC Drilling Machines, 125k
- Hitachi ND4K100E/10P CNC Drilling Machine
- 2004 Pluritec Inspecta HP X-Ray Drill
- Glenbrook X-Ray
- Pluritec Multistation 4-Pod CNC Drilling Machine
- Pluritec Minima Single Spindle CNC Drill
- (2) Telmec SL13.9 CNC Scoring Machines
- (4) Pluritec PDN & Maxima CNC Routers
- Techtron SF 2000 Edge Scoring
- Orbotech Spiron 8800 AOI System
- Orbotech SK75 AOI
- Mania Marco Argos 850 AOI
- Multiline Optiline Post-Etch Punch System
- Projectina Non-Contact CMM
- Burkle 4-Opening Vacuum Mass-Lam Press w.Cold Press
- Barco Silver Writer Laser Photo Plotter
- Hakuto Mach 630UP Auto-Dry Film Cut Sheet Line
- Hakuto Mach 610i Auto-Dry Film Cut Sheet Line
- (2) Bacher Auto Exposure Lines
- ORC HMW501GW & HMW680GW Exposure Printers
- Morton CSR 2600 Mylar Peeler
- MacDermid Multibond Alternative Oxide Line
- Printar LGP-809 Legend Printer
- Majic M800-1500 Laminate Panel Saw
- Pola & Masa BRS-4A Brush Line
- Pola & Masa Plate Scrubber
- (2) IS Pumiflex Pumice Scrubbers
- IS Titanium Etchmaster & SS Devmaster
- IS LPI Devmaster
- Depeltronik Micro-Etch Line A-1130-EX
- Occleppo Tin (Sn) Stripper 750/02/P-300
- Occleppo Develop-Etch-Strip Line
- Unicote 175 HASL Line
- (2) Argon Hydra 2 & 3 Semi-Auto Screen Printers
- Cross Section & Chemical Lab
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For a preview of these new and innovative products, including images, booth numbers and overviews, visit the IPC New Products Showcase.

Real Time with...
Interviews and Panel Discussions

This year, I-Connect007 and the Real Time with... program returns to San Diego, California, bringing you complete video coverage of IPC APEX EXPO 2013. Last year, we brought you more than 150 interviews—and this year promises to be just as prolific.

The Real Time with team of editors, guest editors, videographers, and video editors will be working throughout this seminal event to capture the keynotes and bring you one-on-one interviews and panel discussions with the industry's top technologists, engineers, and business leaders.

Visit www.realtimewith.com for updated information about IPC APEX EXPO 2013.

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I·CONNECT007
GOOD FOR THE INDUSTRY

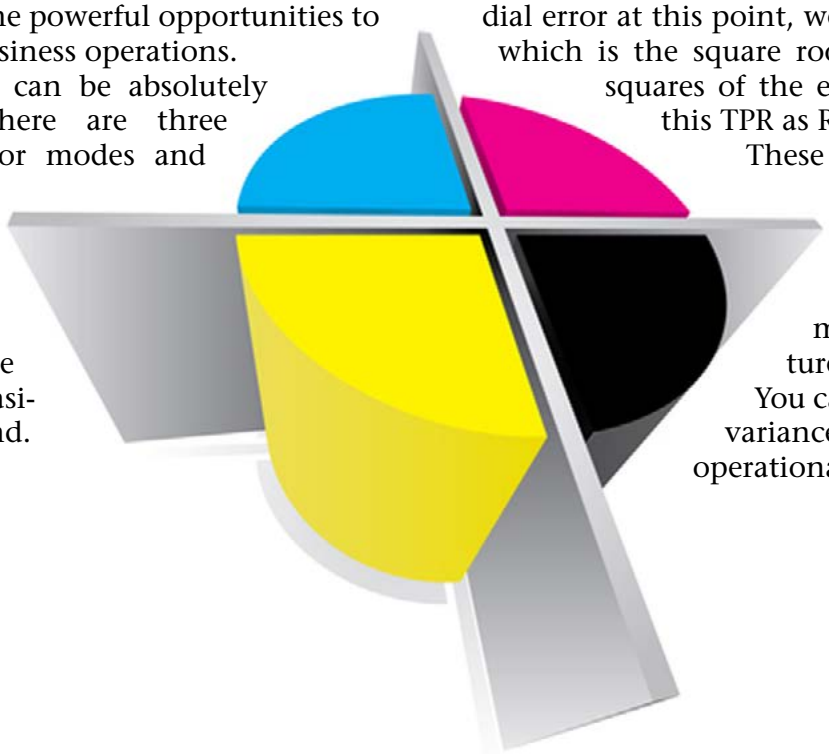
DAM Registration

by Gray McQuarrie
Grayrock & Associates

SUMMARY: By understanding precisely the three different registration error modes, you have huge opportunity to reduce your plant's costs and improve your competitive position.

In last month's column, How Can You Predict Your Company's DAM Future?, I discussed the bad behaviors that block progress in understanding PCB registration. Once data and discovery overtake people's opinions and their need to be right, progress can be made. Today, PCB registration isn't the problem it once was. However, we have left the understanding of registration in the hands of a few specialists. This is a mistake. Registration is fundamental to making a board. It is still a major contributor to scrap from internal shorts. It defines our level of technology capability and is part of any OEM's future technology roadmap. If we don't understand registration the way we need to, then we are blind to some powerful opportunities to improve our business operations.

Registration can be absolutely understood. There are three registration error modes and these are offset, scaling, and rotation. Let's look at the offset errors first, since they are the easiest to understand.



Offset Errors

Let x_{tp} and y_{tp} represent the desired true coordinate position of a hole or connection feature that goes between layers on a printed circuit board. Let's denote the offset error in the x direction to be a and the offset error in the y direction to be b. Let's say our true coordinate position is (1", 1") and we have an offset error of 0.001" in both a and b. The result of adding these offset errors creates a new position, which we will denote as x_i and y_i, where x_i is equal to 1.001" and y_i is equal to 1.001". It's clear from this simple example that the offset registration error formulas are:

$$x_i = x_{tp} + a \qquad 1)$$

$$y_i = y_{tp} + b \qquad 2)$$

If we wanted to know the actual TPR or radial error at this point, we would have √2 mils, which is the square root of the sum of the squares of the errors. We can denote this TPR as RSSE.

These offset errors come from misalignments of different layered images and misalignments of machines to panel features such as in drilling. You can add the offset error variances together from each operational step, but what you

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San Diego, CA

May 20–23, 2013
IPC ESTC™ — Electronic System Technologies Conference & Exhibition
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June 4–5, 2013
IPC/FED Conference on Embedded Components
Frankfurt, Germany

June 11–13, 2013
IPC Conference on Flexible Circuits
Sponsored by Minco
Minneapolis, MN

August 20–22, 2013
IPC APEX India™
Bangalore, India

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IPC Conference on Component Technology: Closing the Gap in the Chip to PCB Process
Sponsored by Amkor Technologies, Inc.
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November 12–14, 2013
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Announcing the Release of the 2013 IPC International Technology Roadmap

Put the informational resources of the IPC Technology Roadmap to work for your long-range and strategic planning activities. It's like adding your own global research department to your staff.

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- Explanation of new business models; expectations between OEMs, ODMs, EMS providers and fabricators; and the rise of contractor specialists
- Expanded coverage of the printed electronics industry as it matures into a truly viable option

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Questions? Contact IPC registration staff at +1 847-597-2861 or registration@ipc.org.

can't do is add the variances from the different registration error modes together. I remember listening to a talk once where the speaker explained that if you did a classic statistical analysis of adding up all of the variances from the different type of registration errors you wouldn't be able to build the board. But he went on to say, "we can build these boards." He said, "It's as if some of these errors subtract from the other ones." His intuition was correct, but his application of statistical analysis was wrong. As you will see, registration error modes interact, where at times they cancel each other out and at other times they add to each other and you can see both of these things happening at the same time over the surface of a board! Next, let's consider the scaling errors.

Scaling Errors

This would be where we overcompensate or undercompensate the stretch of the circuit image to correct for the material shrinkage (though sometimes it is growth) that occurs after PCB lamination. Fortunately, the material movement can be approximated using a linear scaling factor or scalar. For example, let's say we find we aren't aligned to our (1", 1") coordinate, because we have undercompensated the circuit image by 1 mil/inch in both directions. The way we can express this error is by multiplying x_{tp} and y_{tp} by 0.999, which is our linear scalar. At this (1", 1") point, the scaling errors have negated the effect of the tooling error! From this example, our formulas for combining offset error and scaling error, where u is the scaling error in the x direction and v is the scaling error in the y direction are:

$$x_i = x_{tp} * u + a \qquad 3)$$

$$y_i = y_{tp} * v + b \qquad 4)$$

Scaling errors come from bad predictions of material movement, which can have a number of different sources including circuit image measurement errors. Today, we have sophisticated imaging systems that can measure the movement of each layer, feed this information into a data base, and then extract the scalar values we should use from software using a neural net algorithm. Moreover, direct imaging systems in many ways have removed the errors created from environmentally unstable artwork tools. As sophisticated as these systems are, they don't correct for devastating rotational errors that happen because we still need hard tools such as those required for aligning cores to each other in multilayer lamination.

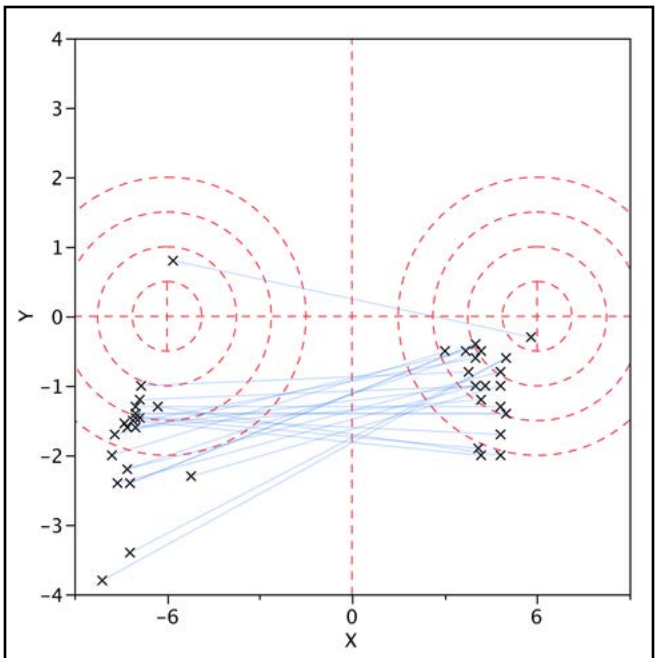

Figure 1: Post-etch punch data for 23 panels punched consecutively. Shown are the locations of the left and right side tooling holes. The blue lines connect each left-right pair and reveal (though exaggerated) the rotational error.

Rotational Errors

Figure 1 shows post-etch-punch data presented in a unique way (using script I composed with JMP statistical analysis software). This is real data from 23 panels from the same PEP machine, where one panel was punched right after the other. So often we see PEP data presented in an almost incomprehensible way using an SPC chart. An SPC chart hides how punched holes interact on the left side and the right side creating a rotation. The blue lines in Figure 1 show the obvious rotation created from each left side and right side data set.

Too many of us try old ways of presenting data, not appreciating that visualizing data is

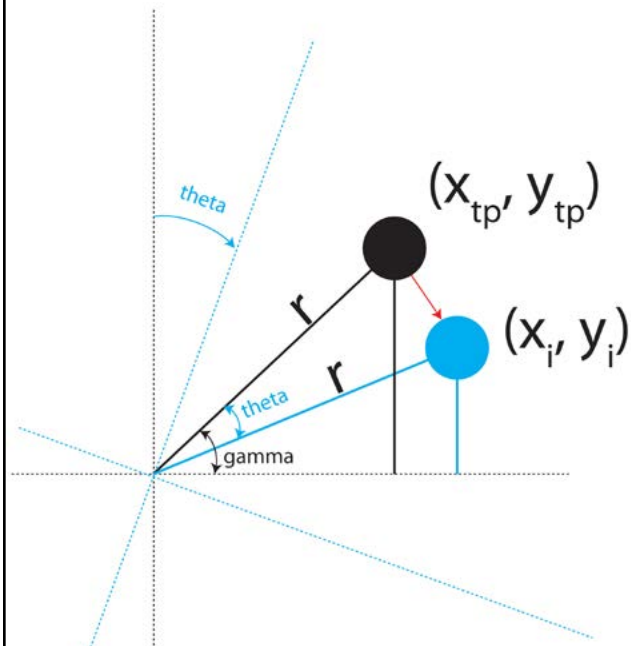

Figure 2: The trigonometric relationships that allow us to derive and understand a rotation of a coordinate grid by an angle theta.

vital to our understanding and decision making. Being creative with the way you plot data is an important skill that needs to be nurtured. In order to appreciate the possibilities, consider one of Edward Tufte's books, such as, "The Visual Display of Quantitative Information," which provides inspiring examples.

In Figure 1, I added 6 mils to the x-dimension for the right tooling hole data and -6 mils to the x-dimension for the left tooling hole data. In this way I can see both the right and left tooling hole data sets on one graph. The rotation is exaggerated since the distance between the left and right tooling holes is compressed. The important point with this graph is that the offset and rotational errors are obvious.

You can find the mathematical formula for a rotation of a coordinate grid on the internet since this is the math behind rotating 2Dand 3D objects in computer programs. In order to understand rotational effects, let's do a rough derivation.

Figure 2 shows the effect of a rotation of an angle of theta radians in a clockwise direction emanating from the center of the panel. With this rotation, the true position shown in black moves to the resulting position shown in blue. By the way, if you want to change the center of rotation on the panel you simply add offset errors!

From Figure 2 we have:

$$x_i = r * \cos(\text{gamma} + -\text{theta}) = \quad 5)$$

$$r * \cos(\text{gamma})*\cos(-\text{theta}) - r * \sin(\text{gamma}) * \sin(-\text{theta}) \quad 6)$$

Since we will keep track if we are making a negative or positive rotation (clockwise or counter clockwise) within the sign of the angle (negative or positive), we don't have to keep track of the sign of the angle for rotation (theta) as we continue with this derivation.

We see from Figure 2:

$$x_{tp} = r*\cos(\text{gamma}) \text{ and } y_{tp} = r*\sin(\text{gamma}) \quad 7)$$

When we substitute equation 7 into equation 6 we get:

$$x_i = x_{tp} *\cos(\text{theta}) - y_{tp} *\sin(\text{theta}) \quad 8)$$

Similarly, we can show:

$$y_i = x_{tp} *\sin(\text{theta}) + y_{tp} *\cos(\text{theta}) \quad 9)$$

If we consider an angle error for x_i of -0.001 radians we have from equation 8, after taking the cos and sin of theta: 1 + 0.001 or a 1 mil shift to the right in the x direction and approximately 1 mil shift down in the y direction. Since the scaling errors and the offset errors canceled themselves out at this particular coordinate position, this is the final location of the feature.

Based on the above equations, the grand registration error equations are:

$$x_i = (x_{tp*}u + a) *\cos(\text{theta}) - (y_{tp*}v + b) *\sin(\text{theta}) \quad 10)$$

$$y_i = (x_{tp*}u + a) *\sin(\text{theta}) + (y_{tp*}v + b) *\cos(\text{theta}) \quad 11)$$

Equations 10 and 11 have great power. We can compute all of the registration errors and its variation over the entire surface of a panel if we know the offset errors, rotation errors, and

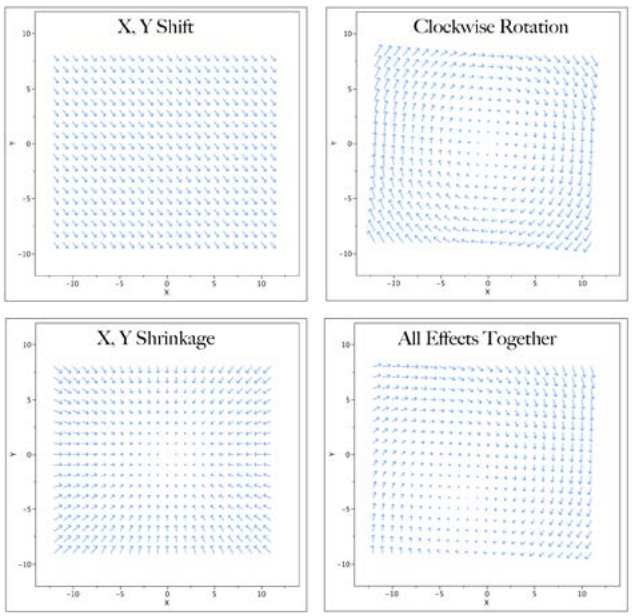

Figure 3: Four graphs that walk us through each of the registration error modes of offset (upper left), rotation (upper left), and scaling error from shrinkage of the material (lower left). When we add all of these effects together by using equations 10 and 11, we get the graph in the lower right.

scaling errors. For example, Figure 3 walks us through each of the different registration errors modes.

Putting it All Together

We see the offset shifts, clockwise rotation, and the scaling errors by themselves, and we see the patterns they make over the entire surface of the board. When we add everything together we get the graph on the bottom right hand side of Figure 3. In this graph, some areas of the board have very good registration, because the errors have canceled each other out and in other areas of the board the errors have grown and compounded each other (far right-hand corner). Without the data shown in Figure 3, a board shop could make panels too big, or accept a job with too tight of registration requirement, or fail to setup the process correctly so as to provide the best yield.

In order to be in the know, we need a method of extracting registration errors out of coordinate measurement data. The way I extract registration error is using a nonlinear fit of co-

Parameter	Value
a	1.89 mils
b	-0.43 mils
u	1.000634
v	1.000259
theta	-0.00034 radians
RMSE	0.0000675

Table 2: The parameters derived from the nonlinear fit of equations 10 and 11 from the data in Table 1.

Xtp (inches)	Ytp (inches)	Error (mils)	Fit Estimate	Corner
-11	-8	-7.75	-7.77	Low Left (X)
		1.24	1.20	Low Left (Y)
-11	8	-2.4	-2.38	Up Left (X)
		5.38	5.35	Up Left (Y)
11	-8	6.23	6.17	Low Right (X)
		-6.26	-6.22	Low Right (Y)
11	8	11.50	11.56	Up Right (X)
		-2.10	-2.07	Up Right (Y)

Table 1: The X and Y errors at each of the four corner position measurements, as well as the estimate from the nonlinear fit used to extract the offset, scaling, and rotational errors.

Most-Read Mil/Aero007 News Highlights This Month

Ventec AS9100C Approval Fully Certified

Ventec Europe Managing Director Mark Goodwin said, "This accreditation confirms our emerging position as a leader in the design and manufacture of high-reliability materials for the military and commercial aerospace sector. I believe Ventec International Group is the only copper clad laminate and pre-preg manufacturer with this accreditation."

N.A. Military Avionics Market Report 2012

As pressure on the budgets of both countries forces reassessments of that spending, the military services will need to think strategically about the future procurements and methodologies.

U.S. Military: $909.3M Budget in Vetronics Procurement

New analysis from Frost & Sullivan, U.S. Military Vetronics, finds that the 2013 U.S. military budget requests $909.3 million in vetronics procurement, which will decline at a rate of 8.6% until 2017.

Global Homeland Security Market to Reach $281B by 2022

In a report titled "The Global Homeland Security Market 2012-2022 - Market Size and Drivers: Market Profile," market analyst Strategic Defence Intelligence forecasts that the global homeland security market will reach $198 billion in 2012 and increase at a CAGR of 3.55% during the forecast period to reach its peak of $281 billion by 2022.

Report Examines UK Defense Industry Through 2017

"Industry Market Opportunities and Entry Strategies, Analyses and Forecasts to 2017" offers the reader an insight into the market opportunities and entry strategies adopted by foreign OEMs to gain market share in the UK defense industry.

Commercial Aircraft Cabin Lighting Market at $1.25B by 2017

According to a new market research report, Global Commercial Aviation Aircraft Cabin Lighting Market, Forecast & Analysis (2012 - 2017), the total global commercial aviation aircraft lighting market is expected to reach $1.25 billion by 2017 with a CAGR of 5.43%.

Global UAV Payload Market to Hit $68.8B by 2022

With the expected growth in market demand and diversity in UAV applications, there is a growing requirement for the future UAV and payload design to combine multi-mission, modular, open architecture features, capable of accomplishing diverse missions.

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ordinate data to equations 10 and 11 using JMP. For example, Table 1 shows the errors found in the x and y dimensions at four corner points of a panel, as well as the predicted result from JMP's nonlinear fit. Table 2 shows the predicted registration parameters as well as the error from the lack of fit expressed as the root mean square error or RMSE.

The Bottom Line

By being able to measure each of the registration error modes and understanding how to add them together correctly, you can reduce your costs and improve your technology in a way that maximizes your company's competitive position. **PCB**

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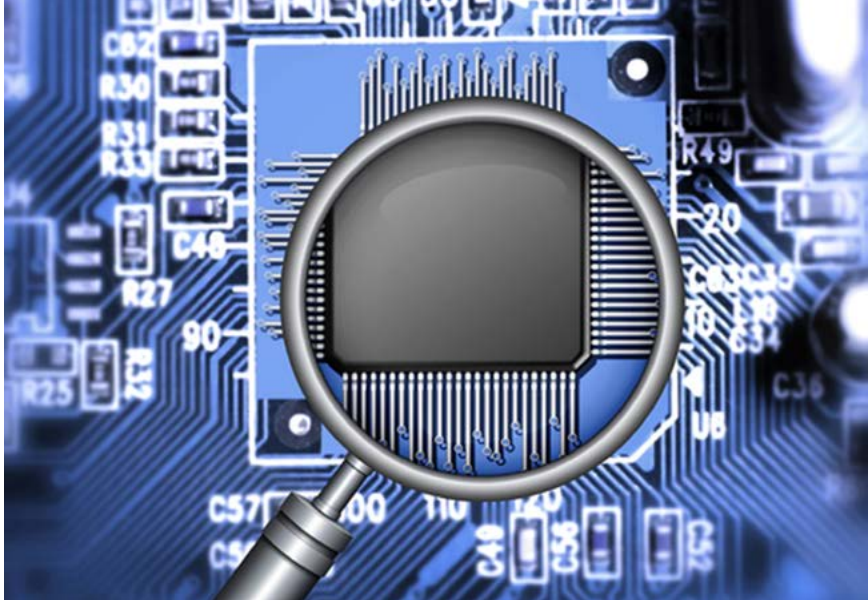
ARTICLE

FIB, BEYOND SEM-EDS ANALYSIS



by Patrick Valentine and Lisa Gamza
OMG ELECTRONIC CHEMICALS

Abstract

The SEM-EDS has proven itself an invaluable tool in examining process outputs, and analyzing defects. Going beyond the SEM-EDS, the focused ion beam (FIB) can be used to qualify processes, and perform root cause failure analysis.

We authors have similar memories from our childhood, of our mothers saying something like, "If you tell a fib people will know." Ironically, many years later, we're using the FIB to detect process fibs.

So just what is this FIB analysis all about?

First, let's look at what a scanning electron microscope (SEM) is and how it works. Just as an optical microscope forms an image by reflecting light from a sample surface, SEM creates an image by producing electrons that are accelerated and focused at the surface of a specimen. Once the electrons strike the surface of the sample, secondary electrons (SE) are ejected from within the sample and attracted by the secondary electron detector (SED).

Unlike optical microscopes, the wavelengths of electrons are much shorter than those of the light photons which allow the SEM to obtain high resolution images. It is also worth mentioning that the uniqueness of three-dimensional SEM images is based on the depth of field phenomenon, which the light microscope lacks (Figure 1).

The basic principles of the SEM imaging involve a flow of electrons formed under high vacuum by an electron gun. The samples are irradiated by the electron beam, and secondary electrons are ejected from the irradiated sample as the result of electron-specimen interaction. Inelastic electron scattering is the basis of electron microscopy. The secondary electrons are attracted to the SED, which are sent through a series of electronics and ultimately displayed on the monitor as an image[1].

The source of the electrons in SEM varies. The most common ones are tungsten (W) hairpin, lanthanum hexaboride (LaB_6), and field emission gun (FEG) installed in FESEM instruments, which are known for their ability to produce the highest resolution.

As time goes by, new developments take place in the microscopy world, but electron microscopy remains one of the most distinctive techniques for imaging and analyzing submicron features[2].

While scanning electron microscopes have been around for a while, FIB came into use in the mid-1980s. It turned out to be the preeminent tool used in a wide range of materials science applications, from analyzing and editing semiconductors and transmission elec-

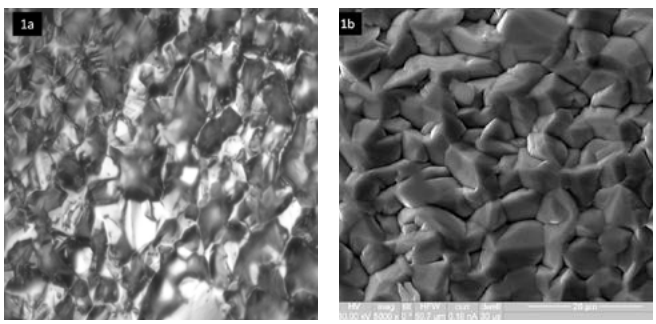


Figure 1: Images of copper-based alloys plated with matte tin deposit taken by optical microscope (a) and scanning electron microscope (b).

tron microscopy (TEM) sample preparation to microstructural analysis and micro- and nano-patterning.

FIB and SEM are very similar tools with the major difference being the use of ions instead of electrons.

SEM images are generated from negatively charged electrons, whereas the FIB technique ejects about two secondary electrons for every ion that strikes the sample. As you can see, both SEM and FIB can produce SE which are attracted to the SED[3].

The most common type of ion source is liquid-metal ion source (LMIS) which is produced with gallium (Ga) material. Its low melting temperature, low volatility and vapor pressure make Ga LMIS one of the most widely used.

During the interaction between large ions and the sample, milling of the samples always happens while under the ion beam. That phenomenon along with the nanometer resolution gives the FIB instrument a unique feature—a capacity of controlled surface patterning and milling.

With the well controlled ion beam, milling is used to create a rectangular, square or a round hole in the sample material; furthermore, the well controlled ion beam has the ability to produce more complicated operations in the nanotechnology field.

FIB patterning/milling allows exclusive power of the controlled removal of the material within the sample. It enables the analyst to view not only the top surface of the material, but also look below the surface while precisely controlling the milling rate and parameters of the cross-section (Figure 2).

FIB secondary electron imaging (Figure 2a) offers complimentary information about tin grain boundaries due to the surface topography and material differences. This phenomenon is called "channeling contrast," and is achieved by ion-induced secondary ions. Such contrast image allows the measurement of the size of the grains on the crystalline structures which are exposed to the ion beam at different incidence angles. Copper alloy grain structure can also be seen on the ion beam image.

FIB imaging is a destructive analytical technique; therefore, a metal line is sometimes deposited on the area of interest to preserve it from the damage that can be caused by the ion beam. Low ion beam currents are also recommended in this technique.

Ion beam technology allows for adding the material to the surface of the specimen as opposed to removing it. This is achieved by a gas delivery system which brings a gas compound close to the area of interest. Most common materials used for the deposition are platinum, tungsten, carbon, and silicon oxide.

One of the few FIB milling artifacts is sample redeposition. Redeposited material lands behind the cross-section with no effect on the region of interest (ROI). Redeposition varies with the material, and increases with the beam current and shape of the feature milled (Figure 3a).

In addition to redeposition, so called "curtain effect" takes place due to surface roughness and shadowing effect. This effect looks like formation of a stripy, rippled pattern across the milling surface. It occurs during ion attack of the milling surface and has to do with the roughening of the milling and diffusion which smoothes the surface; see Figure 3b. To avoid this issue, it is advised to use a protective metal or carbon layer along the ROI before the initial milling, reducing the rough surface layer and allowing the clean surface for the ion beam to mill. If the curtain effect still continues, reducing the beam current is recommended.

Despite the artifacts which come with ion imaging and milling, it is hard to overestimate the role of the FIB examination in materials science research and failure analysis fields.

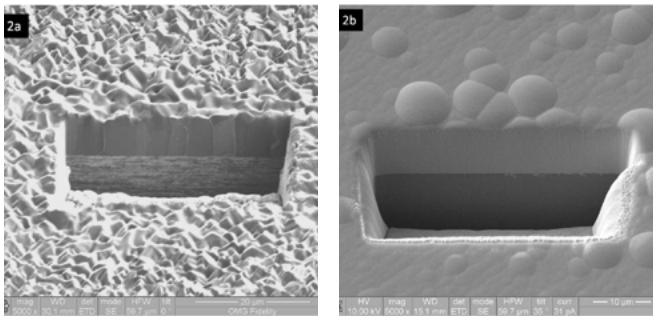


Figure 2: FIB cross-section (a) of copper-based alloy plated with matte tin deposit, as well as FIB cross-section of an electroless nickel deposit plated on aluminum alloy substrate (b).

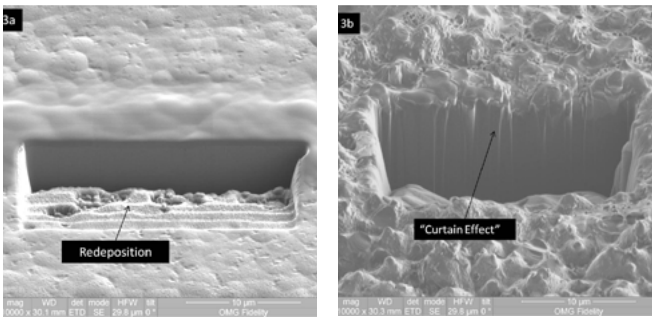


Figure 3: FIB milling artifacts—redepostion (a) and curtain effect (b).

With a solid foundation of what the SEM-FIB is and how it works, let's look at two case studies.

Case Study #1

Two different electroless copper processes are under investigation; the goal is to establish the copper coverage characteristics of each process, specifically looking at the glass coverage.

To digress shortly, since approximately the late 1970s, microscopy has been widely used to detect minute defects in plated through holes (PTH), due to increasing demands in circuit integrity[4]. And instead of using incident light, backlighting was developed which provides a much more sensitive measure of assessing coverage[5]. Backlight coverage scales are either 0-5, or 1-10, with the highest number indicating complete coverage.

Now let's get back to our case study. Both electroless copper processes (denoted A & B) deposit ~50 µin of electroless copper, and both produce backlight ratings of 10. So are both processes producing the same quality output? No!

What makes the processes different? We need to take a closer look to see the differences; the old adage "if you can't see variation then you're not measuring finely enough" applies here. Lets first look at process A. With the PT ground in half we're ready to examine it with the SEM (Figure 4).

With the FIB cut completed we can examine the adhesion of the electroless copper to the transverse glass fibers (Figure 5).

Now let's examine process B and prepare and examine the coupon in the same fashion (Figure 6).

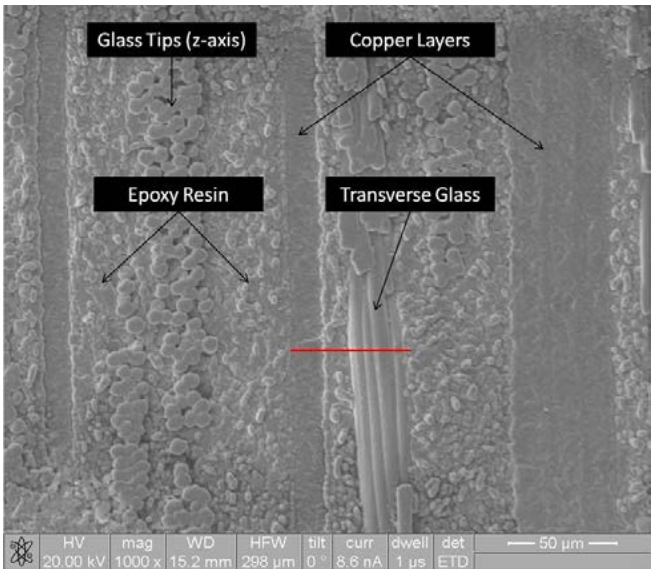


Figure 4: Process-A PTH with components labeled. The red line is the marking for the FIB cut area.

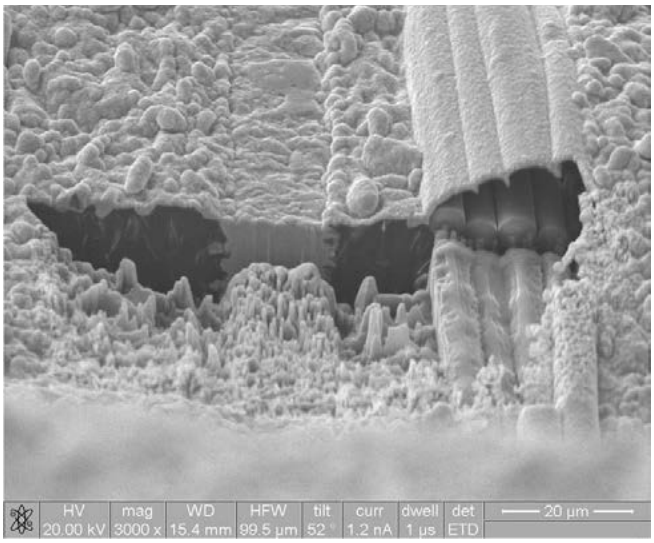


Figure 5: FIB cut of the PTH from Process A. Note the electroless copper lifting from the glass fibers.

The FIB cut reveals the difference between the two processes; that difference being the adhesion of the electroless copper to the transverse glass fibers. Process A lacks adhesion, whereas process B has adhesion; process B was installed.

Relying solely on the backlight ratings caused the service team and process engineer to chase random voiding occurrences in areas that were thought suspect, while the real culprit area

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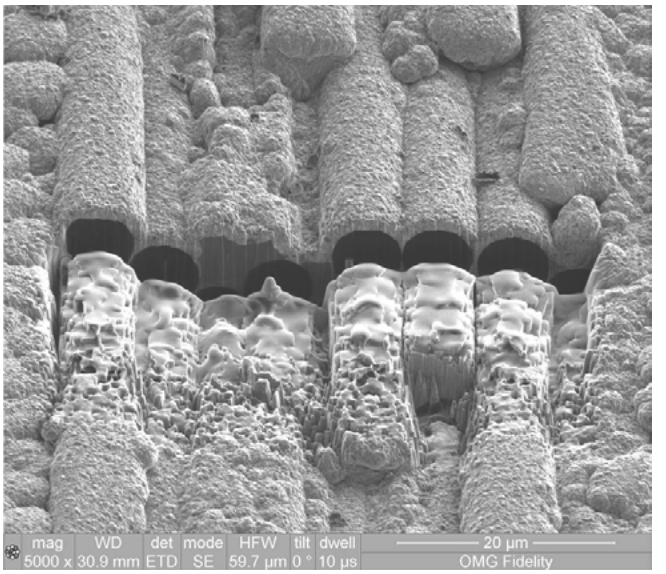

Figure 6: FIB cut of the PTH from process B. Note the adhesion of the electroless copper to the transverse glass fibers.

was deemed robust. Without the FIB cut the service team and process engineer may never have gotten to the actual root cause during the swap out of process A with process B.

Case Study #2

An assembler reported poor solder wetting on a BGA feature, with the final finish being electroless nickel immersion gold (ENIG). Initial concerns were of the dreaded black pad and with those words spoken, Pandora's Box was opened, thus putting into motion the pandemic thoughts of lot scrap, reliability, PCB integrity, process controls, etc. These fears sweep through an organization faster than wildfire. Whatever the root cause is, quickly determining it, quarantining suspect parts, and correcting the root cause are paramount.

If black pad is present, we would expect to see nickel corrosion spikes and other tell-tale artifacts during failure analysis[6]. One of the poorly soldered BGA pads is shown in Figure 7, along with the red (A) and blue (B) lines marking the FIB cut areas; note that the BGA was removed for pad examination. The BGA pad after FIB cut is shown in Figure 8; there is no indication of electroless nickel corrosion.

The FIB cut of Figure 8 revealed an artifact in the bulk solder area that deserved further

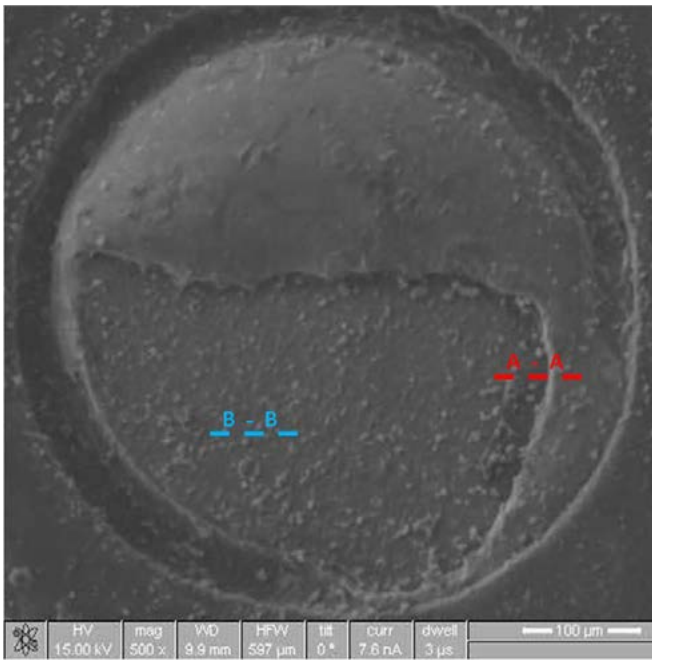

Figure 7: BGA pad with poor solderability.

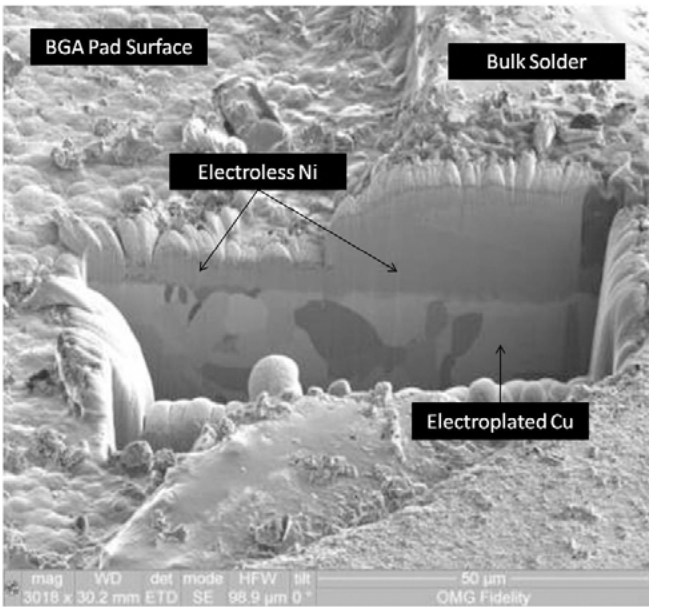

Figure 8: FIB cut of the BGA pad area A.

analysis. The area shown in Figure 9 was analyzed with SEM-EDS and discovered to contain a significant amount of tin, indicating a problem with the solder paste and/or reflow profile.

Area B was FIB cut to look for nickel corrosion spikes and nickel thickness (Figure 10). No evidence of nickel hyper-corrosion (black pad) was detected and the nickel thickness was mea-


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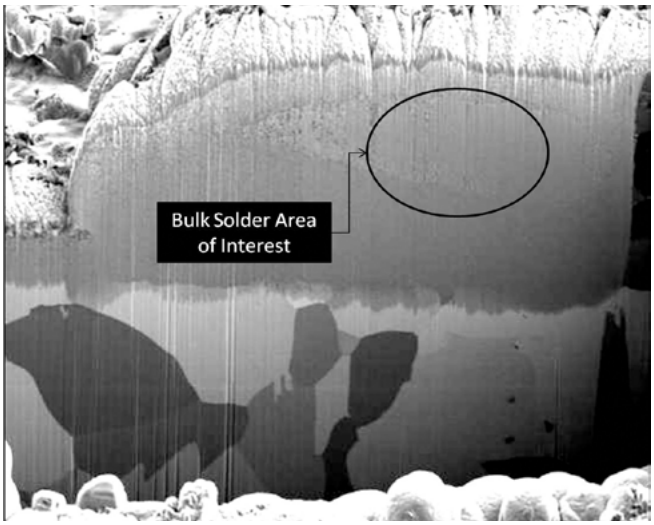

Figure 9: FIB cut of the BGA pad area A, bulk solder was analyzed with SEM-EDS.

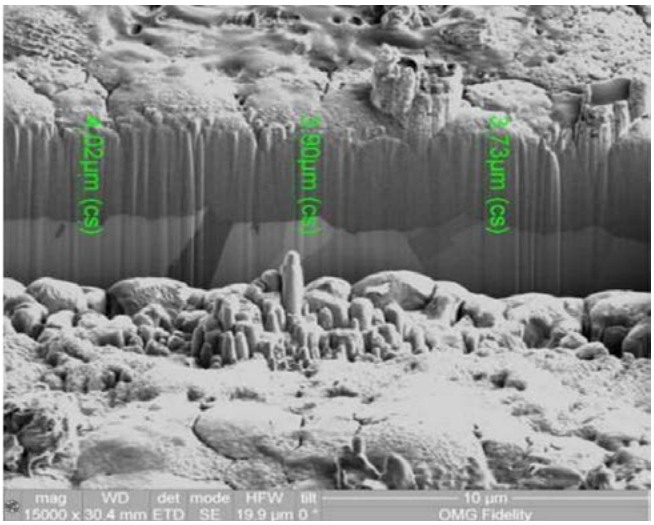

Figure 10: FIB cut of area B, normal nickel thickness with no corrosion spikes.

sured at an average of ~3.88 microns (153 µin), which is well within the IPC-4552 ENIG specification.

With the FIB analysis complete attention was turned towards the reflow profile for investigation. A dye-and-pry was done on an adjacent BGA and cold solder joints were detected. Once modifications were made in assembly the defect was eradicated.

Here again, we see the invaluable asset the FIB is in determining the root cause of the problem.

When a SEM system is combined with the FIB column, it results in high-resolution imaging along with milling capabilities in-situ. Such an instrument becomes an indispensable analytical tool for modern materials science analyses, process qualifications, and root cause failure analysis. As with all tools it has a set of limitations that must be understood, and the tool must be used properly by qualified analysts to get the most out of it.

The authors wish to acknowledge and give special thanks to Paul Anzalone for his review of the FIB theory. **PCB**

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Most-Read PCB007 Market News Highlights This Month

World May Again Dive into Recession

The world economy has weakened considerably during 2012 and is expected to remain subdued in the coming two years, according to the United Nations in its latest issue of the World Economic Situation and Prospects 2013 (WESP). The global economy is expected to grow at 2.4% in 2013 and 3.2% in 2014.

Low-cost Tablet PCs Poised to Gain More Attention

Tablets have become an undisputed highlight for this year's peak season, with under-$200 devices such as Nexus 7 and Kindle Fire HD poised to gain major attention within the market. Considering how Google and Amazon are able to resort to advertising costs and other means to make up for their tablets' low prices, PC vendors are in for some serious competition.

IHS Releases Top 10 Solar Market Predictions for 2013

"The photovoltaic industry is in the midst of wrenching change—buffeted by government incentive cuts and nose-diving prices that has hurt solar suppliers worldwide, rocked by trade disputes among its major players, and hamstrung by a sputtering global economy," said Ash Sharma, director of solar research at IHS.

Significant Growth for Automotive Electronics Market

"Growth areas in automotive development include electrified powertrains, ADAS (advanced driver assistance systems), HMI (human-machine-interface), smartphone connectivity and telematics," says Kevin Mak, automotive electronics analyst. This has propelled regions such as Silicon Valley, California, into the automotive spotlight.

25% of PC Owners May Switch to Other Devices

Twenty-five percent of computer owners say they may not replace their PC when their current machine becomes unusable, signaling a possible trend of consumers becoming PC-less because they switch to a tablet or a similar device, according to a national survey conducted by the Center for the Digital Future.

Global IT Spending Forecast to Reach $3.7 Trillion in 2013

Worldwide IT spending is projected to total $3.7 trillion in 2013, a 4.2% increase from 2012 spending of $3.6 trillion, according to the latest forecast by Gartner, Inc. The 2013 outlook for IT spending growth in U.S. dollars has been revised upward from 3.8% in the 3Q12 forecast.

Global Semi Market Posts Strong November Sales

The Semiconductor Industry Association, representing U.S. leadership in semiconductor manufacturing and design, has announced that worldwide sales of semiconductors reached $25.73 billion for the month of November 2012, the largest monthly total of 2012.

Smartphones Lead Portable Consumer Electronic Market

Smartphones continue to steal market share from portable consumer electronic (CE) devices. Annual shipments of handheld game players are expected to decline at least 4% YoY with the North American market experiencing a fall of nearly 13%. In the digital camera market, shipments are expected to decline over 11% YoY worldwide and nearly 20% in North America.

UK Consumer Manufacturing Industry to See Revenue Drop

The UK consumer electronics manufacturing industry is expected to generate revenue of £2.17 billion in 2012-13, down 1.2% compared with 2011-12. According to IBISWorld industry analyst Nigel Fitzpatrick, "The industry is highly globalised, with exports amounting to £1.78 billion and imports amounting to £5.57 billion in 2012-13."

Global LTE Smartphone Shipments at 275 Million Units in 2013

According to the latest research from Strategy Analytics, global LTE smartphone shipments will grow threefold to reach 275 million units in 2013. It will be a record year for 4G technology. Companies leading the growth spurt will include Apple, Samsung, LG and others.

COLUMN

Conflict Minerals: RoHS on Steroids?

by Steve Williams

SUMMARY: *I never imagined as my wife and I sat in a little theater in Wisconsin, watching Leonardo DiCaprio's newest movie, Blood Diamond, that seven years later just such a thing might have a major impact on our business. But the Conflict Minerals initiative may become more burdensome to our industry than RoHS, thanks to new legislation.*

What is it?

Conflict minerals are certain minerals mined under conditions of armed conflict and human rights abuses in the Democratic Republic of the Congo (DRC). The exploitation is characterized by extreme levels of violence (particularly sexual and gender-based violence) by various militia groups against civilian populations. The looting of the Congo's natural resources is not limited to domestic corruption; during the Congo Wars, Rwanda, Uganda and Burundi, particularly, profited from the Congo's resources. These governments have continued to smuggle resources out of the Congo to this day and direct the profits from the sale of these minerals to finance the continued conflict of the Second Congo War. Conflict minerals are essential raw materials that are used in the manufacture of printed circuit boards and electronic components, which are the backbone of most consumer electronics such as cell/smart phones, tablets, computers, and digital music players, digital cameras, and video game consoles. Also included are many aerospace, automobile, and communication products, as well as bullets and jewelry.

Dodd-Frank Legislation

On August 22, 2012, the Securities and Exchange Commission, as part of the *Dodd-Frank Wall Street Reform and Consumer Protection Act,* adopted a final rule that was passed by Congress (Section 1502) which will require public companies to make disclosures about the use of conflict minerals in the products that they manufacture or contract to manufacture.

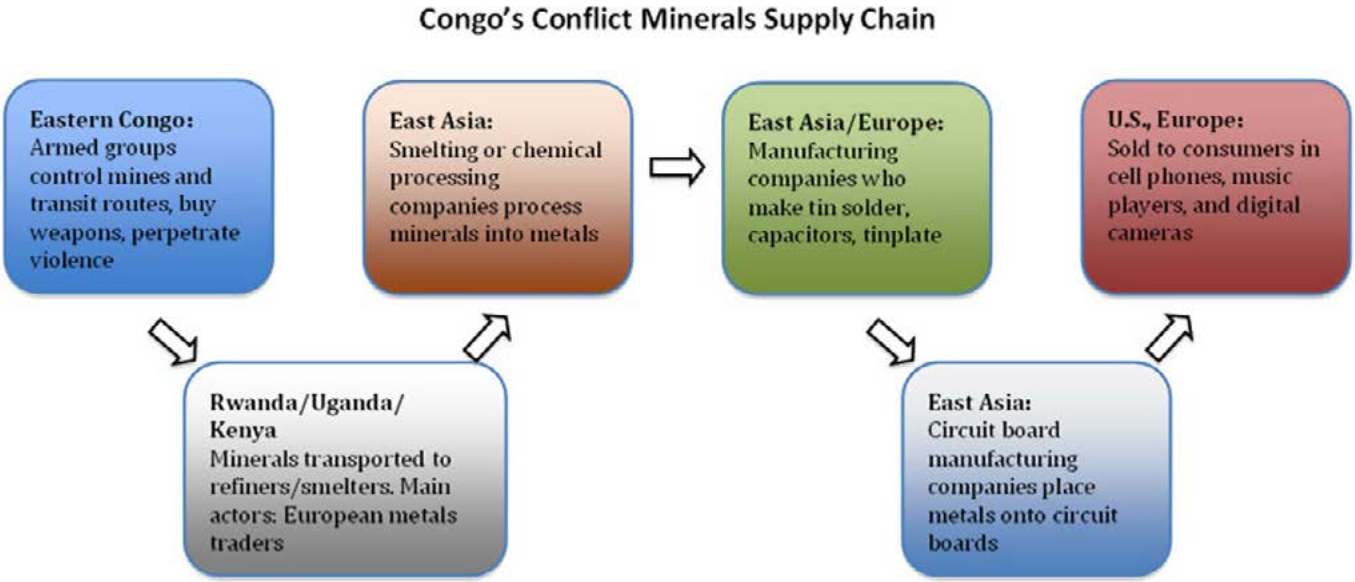

Figure 1: Conflict minerals flowchart. (source: rightrespect.org)

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What are the Minerals?

Conflict minerals are currently* defined in Section 1502 as consisting of four specific minerals and their derivatives:

- ***Columbite-tantalite*** (coltan) is the metal ore from which tantalum is extracted; tantalum uses include electronic components (mobile telephones, computers, video game consoles, digital cameras) and alloys for making carbide tools and jet engine components
- ***Cassiterite*** is the metal ore most commonly used to produce tin; tin uses include alloys, tin plating, and solder for joining pipes and electronic circuits
- ***Gold*** uses include jewelry, as well as electronic, communications and aerospace equipment (provides superior electric conductivity and corrosion resistance)
- ***Wolframite*** is the metal ore used to produce tungsten; tungsten uses include metal wires, electrodes and contacts (lighting, electronic, electrical, heating, and welding applications)

* Any other mineral or its derivatives that the Secretary of State determines to be financing conflict in the DRC countries

Compliance Requirements

Any company that is required to file a Conflict Minerals Report (which will flow down through their entire supply chain) has to exercise due diligence on the source and chain of custody of its conflict minerals. All affected companies must file for a calendar year, regardless of their fiscal year end. They will be required to make their first filing on May 31, 2014, for the 2013 calendar year, and annually on May 31 for each calendar year thereafter.

Compliance to this legislation will be a daunting task as many businesses will find it extremely challenging to conduct the due diligence required to determine the origin of the conflict minerals. It will be critically important to develop a compliance strategy that will encompass both the current conflict minerals as well as any new regulatory additions.

The SEC has defined what the Conflict Minerals Report must contain, summarized below:

DRC Conflict Free: If a company determines that its products are "DRC conflict free," which means that the conflict minerals in those products may have originated from the *Covered Countries,* but did not finance or benefit armed groups in those countries, then the company has to:

- Describe in its Conflict Minerals Report the measures it has taken to exercise due diligence
- Obtain an independent private sector audit of its Conflict Minerals Report
- Certify that it obtained such an audit
- Include the audit report as part of the Conflict Minerals Report
- Identify the auditor

✓ ***Not DRC Conflict Free:*** If a company's products have not been found to be DRC conflict free, then the company, in addition to the requirements discussed above, has to describe in its Conflict Minerals Report:

- The products manufactured or contracted to be manufactured that have not been found to be DRC conflict free
- The facilities used to process the conflict minerals in those products
- The country of origin of the conflict minerals in those products
- The efforts to determine the mine or location of origin with the greatest possible specificity

✓ ***DRC Conflict Undeterminable:*** For a temporary two-year period for all companies and four-year period for smaller reporting companies, if the company is unable to determine whether the minerals in its products did not originate in the *Covered Countries* and came from recycled or scrap sources, or financed or benefited armed groups in those countries, then those products would be considered *DRC conflict undeterminable.* In that case, the company must describe the following in its Conflict Minerals Report:

- The measures it has taken to exercise due diligence

- Its products manufactured or contracted to be manufactured that are *DRC conflict undeterminable*
- The facilities used to process the conflict minerals in those products, if known
- The country of origin of the conflict minerals in those products, if known
- The efforts to determine the mine or location of origin with the greatest possible specificity
- The steps it has taken or will take, if any, since the end of the period covered in its most recent Conflict Minerals Report to mitigate the risk that its necessary conflict minerals benefit armed groups, including any steps to improve its due diligence

For those products that are *DRC conflict undeterminable,* the company is not required to obtain an independent private sector audit of the Conflict Minerals Report regarding the conflict minerals in those products.

Resources

IPC has put together an excellent resource website, which includes many tools and resource links for the electronics industry. The website provides an SEC Compliance Guide, Sample Supplier Letter, Conflict Minerals Seminar Proceedings and numerous external resource links. Other resources include:

- The adopting release for this rule and the disclosure forms can be found on the SEC's website
- Section 1502 of the Dodd-Frank Act
- The OECD Due Diligence Guidance
- The gold supplement to the OECD Due Diligence Guidance
- The GAO's Government Auditing Standards

Practical Impact

This will be a costly initiative to all U.S. manufacturing companies, but particularly to the small business that predominately make up the PCB industry. The IPC states "A survey conducted of IPC members indicated median due diligence burdens in excess of $65,000 (USD) per company in the first year. Additional estimated costs for tracking software, additional staff, training, legal expenses, and third party audits had a median total of $170,000 (USD)."

My personal belief is that these figures are extremely conservative; actual costs will soar past these levels in most companies once total costs are considered and factored. The timing couldn't be worse as job creators are being crushed by governmental taxes, regulations and rising health care costs. This legislation is like RoHS on steroids; another costly initiative that puts American manufacturing at a further disadvantage in the global economy. **PCB**

Steven Williams is the commodity manager for a large global EMS provider and author of the book Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean.

Most-Read PCB007 Supplier/ New Product Highlights This Month

Orbotech Unveils New PCB-AOI System

Orbotech Ltd., a leading global provider of yield-enhancing and production solutions for PCBs, has announced the introduction of its Discovery™ II automated optical inspection (AOI) series for bare PCB production.

WKK Joins Semblant's SPF Premier Partner Program

Semblant today announced the leading supplier of industrial equipment, materials and services in Asia, WKK, has joined its Semblant Plasma Finish (SPF) Premier Partner Program. WKK has partnered with Semblant to address growing demand for PCB surface finish advancements in Asia.

Holders Boosts Capacity; Acquires New Equipment

Holders Technology UK Ltd. has commissioned two Excellon EX300 drill\routers as part of their ongoing capital investment programme. The machines will double the existing capacity for tooling, allowing holders to offer enhanced production lead times. A new soft bed clamping system developed in-house for the Excellon equipment improves operator efficiency.

Ucamco Unveils Ucam 10.1

Ucamco has unveiled a new suite of CAM solutions. Ucam 10.1 delivers a range of new and enhanced tools and functions, unleashing unprecedented engineering software capabilities and allowing incoming data to be entered into production with greater ease, speed, and accuracy.

Aismalibar Enters IMS Market in North America

"We are excited to have a strong team in place for North America to deliver a quality product with excellent support," says Eduardo Benmayor, managing director at Aismalibar. "Our IMS-based copper clad laminates are industry leading in Europe and we aim to soon be a preferred supplier for North American OEMs and manufacturers."

Park Electrochemical Reports On-Year Sales Drop in Q3

Park Electrochemical Corp. reported net sales of $41,265,000 for the third quarter ended November 25, 2012 compared to net sales of $47,312,000 for the third quarter ended November 27, 2011. Park's net sales for the nine months ended November 25, 2012 were $133,741,000 compared to net sales of $149,578,000 for the nine months ended November 27, 2011.

Lackwerke Peters Donates to Children's Home

It was not by coincidence that the visit of Ralf Schwartz, managing director of Lackwerke Peters, to the Bulgarian customer SET, a PCB manufacturer and assembly company based in Rousse, was scheduled for the Christmas season, along with the second campaign of Lackwerke Peters to donate for a children's home in Brestovitsa.

Enthone Joins HDP User Group

Sean Mirshafiei, Enthone Vice President of Global PCB Marketing said, "As a Six Sigma company that employs sustainability practices on a daily basis, Enthone is pleased to participate in HDP User Group's environmental programs which include six projects focused on lead-free and halogen-free electronic materials."

GCT GmbH Posts 20% Sales Increase in 2012

GCT GmbH in Weingarten reported an on-year net sales increase of over 20% in 2012. The crucial factor was the strong demand for diamond-coated drills and routers for the mechanical processing of PCB (IMS) for power electronics.

CML Group Expands Offerings; Adds Test Chambers

The CML Group has a long-term target to monitor the processes in the production of partners proactively as well production materials for continuous improvements. The PCB reliability tests and the long-term PCB testing from different partner factories play an important role.

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COLUMN

Screen Printing Applications in Electronics—Part B

by Karl Dietz
KARL DIETZ CONSULTING, LLC

SUMMARY: Screen printing applications for fabrication and assembly of PCBs and electronic packages and devices vary, depending on use; this month, Karl's Tech Talk reviews the choices.

There are several screen printing applications in the fabrication and assembly of printed circuit boards and electronic packages and devices:

- Screen printing of non-photoimageable, UV-curable or thermo-curable ink through a screen that has been patterned with a photosensitive emulsion. The ink can be screened onto single-sided copper-clad laminate for print & etch circuitization, or as a plating resist for double-sided and multi-layer boards, or as a soldermask
- Screen printing of photoimageable liquid soldermask onto finished circuit boards. This operation can be double-sided in a vertical mode, or single-sided in a horizontal mode
- After soldermask application, so-called legend print is applied, typically by screen printing, more recently also by inkjetting. This white lettering on top of the typically green soldermask coating may contain information regarding lot numbers, date of manufacture, position markings for component mounting, component type, etc.
- In assembly, i.e., the mounting of active and passive components onto the board through solder joint connections, solder paste can be applied by screen or stencil printing
- B^2it process: multiple screen printing steps form cone-shape bumps with silver paste that serve as Z-axis interconnects in a coreless microvia HDI package
- Screen printing of conductors and via fill with thick film conductive pastes on LTCCs (low temperature, co-fired ceramics)
- Screen or stencil printing of conductive or non-conductive via fills in PCBs
- Screen printing of silver paste conductors on solar cells
- Screen printing of embedded capacitor and resistor structures in PCBs, modules and substrates

Let's take a closer look at screen printing of soldermask and legend print.

Soldermask

Historically, soldermask was a non-photoimageable ink that needed to be patterned onto the circuit board through a coated with a photosensitive emulsion exposed through a phototool and then developed. The soldermask ink was then squeegeed onto the board through the open areas of the screen, dried and cured. With the advent of the photoimageable, liquid-soldermask inks, the process changed. The ink was either applied by curtain coating, sequen-


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Figure 1: Vertical, double-sided soldermask screen printer. (source: Circuit Automation)

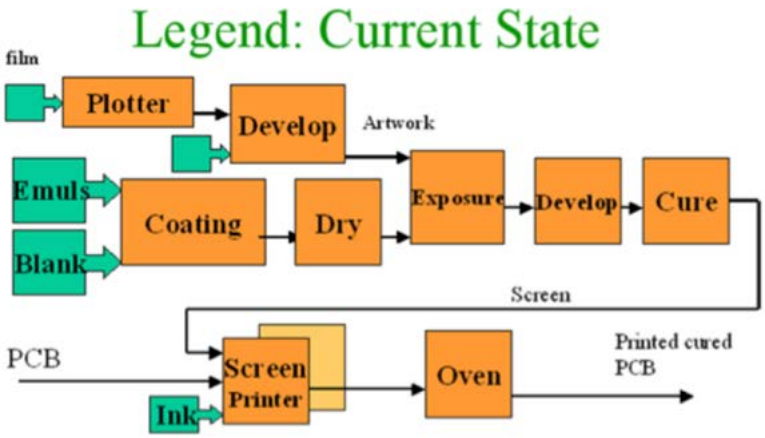

Figure 2: Process flow for conventional screen printing of legend. (source: Printar)

tially from both sides, or spray coated, or screen printed simultaneously from both sides. The screen coater was typically a double-sided, vertical blank (or flood) screen printer (Figure 1) that applied the soldermask ink in the desired uniform thickness, covering the entire board. Imaging followed in a photolithographic step, followed by development and curing. The most popular soldermask inks are two-component epoxy formulations, a resin and a curing agent, that are mixed before screen printing. After mixing, the ink has a limited shelf life. Curtain coating of soldermask ink was dominant in the early to mid-1980s and is still common in Europe, but not in the U.S. where screen printing is the norm. In Asia, we see all three application methods.

Screen printing of solder ink requires less solvent (thinner) than spray coating or curtain coating. Typical thinners for spray or curtain coating are propyleneglycol monomethylether acetate or propyleneglycol monomethyl ether (PM). There is a small amount of solvent in the resin, as supplied. Such solvents are typically carbitol acetate or dipropyleneglycol monomethylether. Development of screen printed soldermask inks is typically aqueous, i.e., an aqueous sodium carbonate solution, whereas curtain-coated inks may require a solvent such as butyrolactone. To clean the screens after printing, one used to employ chlorinated hydrocarbons, but that process has now switched to water-miscible solvents based on glycol ethers or acetates.

Legend Print

Legend refers to printed information, typically in white, on top of the typically green soldermask. The legend may contain information regarding lot numbers, date of manufacture,

Figure 3: Process flow for legend print by inkjetting. (source: Printar)

Most-Read PCBDesign007 News Highlights This Month

IPC Design Standard Tackles Technologies, Techniques

The newly revised IPC-2221B, "Generic Standard on Printed Board Design," provides a basis for the design of all types of printed boards and addresses areas as diverse as testing, via protection, test coupon designs and surface finishes.

Bus Maker Alexander Dennis Selects Zuken's E3.series

Alexander Dennis Limited, Britain's largest bus and coach manufacturer, has adopted Zuken's leading electrical and fluid CAD software, the E3. series. The software will enhance the accuracy, consistency and availability of the firm's data, helping them meet the future challenges of competitive product development and manufacturing.

Ucamco Unveils Ucam 10.1

Ucamco has unveiled a new suite of CAM solutions. Ucam 10.1 delivers a range of new and enhanced tools and functions, unleashing unprecedented engineering software capabilities and allowing incoming data to be entered into production with greater ease, speed, and accuracy.

Intercept Celebrates its 30th Anniversary

Founded in 1983, Intercept began as a consulting firm performing electrical engineering-related software and hardware projects. During the company's first 10 years, the issues with CAE and CAD software were so apparent that the firm began developing its own EDA software. Pantheon PCB design software was first released to the public in 1994, and quickly became a success in the EDA market.

PCB Design Software Market Shows CAGR of 5.3%

The global PCB design software market has witnessed an increasing availability of cloud-based PCB design software. However, the availability of open-source PCB design software could present a challenge to the growth of this market.

EDA Consortium: PCB & MCM Revenue Up 9% in Q3

EDA Consortium's Market Statistics Service reports that EDA industry revenue increased 4.9% for Q3 2012 to $1.62 billion, compared to $1.54 billion in Q3 2011. PCB and MCM revenue of $153.0 million represents an increase of 9% compared to Q3 2011. The four-quarters moving average for PCB & MCM decreased 1.7%.

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position markings for component mounting, component type, etc. Military PCBs typically specify epoxy-based ink formulations. There has been an ongoing debate about the need for legend print, but this has not changed the reality that it is still alive and well. Most legend is screen printed with non-photoimageable inks, i.e., they require a patterned screen. Figure 2 outlines the rather involved processing sequence for such an application. This process still has the aura of an art form, and screen printers are sometimes viewed as the last prima donnas in the industry. In today's digital environment, they appear to be losing ground to a new, much simpler legend print process based on inkjetting, as shown in Figure 3. There is no lead time for phototool preparation and screen patterning. The legend information can be digitally changed, even from board to board, if needed. Yet, the printing process is slower compared to screen printing so that early applications favor prototyping and small lot manufacturing, just like laser direct imaging (LDI) found its early adoptions in these applications. **PCB**

Karl Dietz is president of Karl Dietz Consulting LLC, offering consulting services and tutorials in the field of circuit board and substrate fabrication technology. Dietz can be reached by e-mail at karldietz@earthlink.net or phone (001) 919 870 6230.

Most-Read PCB007 News Highlights This Month

① Exception's PCB Solutions Business Acquired by Fastprint

Qiu Xingya, chairman of Fastprint, says, "This acquisition will help Fastprint establish a strong base in Europe for both manufacturing and trading. Post-acquisition, we will continue to invest in PCB manufacturing to maintain, as well as enhance, the market-leading position in Europe in terms of quality and speed."

② Global PCB Market to Reach $68.5B in 2016

Asia growth will be sustained mainly by domestic demand but will nevertheless experience a very respectable average annual growth of a little less than 5% in 2013 before picking up in 2015 resulting in a growth rate of between 6% and 7% for China between 2011 and 2016. Global PCB market value will increase from $56.6 billion in 2011 to $68.5 billion in 2016 meaning China's share of PCB production will increase further from 45% to 51%.

③ N.A. PCB Industry Reports Negative November Results

Rigid PCB shipments were down 5.4% in November 2012 from November 2011, and bookings decreased 8.7% year over year. Year to date, rigid PCB shipments declined 4.5% and bookings decreased 0.9%. Compared to the previous month, rigid PCB shipments were down 5.6% and rigid bookings fell 2.1%. The book-to-bill ratio for the North American rigid PCB industry in November 2012 fell to 0.95.

④ TTM Partners in EU Optical Transmission Technologies

TTM Technologies, Inc. is partnering in a development project of optical data transmission technologies sponsored by the European Union. The EU is providing EUR 9 million funding for the four-year project, which began in October 2012 under the name PhoxTroT.

5 Sunstone Circuits Reveals "Share Your Story" Winners

"I took part in the contest because circuit boards are a big part of my life. As an electrical engineer, there are few things as satisfying as seeing and bringing to life something you've designed. For me, that's a circuit board." – Clive Bolton, Andover, MA.

6 IPC Releases Annual Report; Much Accomplished in 2012

Last year proved to be a year of modest growth for the electronic interconnect industry. It was also a year filled with innovative standards development, a flurry of environmental and governmental legislation, global activity expansion, membership service initiatives, and more.

7 IPC Strengthens Support for Chinese Manufacturers

China's rise as a manufacturing powerhouse is one of the inescapable factors in any analysis of the electronics industry. With a powerhouse of its own, new IPC China President Philip S. Carmichael, IPC is beefing up its efforts to help Chinese manufacturers come into alignment with other global companies that employ IPC standards to improve business plans and manufacturing capabilities.

8 Q.P.I. Group Acquires Macer Sweden AB

The Helmond based company Q.P.I. Group Holding B.V. has acquired the Swedish company Macer Sweden AB, which specialises in the supply of printed circuit boards and in DFM (Design For Manufacturing).

9 Invotec Appoints Mark Sykes Sales Account Manager

Matt Bowman, sales director, commented, "We are delighted to announce the appointment of Mark Sykes as account manager, focusing on building on our client base in the Southern region. Mark brings plenty of experience and the drive our clients demand."

10 Spirit Circuits Appoints Harzendetter as Sales Agent

Spirit Circuits has appointed a new sales agent Rupert Harzendetter to handle operations in Germany.

For the latest PCB news and information, visit: PCB007.com

Social Media: It's Nothing New...or Is It?

by Barry Matties
I-CONNECT007

I was told recently that I sounded like an "old man" during a discussion on social media. The name-calling happened when I shared a comment from a friend who told me she values social media as important because she can better keep in touch with friends and family; get updates from her favorite companies about specials and discounts; learn about activities happening each weekend at the local farmers' market; and even win free dog treats from a dog food company. If agreeing with and sharing the view of a 30-something-year-old friend makes me sound like an old man, so be it.

The conversation I was engaged in wasn't about whether or not social media has a place, though I believe that's how my friends viewed it. I believe it does. However, I'm looking at it differently. I see social media as the new venue for doing what we have done for thousands of years—communicate messages. And when it comes to messages, everyone seems to have one these days. The nice thing about social media is just that—it's social. We are just getting hung up on naming the activity and the delivery tools. I think what we are really witnessing is mass media in its most explosive state. The rules are still being defined while people continue to learn new ways to express themselves.

The outlet for messages in the past were available only to those with access to the news media, billboards, TV networks, cable TV, radio, newspapers, magazines, newsletters, speeches, chain letters, etc. Now, everyone has immediate access to tools that will broadcast their message to anyone who will listen or read. Dog food companies to their customers, rock stars to their fans, a politician to his base—the messages go to whomever cares what you may have to say… and even to those who might not care at all. But the real strength, right now, is for those who need to reach a broader group. And the broader the target market, the more effective social media becomes.

My social media discussion really just revolved around a tendency to confuse social media with B2B marketing. The basic concept I was sharing is that no matter what you call it—social media, tweeting, posting, blogging, advertising, connecting, Facebooking, circles, spheres, groups, forums, friends, etc.—strength in B2B marketing is found in efficiently focusing on a specific community. Many different communities make up our life—work, friends, family, sports, religion, politics, hobbies—and we all like to share our opinions, comments, or insights with a like-minded group of people.

What's happening now is a rush to social media, everywhere. Do you remember when the Internet really started catching on? Okay, now I do sound old, but back then everyone was rushing to be a part of this new community. Millions of dollars were made, and then lost, on Internet

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The Semiconductor Thermal Measurement and Management Symposium is an international forum dedicated to the thermal design and characterization of electronic components and systems. The symposium fosters the exchange of knowledge between practitioners and leading experts from industry, as well as the exchange of information on the latest academic and industrial advances in electronics thermal management. We encourage you to report on your latest modeling, designs, and results.

New for 2013!

Thermal Management Executive Briefing: Thermal Management Market Visions & Strategies
Monday, March 18
Presented in association with MEPTEC and Electronics Cooling Magazine

Where in the market are the opportunities, directions and challenges that will be created over the next few years? SEMI-THERM aims to answer that question and provide exclusive market and technology insight at this new event. With nearly thirty years of direct industry involvement and its long-time location in Silicon Valley, SEMI-THERM is perfectly poised to offer this new information stream to the industry.

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  Tuesday, March 19 – Microfluidic Thermal Management and Thermal-Electronic Co-Design for Chip Stacks

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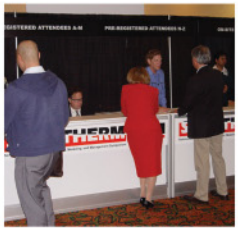

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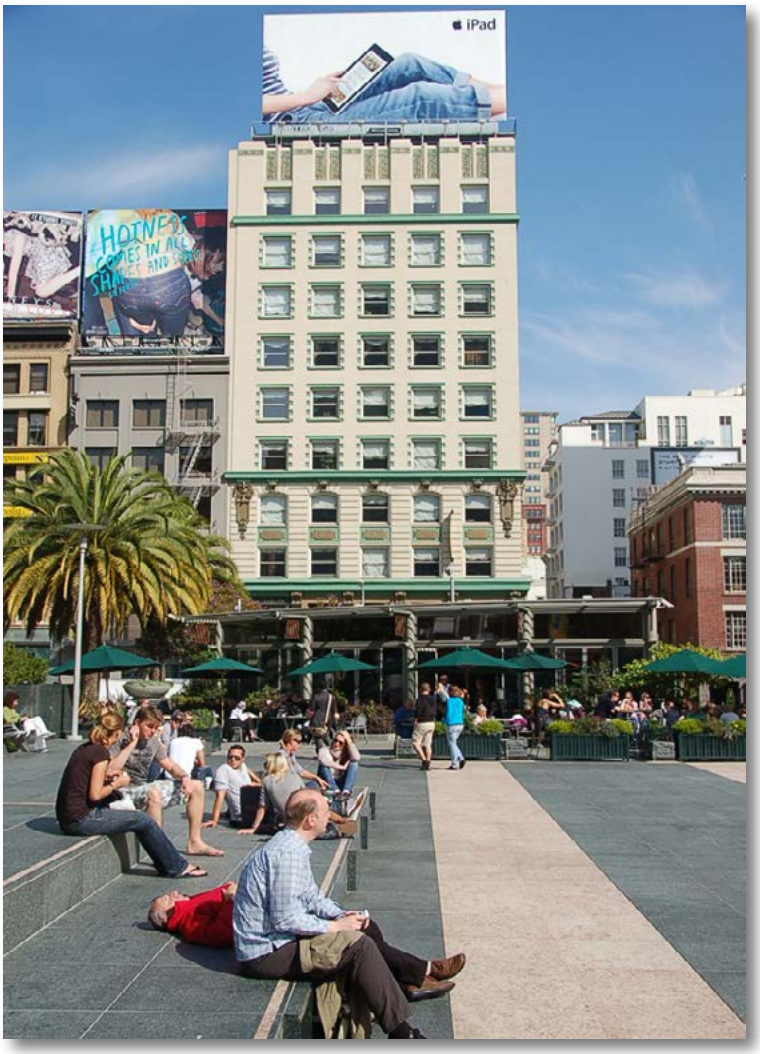
start-ups. As Alan Greenspan said, an "irrational exuberance" lead to a huge bubble that eventually popped. Is social media following that same path? Perhaps, to a degree, but I think the fallout will be less monetary and more social.



The ultimate goal of social media is to get a message to a target audience in the most efficient way possible. When it comes to niche market B2B, advertising during the Super Bowl or purchasing a billboard along a highway may not be the best use of your resources. So, what's the answer? When you are looking to market to a particular community, find out where the community already exists and get your message there. Where do you find the communities? Trade journals are a good place to start...and it's not just advertising, it's positioning yourself in a market in a way that allows you to gain market share.

Trade publications focus relevant and valuable information to an established community. If you want to blog, post your blog in an industry publication that already has the attention of the right community. If you want direct connections to the audience, invite them to subscribe to your blog. Once they subscribe you will have direct contact with them. The point I'm making here is to start your efforts in the place where the community already exists.

Become a columnist to share your expertise with the industry. If your message is so important that a magazine invites you to be a columnist, that brings a higher level a credibility to you and your message, compared to just a posting on a social media site. If you want to introduce a new product, submit press releases where your target market goes to get industry information. It streamlines the process for you, and when potential customers read the press release they are in the right frame of mind.

Social media marketing isn't limited to texting or status updates; it's also about people communicating in person. Trade shows, an assembly area for your community, are a great place to share your message. But keep in mind that trade shows offer much more than just a place to exhibit. Become a speaker, chair a session, or take part in technical discussions. Be a part of the content. Remember, it's not the size of your booth that matters, it's how you connect with your target community and how they connect with you.

An argument was made during my social media discussion that by using social media sites you can conduct surveys. That's true, but you have to first develop a network (target customers) that fits into the circle, sphere, group, or whatever you call it. Only then will you have a base upon which to draw. I shared with my friends that a smart company—smart because they know how to tap into a community with little effort on their part—looking for detailed market information asked us to conduct a sur-

vey for them. Within days we provided over 500 detailed responses to their questions. The results we acquired came from the exact target market the company was looking for and was not limited to companies with which they already had relationships, or as some might call them, the company's "circle of friends." Not only did it give them important market intelligence, but it also gave them direct leads.

It's not whether or not social media is good, bad, or here to stay; it's about focusing on your community and delivering your message. Social media is nothing new; it's been around for thousands of years. The difference now is that new outlets allow any person to have an immediate voice and be relevant.

I'm not saying the new media outlets don't play a part in your marketing. In fact, I think they do. But I would say be smart about it and start by going where the community already assembles and grow from there.

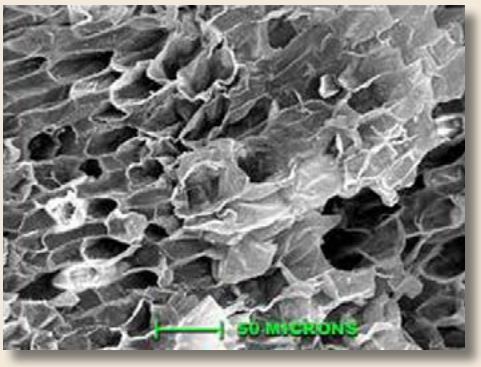
So, if telling people they should focus their message to the right market makes me sound like an old man, I am okay with that. I've also been told there is no substitute for experience. When experience makes you sound old, well, I take it as a compliment. **PCB**

Barry Matties is the publisher of the I-Connect007 family of publications. He started in PCB manufacturing in the early 1980s and in 1987 became a founder of CircuiTree Magazine, which sold nearly 13 years later as the leading industry publication. In the early 2000s, Barry and longtime business partner Ray Rasmussen joined forces again and acquired PCB007 and launched the I-Connect007 family of publications. Later, in July 2010, SMT Magazine and SMT China were also acquired by I-Connect007. With his proven successful business development and leadership skills, Barry now produces this column relating over 25 years of successful business experience, including business, marketing and selling strategies that really work. Contact Barry here.

Mirroring Cork Structure May Unlock the Potential of Graphene

Published in Nature Communications, a Monash University study led by Professor Dan Li has established an effective way of forming graphene, which normally exists in very thin layers, into useful three-dimensional (3D) forms by mirroring the structure of cork. The process may revolutionise fields from computers and batteries to composite materials.

Graphene is formed when graphite is broken down into layers one atom thick. In this form, it is very strong, chemically stable, and an excellent conductor of electricity. It has a wide range of potential applications, from batteries that are able to recharge in a matter of seconds, to biological tissue scaffolds for use in organ transplant and even regeneration.



Professor Li, from the Department of Materials Engineering, said previous research had focused mainly on the intrinsic properties and applications of the individual sheets, while his team tackled the challenge of engineering the sheets into macroscopically-useable 3D structures.

"When the atomic graphene sheets are assembled together to form 3D structures, they normally end up with porous monoliths that are brittle and perform poorly," Professor Li said. "It was generally thought to be highly unlikely that graphene could be engineered into a form that was elastic, which means it recovers well from stress or pressure."

The researchers used cork, which is lightweight yet strong, as a model to overcome this challenge.

PhD student, Ling Qiu, also from the Department of Materials Engineering, said, "The fibres in cork cell walls are closely packed to maximise strength and individual cells connect in a honeycomb structure which makes the material very elastic."

EVENTS

- **IPC Complete Calendar of Events**
- **SMTA Calendar of Events**
- **iNEMI Calendar**
- **PCB007 Online Events**

SPIE Photonics West 2013
February 2-7, 2013
San Francisco, California, USA

6th Annual Mobile Deployable Communications
February 7-8, 2013
Amsterdam, Netherlands

Medical Design & Manufacturing
February 11-14, 2013
Anaheim, California, USA

Electronics Manufacturing Korea 2013
February 13-15, 2013
Seoul, Korea

IPC APEX EXPO® Conference & Exhibition 2013
February 19-21, 2013
San Diego, California, USA

CMSE - Components for Mil & Space
February 20-21, 2013
Los Angeles, California, USA

Embedded World
February 26-28, 2013
Nurnberg, Germany

MEDTEC Europe
February 26-28, 2013
Stuttgart, Germany

IEEE CPMT Advanced Pkg Material
February 27 - March 1, 2013
Irvine, California, USA

Medical Devices Summit
February 28 - March 1, 2013
Boston, Massachusetts, USA

Economic Retreat
March 7-9, 2013
Snowmass, Colorado, USA

29th Annual SEMI-THERM Expo and Conference
March 17-21, 2013
San Jose, California, USA

Executive Briefing: Thermal Management Market Vision & Strategies
March 18, 2013
San Jose, California, USA

SOLARCON China 2013
March 19-21, 2013.
Shanghai, China

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ADVERTISER INDEX

Next Month in *The PCB Magazine:* Materials

Printed circuit materials must satisfy many physical, mechanical, thermal and electrical requirements. With the enormous range of laminates available, what considerations determine the selection of an appropriate material for a particular application? What are the latest advances in the technology of dielectric materials and copper foils, and how can the designer best exploit them to meet performance demands? Find out in the March issue of *The PCB Magazine.*