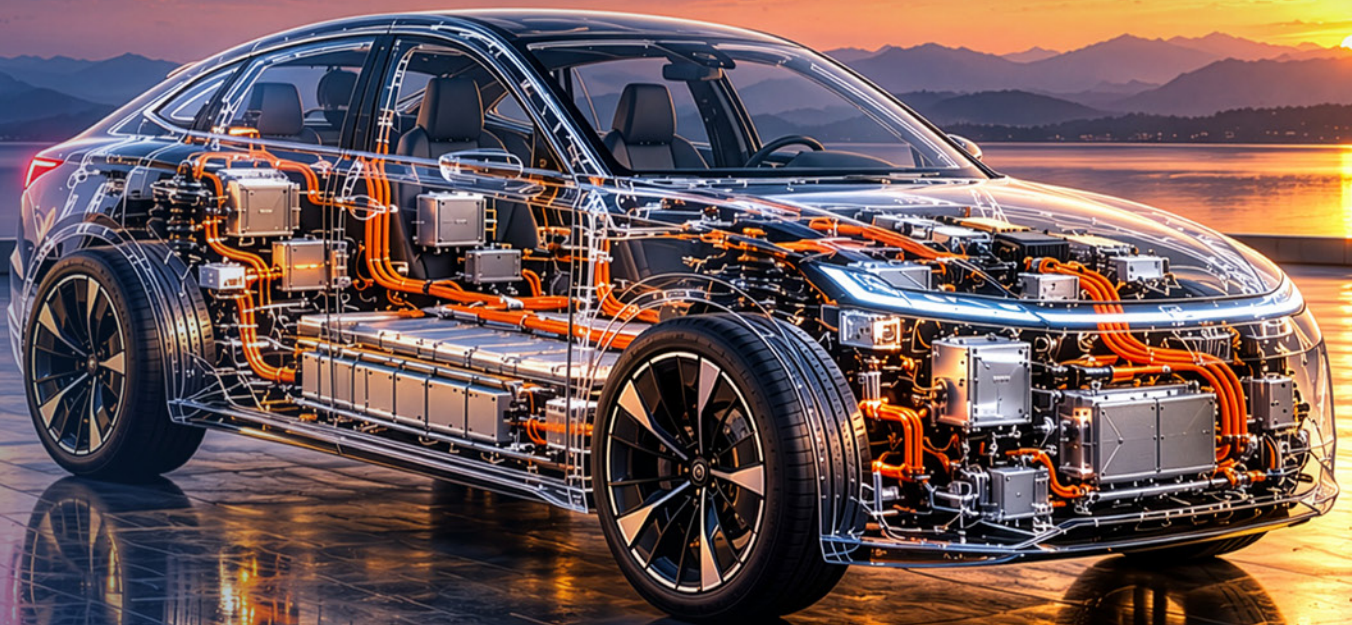


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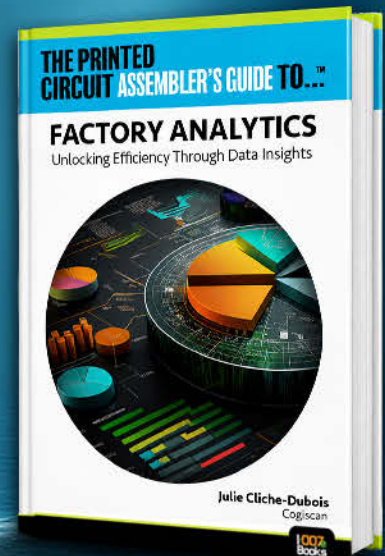
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Automotive: Building in Reliability

Automotive electronics demand reliable assembly at an extraordinary scale. This issue examines how soldering technologies and process controls are evolving to meet those requirements, from reflow and laser soldering to silver management, BGA warpage, voiding, power board testing, and insights from experts focused on the road to reliability in automotive assembly.

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Automotive Is Gearing Up Again



BY NOLAN JOHNSON, I-CONNECT007

In 2009, I bought a new car from the dealer, something a bit unusual for me, as I've tended to pick up a desirable, durable used car rather than betting on the reliability and panache of the latest model. Of the 12 vehicles I've purchased, only four were brand new. But back then, I needed something reliable to haul my family and all their stuff to meet the bus, get groceries, and go on the occasional weeklong camping trip.

I finally settled on a Honda Odyssey. While pitching the add-on warranty programs, the sales manager warned me that "things could go wrong." How could I dispute his claim? I didn't have any data readily available to question him. Now, however, with my favorite AI tool, I've been able to fact-check that sales

manager. How reliable was the Honda Odyssey?

According to Honda and NASA: "A well-equipped 2009 Honda Odyssey had more electronic control units than the Space Shuttle had general-purpose flight computers, but not necessarily more processors than the Shuttle's entire avionics system."

The electronics in cars in 2009 were quite advanced, but they seem pretty primitive in 2026. Consider Tesla. Measured in trillions of operations per second (TOPS), Tesla's HW3 computer delivers about 144 TOPS. By comparison, the Space Shuttle carried five general-purpose computers. During critical phases of flight, four operated simultaneously as a redundant set, while a fifth provided an independent backup. Even the upgraded Shuttle



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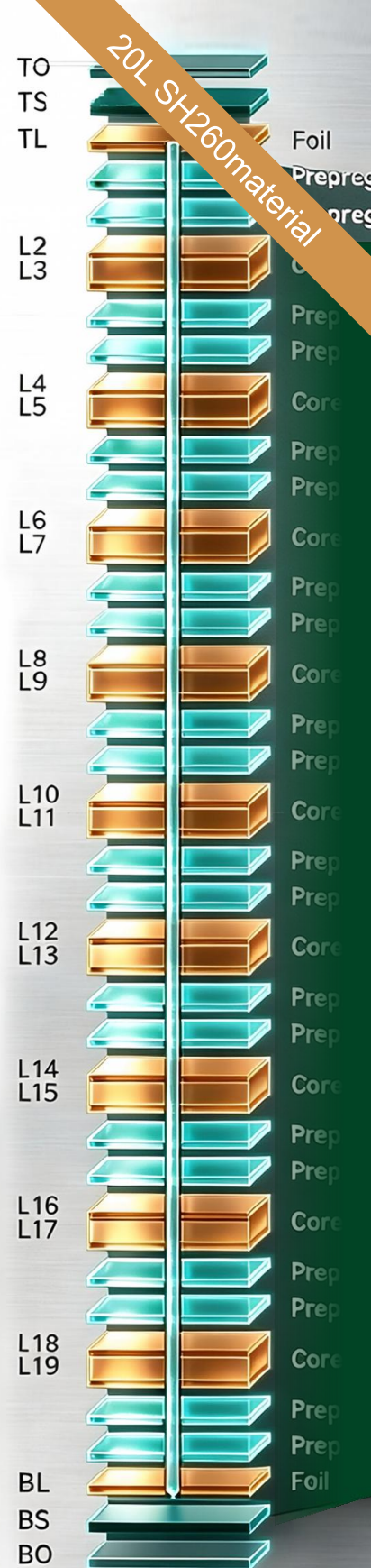
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computers processed only about 1.3 million instructions per second. Although TOPS and instructions per second are not directly equivalent measures, the comparison illustrates the enormous capability available in today's vehicles.



This car has more computers than the Space Shuttle! That's why this extended warranty is a good deal."

— Honda sales manager

The same progression can be seen in consumer electronics. Apple's iPhone 12, introduced in 2020, incorporated a Neural Engine capable of 11 trillion operations per second. We've come a long, long way.

Now consider production volumes. The automotive industry produces close to 100 million vehicles annually, and electric vehicles represent a rapidly growing share. If 25 million EVs each contain roughly 100 circuit boards, including boards in cameras, sensors, lighting, airbags, and other subsystems, that alone represents 2.5 billion PCBs. Even allowing for variations in PCB counts from one vehicle architecture to another, the shift toward electrification and electronic vehicles represents an enormous market for circuit boards.

As more EVs are produced, we will see increased demand for circuit boards, and safety regulations are only adding to the electronics required to run our modern vehicles. AI and data centers may be gobbling up much of the demand for boards, but automotive remains a major volume driver.

Of course, billions of boards are only part of the challenge. They also have to be assembled reliably, efficiently, and at automotive production volumes. The automotive industry has been advancing its electronics technology for many years and those demands continue to influence electronics manufacturing. In this issue of SMT007 Magazine, we

look specifically at soldering and how recent developments are helping manufacturers meet the automotive industry's evolving requirements.

In my interview with KIC's Miles Moreau, he discusses reflow oven controls for reliability. I also explore lasers as a soldering option in a separate article. MacDermid Alpha Electronics Solutions presents a case study on managing silver in production, which is very timely, given silver's recent volatility. In another article, Akrometrix advises us on alternative methods to check BGAs for warpage. We're publishing an Indium paper from SMTA International on voiding, and SPEA tackles automotive power board testing. Closing out our features is an interview with Stan Rak, author of this year's article series called "The Road to Reliability."

In columns this month, Jennie Hwang sends a letter to future generations, FSQuality's Tianming Liu examines the concept of core competencies across regions, and Nash Bell discusses the value of interposers in rework.

I'm excited to welcome our newest columnist, Adam Klett, doctor of science at KYZEN. Adam was one of our contributing experts on the cleaning issue earlier this year, and we're delighted to have him join us as a columnist.

Returning to my analogy of the reliability of new cars, I leaned on the automotive industry's relentless pursuit of reliability even then, and asked the sales manager, "Are you suggesting that my Honda will be as fragile as the Space Shuttle? Will I have to scrub trips on the regular because of electronic failures? If so, I don't think this is the minivan for us." He assured me all would be well, so we moved on to signing paperwork. And 100,000 miles of driving proved him right. Now, if the sales manager been talking about a "2001 Odyssey," and had he mentioned that one of the modules was named HAL, I might have fallen for it. **SMT007**



Nolan Johnson is managing editor of *SMT007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To contact Johnson, [click here](#).

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What I Hope the *Next Generation* Will Carry Forward

BY DR. JENNIE S. HWANG, H-TECHNOLOGIES GROUP

As parents and grandparents, we often wonder what we can give the next generation that will matter long after the gifts have been opened and the celebrations have passed. When a child leaves for college, this occasion naturally invites reflection. The older I become, the more I realize that the most meaningful things we can pass on are not possessions, accomplishments, or even answers. I want to offer encouragement, perhaps a few words of wisdom, and some lessons that life has taught me. These are perspectives, ways of thinking, choices to consider, and principles to carry through an ever-changing world.

Recently, I wrote a personal note to my very first college-bound grandson with a few observations gathered not from textbooks but from decades of living, working, leading, succeeding, making mistakes, and watching and coping with the world as it changes. I intentionally tried to avoid the familiar clichés of advice and instead focus on things I have

come to believe are genuinely useful and real.

As I reread that note, I thought it might resonate beyond our family, as many of us are experiencing similar situations as our children and grandchildren enter college, begin careers, or find their way in this complex world. The technologies, careers, and circumstances of life certainly will change, especially with AI, but some principles remain remarkably durable.

So, I share these thoughts as one generation speaking to another. Perhaps it will prompt reflection, some discussion around the dinner table, or simply a smile of recognition. After all, one of the privileges of getting older is having accumulated enough experience to know that we cannot choose the path for those who follow us. We can, however, offer a few signposts along the way.

Here is my note to my first college-bound grandson, who seems to have grown to 6-foot-3 almost overnight.

Bobby



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A Note to My College-Bound Grandson

Bobby,

As you prepare for this exciting new chapter of life, in addition to a college send-off/dorm-move-in gift, I would like to leave you with a few thoughts and observations gathered from life and experience that may serve you well in the years ahead. These are not clichés, but real things, and high-value lessons that have proven true over time.

1. Stay away from unhealthy habits.

Avoid smoking, drinking, drugs, and other destructive behaviors. Your health, energy, and clarity of mind are among your greatest assets. Protect them.

2. Choose your company wisely.

Surround yourself with ambitious, forward-thinking, positive people. The friends and classmates with whom you spend your time will influence your thinking, aspirations, habits, and ultimately your future.

3. Remain disciplined in your core mission to learn.

College is an opportunity to develop your mind. Be diligent in your studies (Family offers cash award for grade A), intellectually curious, willing to take on leadership roles, and committed to excellence. The knowledge, skills, and habits you build now will serve you for a lifetime.

4. Use money wisely.

Save and invest, and change your consumption habits from buying things to experiencing things.

That mindset will help you take advantage of the uniqueness of this period in one's life. Learn the value of financial discipline early. Save consistently, spend thoughtfully, and invest as much as practical. Early gratification is not a virtue. It's like premature harvesting; you don't get good crops. Time is one of the greatest advantages a young person has when building financial security and wherewithal. Money makes money!

5. Nurture your relationships, make time to communicate, and build lifelong mentors.

- Be mindful of your personal and professional relationships. Build meaningful connections and seek mentors who can guide, challenge, inspire you, and offer honest feedback.
- Leave an impression by being fully engaged in whatever you do, whether it's a big task or a small chore. People are surprisingly more observant and perceptive than we realize, albeit tacitly.
- Never underestimate the value of helping someone in need; kindness has a remarkable way of enriching both the giver and the recipient.
- Develop a reputation for being dependable and reasonably accommodating, not merely focused on your own likes.
- Reply to messages, emails, and communications promptly and consistently. People remember those who are responsive, consistent, and reliable.
- Be a gentleman!

You are an intelligent, capable, and handsome young man with tremendous opportunities ahead of you. Talent alone, however, is never enough. Hard work is absolutely indispensable. Saying the outcome/success is directly proportional to the hours you work on it is not an exaggeration, but like a mathematical equation:

$$S = C \times H$$

where

S= success or positive outcome

H=number of hours spent

C=coefficient, which can be multiple parameters, e.g., E (Effort) + E (External factors)

We are immensely proud of you and look forward to watching you grow, contribute, and thrive in the years ahead. Have a great start in college, Bobby!

With love, NaiNai

Your Preparation for Life

Prepare for college, but even more importantly, prepare for life. A college education can provide knowledge, skills, credentials, and opportunities; however, character, judgment, discipline, integrity, and compassion ultimately determine how far those opportunities will carry a person. The years ahead will undoubtedly bring extraordinary technological advances, new professions, and challenges we may not foresee. Yet the fundamentals of a meaningful and successful life are unlikely to change: a sound mind and body, a commitment to learning, wise choices, financial prudence, strong relationships, respect for others, a willingness to work hard, and a desire to contribute beyond oneself.



The years ahead will undoubtedly bring extraordinary technological advances, new professions, and challenges we may not foresee.”

We cannot, nor should we, walk the journey for the next generation. Their future will be theirs to shape. We can share the lessons learned through our own triumphs and setbacks, offer guidance without imposing it, and provide encouragement.

If, along the way, a few of our experiences help them avoid unnecessary detours, seize worthy opportunities, or navigate life's inevitable crossroads with greater confidence and wisdom, then we have contributed something of lasting value.

Ultimately, every generation inherits a world it did not create and leaves behind a world it has helped shape. My hope is that we pass forward not only knowledge and resources, but also values, perspective, resilience, and a sense of responsibility toward others. If we do that well, then our legacy will not be measured by what we leave behind, but by what those who follow us carry forward. **SMT007**

Upcoming Appearances

Dr. Jennie Hwang will present a lecture on “Artificial Intelligence & AI-Powered Future Manufacturing” on Oct. 27, and on “Mastering Intermetallics for Reliable Electronics” on Oct. 26, at SMTA International 2026 in Chicago.



Dr. Jennie S. Hwang, an international businesswoman, speaker, and business and technology advisor, is a pioneer and long-standing leader in SMT manufacturing since its inception, and in developing and implementing lead-free electronics technology and manufacturing.

She has served as chair of Artificial Intelligence-Justified Confidence for DoD Command and Control study, chair of AI Committee of the National Academies, and Review Panels of NSF National AI Institutes and Committee of Strategic Thinking for Engineering Research. An International Hall of Famer (Women in Technology), she has been inducted into the National Academy of Engineering, named an R&D-Stars-to-Watch, and received the YWCA Achievement Award. She has held senior executive positions with Lockheed Martin Corp., and was CEO of International Electronic Materials Corp. She is currently CEO of H-Technologies Group, providing business, technology, and manufacturing solutions.

She has served as chair of the Laboratory Assessment Board, the DoD Army Research Laboratory Assessment Board, and the Assessment Board of Army Engineering Centers. She is on the board of Fortune-500 NYSE companies and civic and university boards, Commerce Department's Export Council, National Materials and Manufacturing Board, NIST Assessment Board, various national panels/committees, and international leadership positions.

She is the author of 10 books (four as co-author) and 750+ technical/editorial publications. She is a speaker and author on trade, business, and education issues. Her formal education includes four academic degrees (Ph.D., M.S., M.A., B.S.), as well as Harvard Business School Executive Program and Columbia University Corporate Governance Program. To read previous columns, [click here](#).



Stan Rak's *Road to Reliability* Continues

Dr. Stanton Rak spent the better part of this past year taking readers inside the electronic systems that enable electrification through his “Road to Reliability” series, to find out what it takes to make them reliable. Now that the series has concluded, he explains his motives for writing it, his holistic approach to covering EV reliability, and how it can become an important technology driver for high reliability electronics more broadly.

Nolan Johnson: Stan, your series has been a fantastic read, I have to say. Now that it has concluded, I'd like to look back and discuss it. Please summarize the series and what you set about to accomplish.

Stan Rak: In the series, I wanted to take readers inside the electronic systems that make electrification possible and ask what it takes to make those systems reliable over the life of the vehicle, rather



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than focusing primarily on batteries, range, and vehicle performance, like many publications do. I want to acknowledge the invaluable help I received from Tracy Riggan at the Global Electronics Association, who kept this train on the rails, so to speak. We started this series with an overview of the EV landscape and then moved through power electronics, vehicle controls, high-voltage auxiliary systems, ADAS and connectivity, charging infrastructure, and the materials and manufacturing technologies behind them.

The final article brought those topics together through field failures, monitoring, qualification, and standards. You can certainly choose an individual article that interests you, but when you read the series as a whole, I think you begin to see how interconnected EV reliability really is.

That was a major takeaway for me: the holistic approach you applied to the entire system, looking at the car not as a bunch of subsystems but as a whole, and discussing how that interaction made a huge difference in identifying the design and power management challenges that we face in an electric vehicle.

Thank you for saying that. I saw a gap between the tremendous attention being given to EV innovation and the little attention paid to the long-term reliability of the electronics that make that innovation possible. We hear a great deal about battery range, charging speed, high voltage architectures, autonomous features, and software-defined vehicles. But every one of those advances places additional demands on electronic components, materials, interconnects, PCB assemblies, and manufacturing processes; all things that SMT007 readers are interested in.

My background has been in automotive electronics materials, manufacturing, and reliability, so I wanted to look at electrification from that perspective. I also thought this series was particularly relevant to the SMT007 audience because many of the answers ultimately come back to what this industry knows very well: material selection, PCB design,



Stan
Rak

soldering, cleanliness, coatings, interconnects, process control, testing, and failure analysis.

EVs may be changing operating conditions, but electronics manufacturers already possess much of the knowledge needed to address the reliability challenge they face.

The key drivers of our development in the industry are AI/data centers and vehicles of all types, especially when you consider infotainment systems, safety sensors, and the like. So, overcoming environmental extremes and long-term usage is a huge challenge. How does a design team respond to that, and do you see those responses trickling down into other sectors, not just automotive?

I don't think EV reliability will be isolated at all. In fact, some of that technology transfer is already going in both directions. The automotive industry has historically learned from aerospace, industrial, telecommunications, and other high-reliability sectors. EVs are now creating their own demanding reliability proving ground because they combine high voltage, high power, harsh environments, advanced electronics, connectivity, software, and very high production volumes, all under immense cost and safety pressures.

The lessons learned in wide-bandgap power electronics, high-voltage insulation, thermal management, contamination control, predictive maintenance, advanced interconnects, and accelerated testing can translate to renewable energy storage, industrial power electronics, aerospace, data centers, robotics, and other high-power electronic systems.

So, rather than EV reliability existing as a specialized branch of automotive engineering, it can become an important technology driver for high reliability electronics more broadly.

This is truly a paradigm shift in the automotive industry. Traditionally, electronics and automotive followed the other sectors I mentioned, with years of work devoted to understanding the reliability of new components in other industries before automotive had an opportunity to work with them.

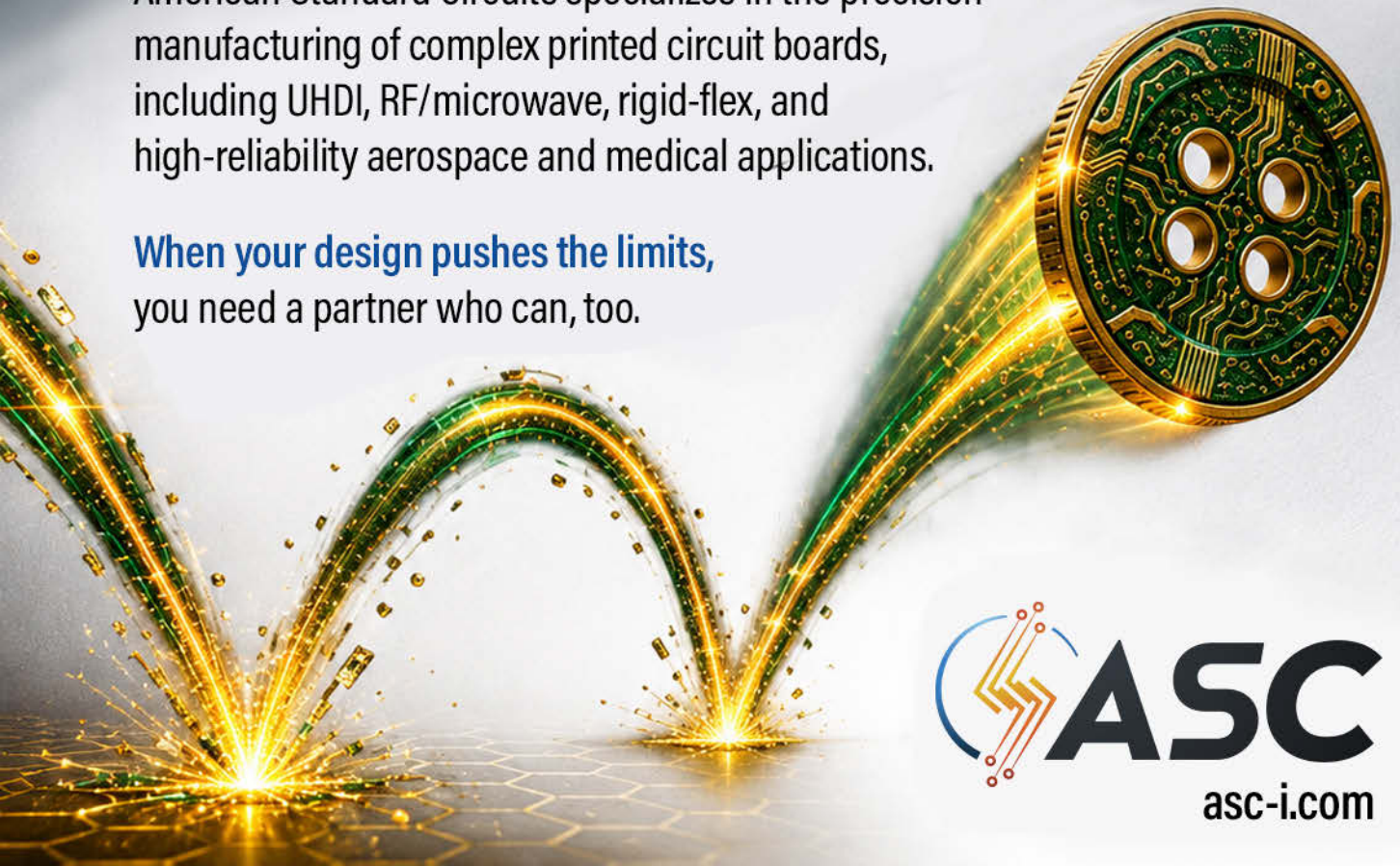
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But now, in many cases, automotive is at the forefront of those changes, and other industries, like data centers, are borrowing some of what's being learned from the EV world.

I can easily imagine data center designers looking to current automotive technologies to better understand how to manage heat, just as an example.

That's always been a challenge for the automotive industry. It's not only the operation of the electronics; sometimes the electronics are adjacent to the engine or other assemblies that produce very high heat.

What we're seeing, especially in power electronics, where fast switching is occurring in power dies, is that new 800-volt architectures are being employed by the EV industry. Those architectures are now also being considered by data centers, which are using a similar approach to design power electronics, power die stacks, and cooling solutions. These similar approaches could create synergies for the automotive industry with other industries like data centers.

What are the implications for electronics manufacturing long term, based on what's developing in EVs and how that's trickling out into the rest of the industry?

One long-term implication is that the process window for acceptable variation will become tighter. Higher voltage, higher power density, faster switching, smaller packaging, and longer expected service life can turn what once seemed like a minor manufacturing variation into a long-term reliability issue.

So, topics we're familiar with, like ionic cleanliness, solder joint quality, coating coverage, insulation spacing, material compatibility, voiding in interconnects, thermal interfaces, and process consistency, all take on a greater significance. At 800 volts, for example, contamination or insulation weaknesses that may have been tolerated in lower voltage electronics can become much more consequential.

I also think manufacturing will become increasingly data-driven. Inspection tells us whether an assembly meets requirements today. The larger reliability question is whether we understand the

materials and process variables that determine how that assembly will perform five, 10, or 15 years from now. That moves electronics manufacturing from simply building to a specification toward manufacturing for lifetime performance.

There's always been this belief that our electronics are generally fragile. The effective life of a cellphone is about four years, for example. Do we expect much more out of our vehicles?

You raise a good point. Even today's qualification methods and standards usually point to an automobile's service life of approximately 8,000 hours, as you know. But now we're seeing that electronics requirements call for operation or monitoring over periods exceeding 120,000 hours. This will require a different thought process. Basically, the vehicle's electronics are always on, even when you're not using it. The battery management system, for example, monitors the batteries' state of health and other information.

There's no rest for the electronics.

Yes, exactly. I like that. All this means is we need to take a different approach to how we view electronics and applications. This always-on type of environment creates combinations we haven't seen before: high voltage, temperature, humidity, contamination, vibration, and the long-term electrical bias effect. The industry will be forced to evolve in how it qualifies and tests products.

Earlier, you called this a paradigm shift. Can you explain what you meant?

Automotive has always really lagged other industries in adopting new components and electronics technologies. We were basic; we relied on tried-and-true solutions. You mentioned that cellphones have a different lifetime expectancy than automobiles, but some of the components available to the automotive industry are the very same components that might be used in a cellphone, say, for a network access device. Now, the challenge is how to make some of these components that were originally developed for the consumer marketplace reliable in an electric vehicle, where conditions can be much more severe, and lifetime and safety expectations

are very different.

My call to action for the industry is that we need to stop treating reliability as something we verify at the end of product development. It has to begin with the materials and the design, continue through the PCB fabrication and assembly, qualification, and manufacturing process control, and then continue into the field. That's the approach I'm trying to emphasize, and achieving that requires participation across the supply chain, from material and component suppliers to PCB fabricators, EMS companies, Tier-1 suppliers, and vehicle manufacturers.

We also need qualification methods and standards that better reflect how EV electronics are actually used, including the combined effects I mentioned previously—high voltage, temperature, humidity, and vibration—and the long-term electrical bias conditions. Perhaps most importantly, we need to close the feedback loop, which is possible now.

Field data, failure analysis, and fleet monitoring, along with predictive diagnostics, should feed back into materials, designs, manufacturing processes, qualification methods, and standards. Reliability should be a continuous engineering process rather than a pass-fail event. We have this capability now to retrieve information from the field, and we can use that to improve reliability as we go along.

What needs to be understood throughout the entire supply chain is how it affects each member and how they contribute to the reliability shift we're looking to achieve.

Stan, you've gained a new following through this series. How can people follow up with you? What conferences or shows will you be at?

The Advanced Electronics Packaging Conference will be part of APEX EXPO, April 3–8, 2027, in Anaheim. For papers, the call for participation is already out, and we're accepting contributions through Sept. 18. We've already planned sessions on power module materials and design, high-voltage assemblies and reliability, and a special EV session featuring invited speakers to help shape the roadmap for where the industry's going. So that's an excellent venue.

Other power electronics conferences I'll be attending include APEC in New Orleans in March, PCIM in Nuremberg in May, and The Battery Show series in the U.S., Europe, and Asia.

Thanks so much for taking the time to have this conversation. I'm sure your "Road to Reliability" series will have a lasting impact on our readers.

I appreciate this, Nolan. **SMT007**

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The Clean Truth About No-Clean Flux



Editor's note: This is a new column by Dr. Adam Klett, doctor of science at KYZEN. It will appear regularly in SMT007 Magazine.

BY DR. ADAM KLETT, KYZEN

One of the most misunderstood terms in electronics manufacturing is “no-clean flux.” It sounds simple enough: Use the flux, complete the soldering process, and, best of all, you don’t have to clean. Unfortunately, that interpretation has led to decades of confusion and, in some cases, preventable reliability problems.

The clean truth is that no-clean does not mean “do not clean.” It means something much more specific.

Understanding what the term actually means, where it came from, and when cleaning remains the right choice is essential for making informed manufacturing decisions.

The Origin of No-Clean

To understand no-clean flux, it helps to look at the history of electronics assembly.

Until the early 1990s, electronics manufacturers



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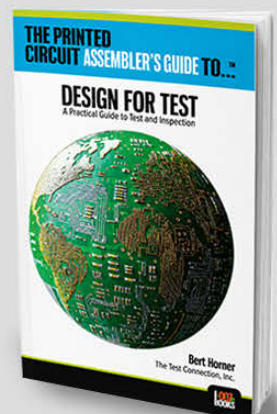
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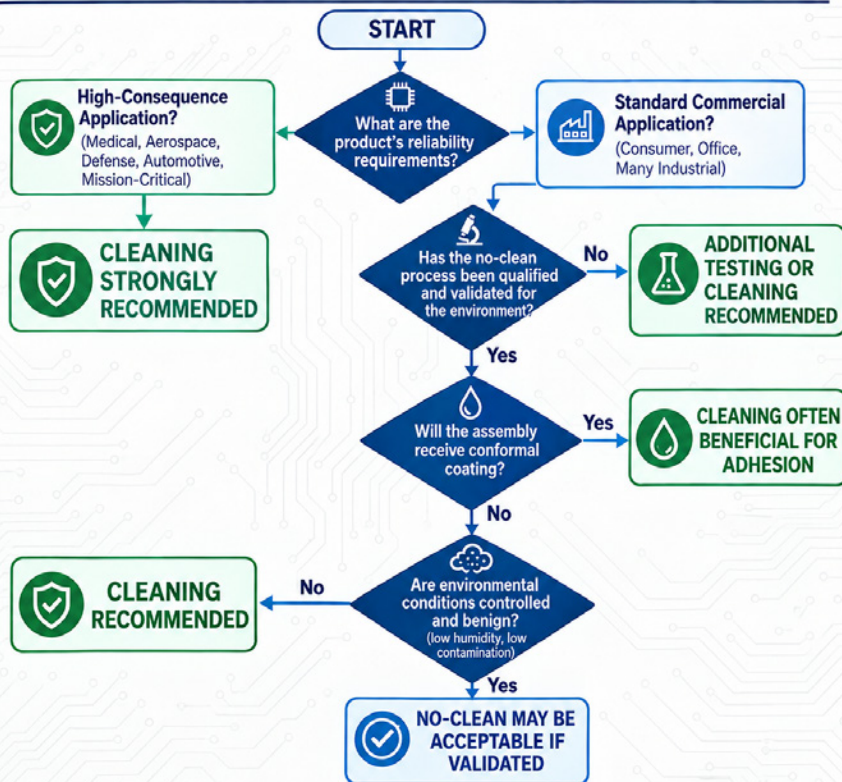
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NO-CLEAN FLUX

A Decision Guide for Cleaning, Not Just a Classification



routinely cleaned assemblies after soldering. Traditional rosin and water-soluble fluxes left residues that were often conductive, corrosive, or otherwise undesirable. Cleaning was simply part of the process.

Then came a significant industry shift. Environmental regulations began restricting widely-used solvent-based cleaning chemistries, prompting manufacturers to seek alternatives, including ways to eliminate cleaning altogether. Flux suppliers responded by developing formulations that used lower-activity activators and left smaller quantities of residue after reflow.

The key objective was not to create a flux that could never be cleaned, but to create a flux whose residues were sufficiently benign so that cleaning would not be required under appropriate conditions. It's a critical distinction.

The term "no-clean" was never intended to mean "cleaning is unnecessary in all cases." It simply

meant that, under the conditions for which the flux was designed, the residue could often remain on the assembly without compromising reliability.

Somewhere along the way, however, many people began equating "no-clean" with "don't clean." Those two concepts are not the same.

What No-Clean Actually Means

Modern no-clean fluxes are carefully engineered systems. During soldering, activators remove oxides and promote proper wetting. After reflow, much of the chemistry is consumed, volatilized, or encapsulated within nonconductive resin systems.

The resulting residue is intended to exhibit great SIR, low electrochemical activity,

and long-term performance in the intended environment. In other words, the residue is designed to be compatible with remaining on the assembly.

Notice what that definition does not say. It does not say that the residue disappears, that it is chemically inert, or that it is suitable for every product or environment.

Even residues that pass standard qualification testing can still interact with humidity, process variation, component geometry, and environmental contaminants. The fact that a residue is classified as "no-clean" does not exempt it from engineering evaluation.

When No-Clean Works Well

There are many situations where a no-clean process is entirely appropriate.

Commercial products operating in controlled indoor environments often perform extremely well with qualified no-clean residues left in place. Consumer electronics, office equipment, and many

industrial products have successfully used no-clean processes for decades.

No-clean can provide several advantages, including lower manufacturing cost, reduced process complexity, and lower resource consumption (e.g., water and electricity). If the assembly design, flux chemistry, and operating environment are compatible, a properly controlled no-clean process can deliver excellent reliability.

The important phrase here is properly controlled.

Qualification data, SIR testing, and process validation still matter. Assemblies should not be considered reliable simply because the flux label says “no-clean.” Industry guidance now emphasizes that no-clean residues must be validated for their intended environment rather than assumed to be acceptable by default.

When Cleaning Still Makes Sense

There are also many situations where cleaning remains the better engineering choice, even when no-clean materials are used.

One obvious example is high reliability electronics. Medical devices, aerospace systems, defense products, automotive electronics, and mission-critical controls often operate in environments where failure carries significant consequences. In these applications, engineers frequently choose to remove residues to reduce uncertainty and maximize reliability margins.

During manufacture, residues may become trapped beneath components or concentrate in areas where environmental exposure is difficult to predict. Research has shown that flux residues can absorb moisture and contribute to leakage currents, reduced insulation resistance, electrochemical migration, and corrosion-related failures under humid conditions.

Another common reason for cleaning is the application of conformal coatings, where cleaning may improve both coating adhesion and long-term reliability.

Reliability: The Real Decision Driver

Perhaps the most important lesson is never to ask, “Is this a no-clean flux?” Instead, ask, “What level of cleanliness does this product need to achieve its reliability requirements?” Those are fundamentally

different questions.

A no-clean residue may be entirely acceptable for a consumer electronic device stored indoors for five years. The same residue may be unacceptable for an autonomous vehicle controller, a satellite communication system, or an implantable medical device.

Reliability depends on the interaction between an ensemble of parameters, including but not limited to, the chemistry of the materials involved, design choices, environmental exposure, and electrical loading. No single flux designation can account for all these variables.

The industry has accumulated ample evidence that residues can contribute to electrochemical migration, dendritic growth, corrosion, leakage currents, and reduced surface insulation resistance when sufficient moisture and electrical bias are present. At the same time, countless successful products demonstrate that qualified no-clean processes can provide years of reliable service when used appropriately.

Both statements are true.

The Clean Truth

The biggest myth surrounding no-clean flux is that the name itself answers the cleaning question. It does not. “No-clean” is a material or process classification, not a reliability strategy.

The term originated because certain residues could remain on assemblies without requiring mandatory post-solder cleaning under appropriate conditions. It was never intended to mean that cleaning is unnecessary, undesirable, or irrelevant. Every assembly still requires an engineering decision based on risk, environment, design complexity, and reliability expectations.

The clean truth is that no-clean means cleaning is optional only when the evidence says it is. When reliability demands it, no-clean can quickly become must-clean. **SMT007**



Dr. Adam Klett is director of science at KYZEN.

Building Consistent Reflow Results Across Automotive Manufacturing Sites

As automotive electronics production shifts among global locations, replicating a successful assembly process isn't as simple as moving the equipment or copying a recipe. Miles Moreau of KIC talks with Nolan Johnson about the challenges of maintaining consistent reflow performance across different lines and facilities. They explore what manufacturers can learn from better process data, where optimization can make a difference, and why experienced engineers still play a critical role in getting the process right.

Nolan Johnson: Miles, from your perspective, how does a manufacturer maintain product consistency and reliability across facilities when automotive electronics assembly is expanded or relocated?

Miles Moreau: Realigning the supply chain adds process demands because you're now trying to move a line to a factory with different equipment. It was running fine in Europe or Asia, and now it has to run the same way in Mexico or North America. Setting the line up identically probably won't be enough. Are they meeting the same process demands now that they've moved the equipment, or are they combining different equipment? These supply chain maneuvers add another layer of process complexity.

When a process is duplicated at another facility, what does it take to achieve comparable performance and consistent results?

You start with the process itself. One way to see the transfer challenge is through higher-power automotive assemblies, where voiding can be a key issue. These products must manage significant heat, and voids can reduce the effective heat-transfer area and increase thermal resistance.

Our customers are trying to reduce the occurrence of voids, and the reflow profile is one of several factors they can work with. Vacuum reflow ovens can reduce voiding, while adjustments to ramp rate, soak, and time above liquidus may also help, depending on the solder paste, component, and assembly. The objective is a more robust and repeatable process.

When you get into the process audit, you ask





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yourself, “Is this process in control?” Optimization helped center the process where it needs to be, and now you’re talking about moving product manufacturing. It was running on a line with oven manufacturer A, and now they’re standing up a line in the U.S., where they’re not using oven A. The U.S. oven might have two fewer zones or some other difference. So, how do we get up to the same level of process control as at the original facility? That’s where our “Heat to Data” concept takes hold.

Automotive is a demanding market segment; you have to optimize around a lot of parameters to reduce defects, and that’s challenging. So, if we can use that profile data to optimize the setup and then use the production data to ensure they maintain the desired parameters, you can do the matching. You may have different settings and different ways the machine is run, but your end result is comparable.

Research shows that stencil thickness has the most influence on reducing voids, but reflow was number two. Your solutions have a significant influence on how voids are managed and mitigated. What are you finding as you work with customers? How high is their awareness that the oven profile has so much influence?

I think it’s pretty good. From a solder paste standpoint, if something is wrong, someone may immediately say, “It’s the paste.” But the oven and profile also have to be understood. After optimizing the reflow profile, a paste that appeared to be struggling may perform well.

One solution to voids is vacuum reflow, but those machines cost more than a standard reflow oven. There’s more maintenance and understanding needed regarding a vacuum in the middle of your reflow process. It’s a successful way to reduce voids, but you can manipulate and optimize the reflow profile to further reduce them, combined with stencil design and other measures along the line. PCB design, surface condition, and pad configuration can also influence voiding and other soldering issues.

We try to inform our customers as best we can that, yes, it’s a relatively straightforward investment



Miles Moreau

to use a reflow profiling tool to optimize the recipe. That goes back to the Heat to Data idea. It’s not sufficient to say, “Here’s my high and low on my spec for the profile, the paste, and the components, and if I’m inside that range, I’m good to go, and it will pass test.” Automotive is looking for more than that.

For automotive work, being barely inside the process limits may not be enough. Manufacturers want the profile centered in the process window and the process tightly controlled, so they can provide customers with objective evidence that it is stable and repeatable. That evidence supports the monitoring, traceability, and audit expectations automotive suppliers encounter under IATF 16949, VDA 6.3 and customer-specific requirements.

Our reflow process inspection (RPI) system provides calculated thermal-profile data for each board during the production run. That gives the manufacturer board-level process traceability and objective evidence to support customer audits and traceability requirements.

Tell me more about your reflow inspection solutions. To move to the data, you need to know the results of your profile, and getting a feedback loop seems important to keep everything in process. You’d want to know if parameters are starting to drift, so you can pull them back into the solid part of your process, for example.

KIC has always focused on thermal process measurement and monitoring. It is one of our core technologies and what the company was founded on. We first developed profiling tools to establish the process correctly, then added automatic monitoring, prediction, and optimization based on extensive profiling data.

Reflow process inspection differs from other inspection steps. SPI verifies solder paste deposition, while pre- and post-reflow AOI inspect component placement and visible solder-joint conditions.

In reflow, the process adds heat rather than physical material. A board may appear acceptable at AOI, but that inspection does not reveal the thermal profile the assembly experienced.

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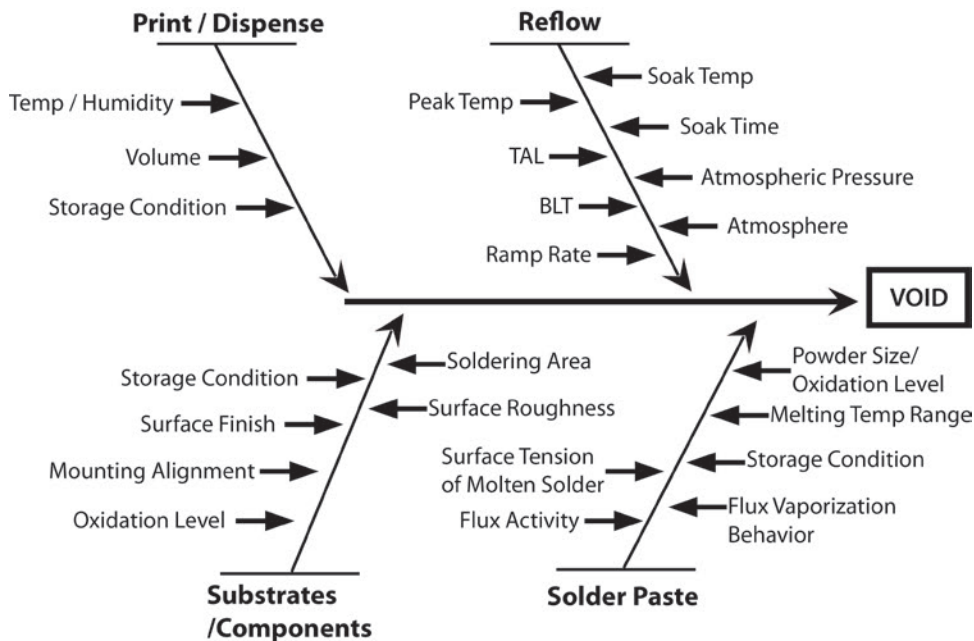
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Many factors influence reflow consistency.

We embed sensors at the appropriate positions to gather temperature data along the board path. The principle is consistent with what we now call Industry 4.0, although KIC began monitoring conveyorized thermal processes in 1977. The oven's control thermocouples confirm that its zones are controlling to their setpoints, but they do not show what is happening to the product at the conveyor level. Our patented sensor hardware and software use 30 fixed thermocouple measurement points, together with conveyor speed and product position, to calculate the thermal profile each board experienced.

The engineer or technician runs that baseline profile in programming mode. As with programming SPI, you provide baseline images, and when it's inspecting production boards, it flags deviations.

In the reflow process, the baseline is established with thermocouples attached to the board. Once that data is used to optimize the profile, it programs the inspection system. During production, the system tracks each board past the embedded sensors and calculates its profile as it exits, including ramp rates, soak times, time above liquidus, and peak temperature.

Do these thermocouples pass that information back to the oven controller so the oven can adjust in real time to keep the temperatures right?

Is KIC in the control loop, in other words? That's not a straightforward answer, because there's a lot more that influences the profile beyond what we're monitoring. We can accurately read the situation, but there are other parameters. We can identify that the profile has changed, but the data alone may not identify the cause. Is it the load? Maybe it's a panel of 8-up engine controllers on one panel, where it's a bigger board, and they're running a board every eight inches. When the oven is fully loaded,

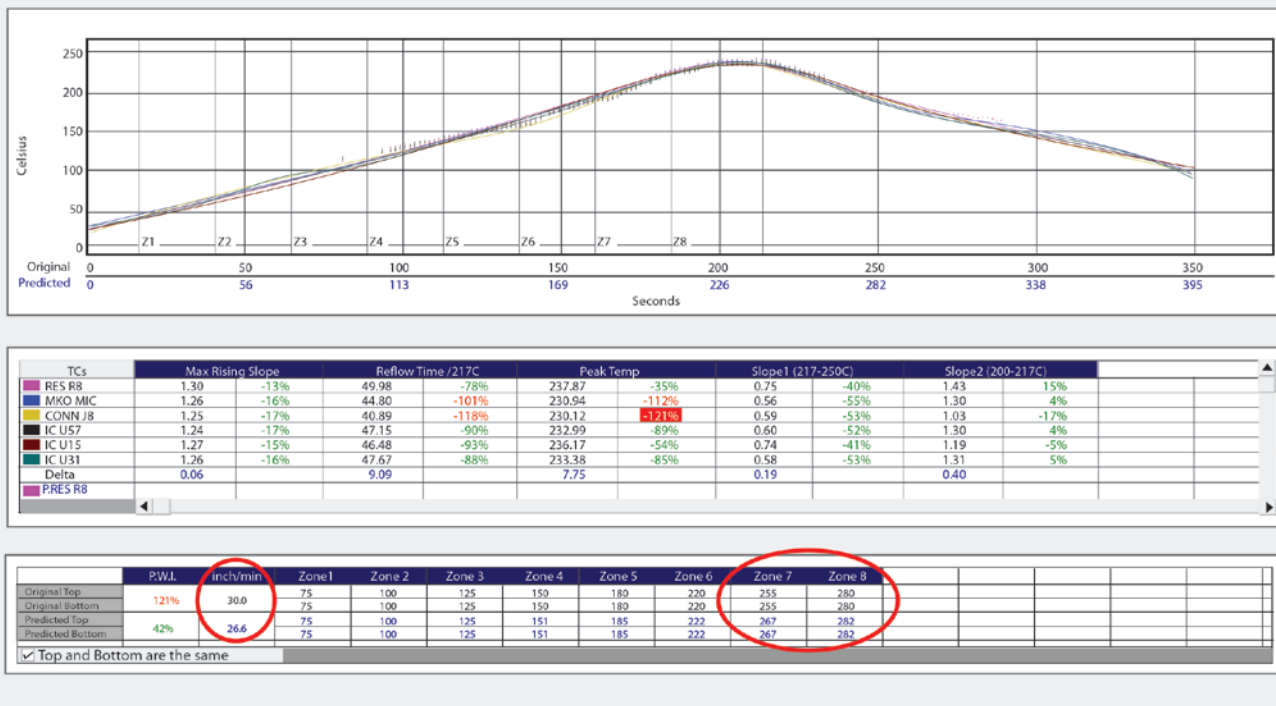
those boards are really pulling heat. We don't want to start adjusting the control loop because of these other influences. Instead, we use a human-in-the-loop approach.

When we see a trend moving in the wrong direction, the system alerts the user and provides as much guidance as possible. If necessary, the engineer can run an instrumented profile and re-optimize the recipe.

You're providing the data and process monitoring, but are you leaving the ultimate decision-making to the process engineers to make the appropriate adjustments?

We give direction, not just an alarm. Because factors beyond the oven's basic control loop can influence the profile, the process still needs a human in the loop. As the technology improves, more decisions may be integrated into the control loop, but today the best result is notification followed by guidance on where the issue may be.

We don't want to hide something by continuing to control the oven when it has nothing to do with adjusting the heat. For example, if reflow time were increasing and an automatic loop responded only by speeding up the conveyor, the assembly could receive insufficient thermal exposure because conveyor speed was not the root cause. There are



Adjusting parameters can be complex. In this example changing conveyor speed has a dramatic effect on temperatures at the end of the process.

too many interacting variables to make that adjustment safely without engineering judgment.

We have enough data to provide good guidance on how to address the issue, and then they can re-optimize. That human step helps make sure you don't start covering up issues.

That brings us back to the start of our conversation about automotive electronics programs and production capacity shifting or expanding across the Americas. When multiple locations are expected to build the same automotive component, how do you achieve comparable results at different facilities, potentially with different equipment?

This ties right into Heat to Data, where we've developed a metric in our software for that. Customers might have the same recipe in multiple factories, yet the profiles are different. Their first reaction is often to talk to the oven manufacturer. But what's the goal? They want the same quality result. To achieve a comparable quality result, it does not matter if the recipe is different. Oven condition, airflow, maintenance history, and production loading can all affect heat transfer, so identical settings do not guarantee identical profiles.

We created this process window index that's similar to a CPK, where you have your process window, low and high, and your data. You run your

profile with your thermocouple attached, say it's peak temperature, and your data ends up at some point in that process window.

This index helps tell our customers how this process compares to the line right next to it or the line across the world. Now, instead of saying, "I'm running this recipe versus that recipe," it's based on the quality result of the profile itself. That drives our optimization model.

We try to build that kind of engineering knowledge into the software. Customers have historical profiles already in their data set. The software can look at all their historical data and recommend a recipe. Then we can further optimize it to get them using that optimal PWI value, which is the end goal.

When customers have transparency and good visibility into the process, they can more easily demonstrate that they're in control. They also gain that last critical element: traceability. In automotive, process data often must be retained for extended periods based on customer-specific and regulatory requirements. The reflow profile can become part of that production record, providing a more complete manufacturing history.

That's super, and a great place to finish.

Excellent. I appreciate it. **SMT007**

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The 61,000-square-foot facility increases CACI's manufacturing space by more than 300% and will serve as a hub for the development, test, assembly, and delivery of advanced electronic warfare technologies that give U.S. forces a decisive advantage in contested environments.

FRACTAL Unveils Mesh-to-Gateway D2D Satellite System ►

A patented and patent-pending Mesh-to-Gateway (M2G) architecture for unlicensed Part 15 wireless networks with D2D/LEO satellites, enabling ubiquitous connectivity for sensors, machine control, fleet management, IoT, robotics, and other Part 15 devices, has been disclosed.

ITAR vs. EAR: When PCB Fabrication Can Move Outside the U.S. ►

ITAR and EAR are both export control frameworks, but they regulate different types of programs and data in different ways. Understanding that difference is critical for procurement, supplier quality, and engineering teams making supplier decisions.

Javelin JV, Tata Advanced Systems Sign India Missile Co-Production Deal ►

Tata Advanced Systems and the Javelin Joint

Venture (JJV), a partnership between Raytheon and Lockheed Martin, have entered into a memorandum of understanding (MOU) for the co-production of the Javelin All Up Round (AUR) in India. Tata Advanced Systems has been selected by JJV as the prime partner for future in-country co-production efforts.

IPC-1751 Builds Supply Chain Infrastructure for the Future ►

IPC-1751 Committee Chairs Nikki Johnson and Dr. N Nagaraj discuss IPC-1751, the newly adopted JSON-based standard that replaces the older XML format. IPC-1751 serves as a modular "envelope" that connects related standards (IPC 1752–1757, IPC-1782) for material composition, lab reports, and conflict minerals.

Lockheed Martin, Saildrone Demonstrate Launch from USV Platform ►

In coordination with the USS Theodore Roosevelt (CVN-71) Carrier Strike Group the Saildrone Surveyor demonstrated its interoperability by acting on target data for a surrogate high-speed surface craft. The demonstration went from concept to demonstration in six months in partnership with the U.S. Navy.

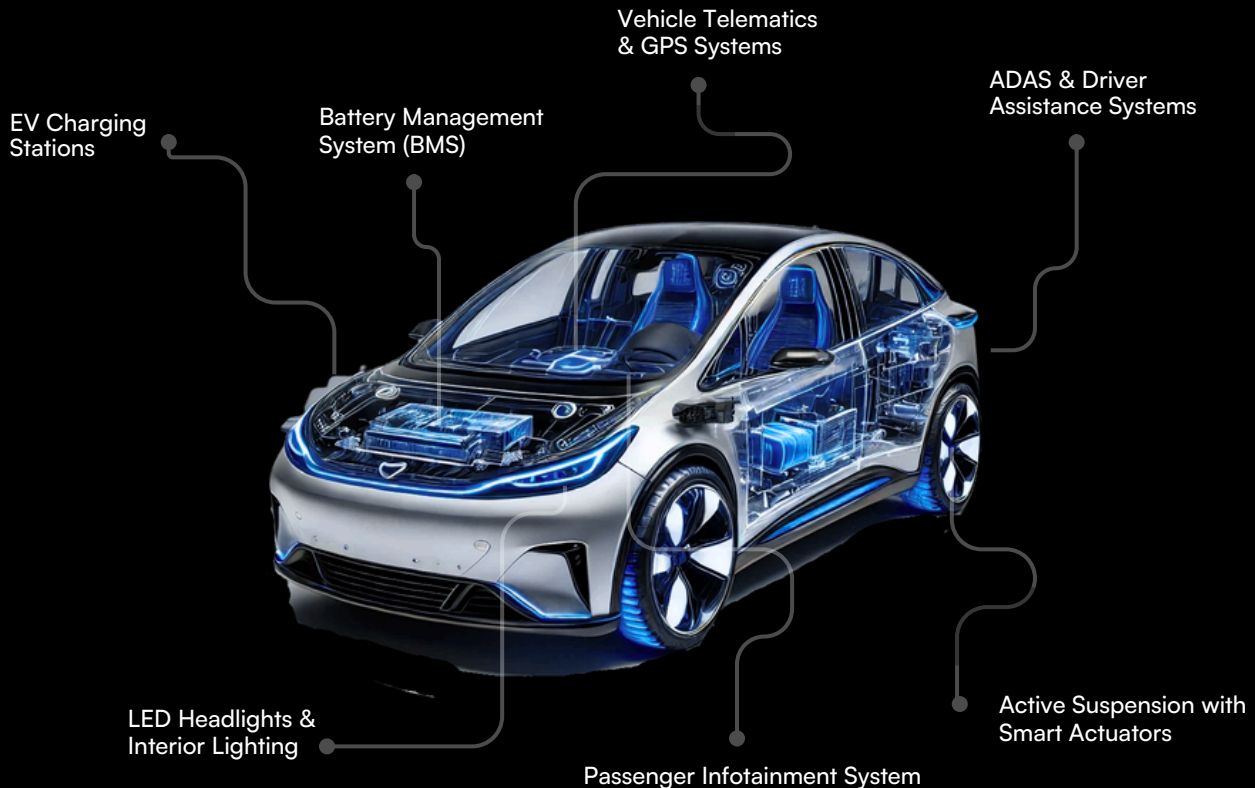
Teledyne Surpasses 1,000 Space Imaging Sensors With NASA Roman Telescope Launch ►

With the launch of Roman, there are now more than 1,000 Teledyne scientific imaging sensors in space, including those aboard the Hubble and James Webb missions. The detector technologies supplied by Teledyne support both of Roman's primary scientific instruments, enabling investigations into dark energy, exoplanets, and a broad range of astrophysical phenomena

NASA Awards Infleqion \$20M as World's First Quantum Gravity Mission Advances Toward Flight ►

NASA has awarded the company a \$20 million follow-on contract to continue development of the Quantum Gravity Gradiometer Pathfinder (QGGPf), a mission led by NASA's Jet Propulsion Laboratory (JPL) that is designed to fly the world's first space-based quantum gravity sensor.

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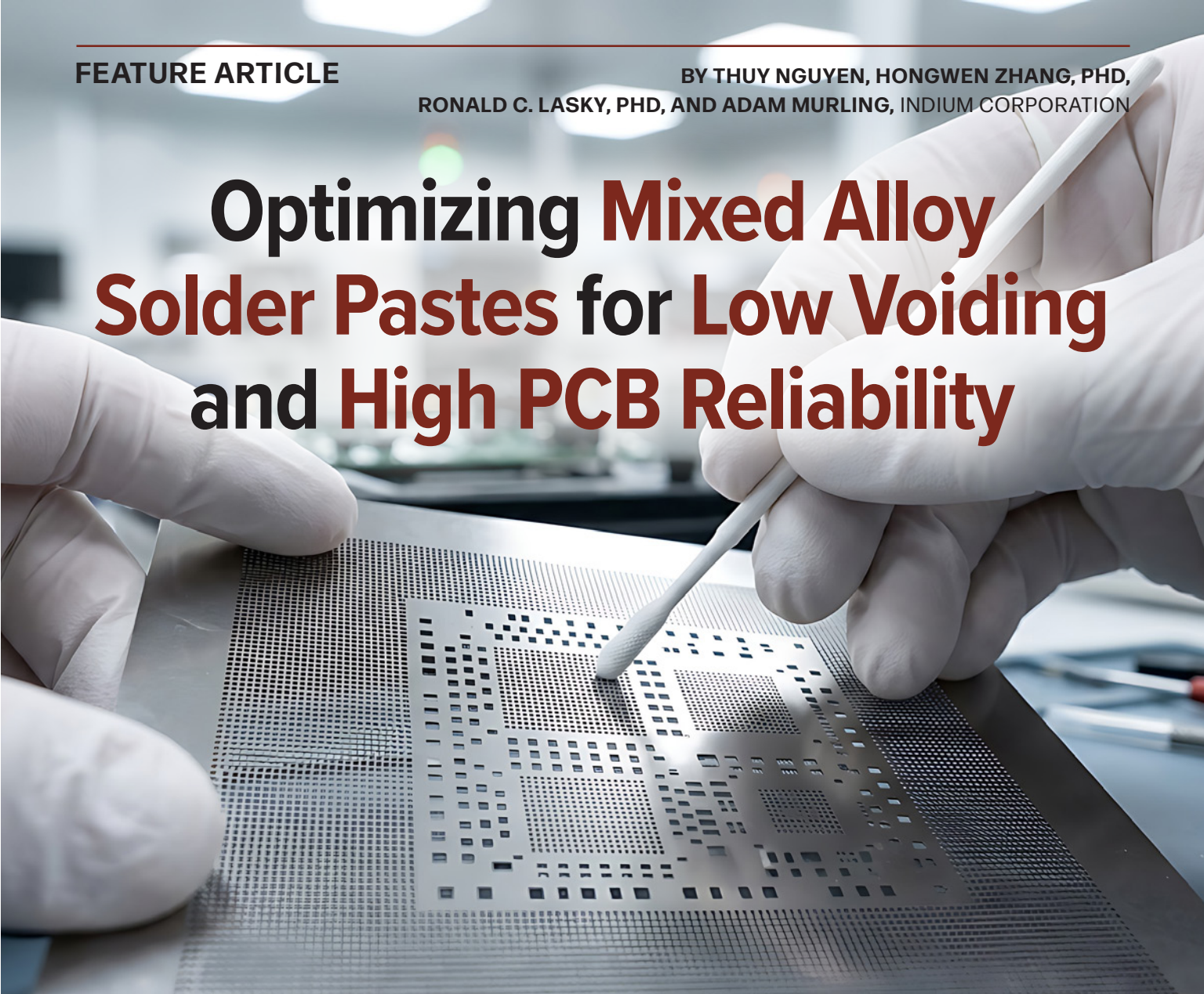


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Optimizing Mixed Alloy Solder Pastes for Low Voiding and High PCB Reliability



Editor's note: This is a condensed version of a paper originally presented at SMTA International in October 2025. Download the full paper from [I-Connect007.com](https://www.l-connect007.com).

Solder joint voiding remains a critical reliability concern in electronic packaging, particularly for high-performance and safety-critical applications such as automotive electronics. Excessive voiding can adversely affect both thermal conductivity and mechanical strength, leading to elevated junction temperatures, accelerated fatigue failure under thermal cycling, and ultimately reduce product lifetime.

To address these concerns, industry standards such as IPC-7095 provide general acceptance criteria for voiding in ball grid array (BGA) packages. For bottom-terminated components (BTCs),

including quad flat-pack no-leads (QFNs), IPC-A-610, and J-STD-001 are typically applied. The DKE automotive addendum from the IPC-A-610H and J-STD-001H further harmonizes evaluation methods by establishing consistent definitions and standardized procedures for void area measurement, enabling comparability of results across laboratories and studies.

Multiple factors contribute to void formation during the surface mount assembly process, including stencil thickness, reflow profile, and solder paste formulation. In this study, solder joint voiding was evaluated in accordance with the DKE automotive

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addendum to ensure standardized measurement practices. The key factors investigated included surface finish (OSP vs. ImSn), nano-coated stencil thickness (4 mil vs. 5 mil), reflow profile (Profile A vs. Profile B), and solder paste. Both overall void percentage and maximum individual void size were used as response variables.

The objective of this work is to provide a clear, data-driven ranking of factor importance for voiding control in QFN assemblies. The goal is to reduce voiding, improve assembly reliability, and support robust electronics production for demanding automotive environments. In light of voiding concerns, attempts have been implemented to determine if the newly developed mixed alloy solder paste (DFHR: SnAgCuBiSbInNi) could deliver voiding performance comparable to, or even lower than, SAC305, the most commonly used lead-free solder.¹⁷

Solder Pastes

The solder pastes selected in the current experiment are shown in Table 1. SAC305, Flux A, type 4, 88.5 wt.% solder paste (Paste 1) was used as a control to compare to the selected high-reliability (hi-rel) paste, and DFHR + Flux B, Type 4, 89.0 wt.% solder paste (Paste 2).

Two halogen-free flux formulations were evaluated in this study. Flux A is a robust formulation designed to enhance stencil transfer efficiency, minimize voiding, and extend stencil life. Flux B is optimized for reduced voiding while maintaining excellent printability and formulation stability. Halogen-free fluxes are the industry’s preferred path forward for meeting modern environmental, safety, and reliability requirements, especially in high-reliability or no-clean applications. Halogen-containing fluxes are still used in legacy or specialty cases but carry trade-offs in regulatory exposure.

Table 1

Paste 1	SAC305, Flux A, Type 4, 88.5 wt. %
Paste 2	DFHR, Flux B, Type 4, 89.0 wt. %

Stencil Design

The two test vehicles used stencils with different thicknesses. Even small changes in stencil thickness can significantly affect solder volume, despite

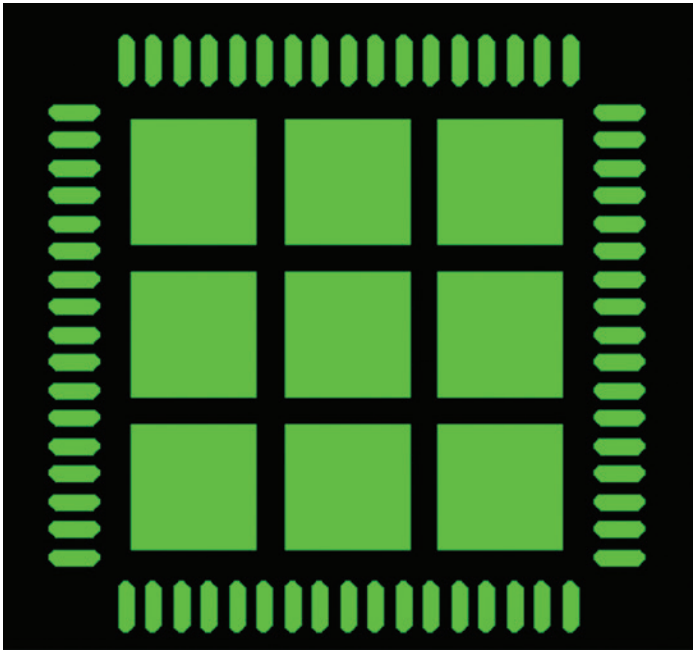


Figure 1: QFN68 thermal pad stencil design with standard cross-hatch.

an identical nine-pane window design. This is because stencil thickness directly influences paste transfer efficiency and the effective aperture area ratio, which, in turn, alters the deposited solder volume and coverage.

Both stainless steel stencils had a laser-cut, nano-coated surface and featured the same nine-pane window design, as shown in Figure 1. Each pane consisted of a 2.24 mm (88 mil) square aperture spaced 0.50 mm (20 mil) apart, resulting in a center-to-center pitch of 2.74 mm (108 mil). The full window array measured 7.72 mm (304 mil) across. In both cases, the total stencil aperture-to-pad area ratio was 75%.

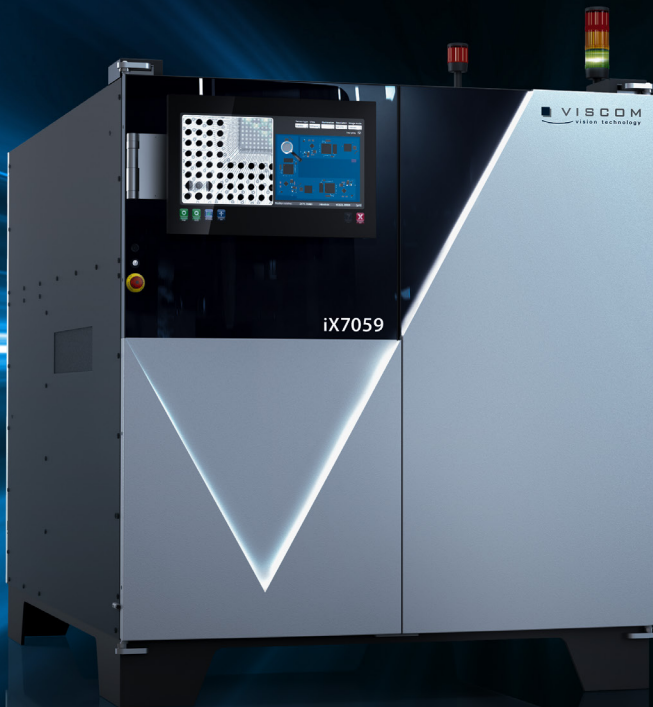
The first stencil was 4 mils (0.102 mm) thick and had an area ratio of 5.5 per aperture. The paste volume was 0.51 mm³ per pane, for a total of 4.59 mm³ across the array. The second stencil was 5 mils (0.127 mm) thick. This reduced the area ratio to 4.4 but increased the paste volume to 0.64 mm³ per pane, totaling 5.76 mm³ for the array.

Experimental Procedure

Both solder pastes were printed on the PCBs at a speed of 50 mm/s using a print pressure of 5 kg. The stencil separation distance was 2 mm at a speed of 5 mm/s. Print pressure was optimized by printing four setup boards. Any printing defects were observed



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and documented. The stencil was cleaned with a wet/dry/vacuum cleaning profile after each board was printed. The PCBs were processed through pick-and-place and then reflowed. Each board was inspected for voids using DAGE Quadra 7 X-ray inspection. The voiding data was then analyzed with JMP® statistical software.

Reflow and Inspection Methods

An eight-zone convection oven was used for the reflow process. In this investigation, two additional profiles were introduced to optimize key reflow parameters, including soaking time, peak temperature, time above liquidus, and heating ramp rate. The primary difference between the two new profiles was the ramp rate from 180°C to 220°C, set to 1.0°C/s and 1.5°C/s, respectively.

For temperature measurement, one thermocouple was placed under each QFN location (QFN 1, QFN 5, QFN 8, and QFN 12) to ensure accurate readings of the test vehicle PCB. An additional thermocouple was used to monitor air temperature, resulting in a total of five thermocouples.

Voiding Inspection

After reflow, the PCBs were inspected for voids with the DAGE Quadra 7. The voiding data captured was then analyzed with JMP®. The goal was to find the best combination of solder paste, reflow profile, and stencil thickness to achieve an overall average voiding amount below 15%.

Analysis

Across the three trials, a clear progression in voiding performance was observed, shaped by the combined effects of surface finish, stencil thickness, alloy, and profile,

as shown in the one-way ANOVA overall voiding and largest void area analyses in Figure 2. Trial 1 (OSP, 4 mil) showed only a modest impact from reflow profile modification, with overall voiding for Paste 2 reduced to 11% and 9.0%. Trial 2 (ImSn, 4 mil) followed a similar profile-driven trend but with consistently higher voiding performance, with Paste 2 reduced to 14.3% and 13.1%. The higher voiding observed with ImSn underscores the importance of surface finish, particularly in combination with SAC305, which exhibited the worst performance in this study.

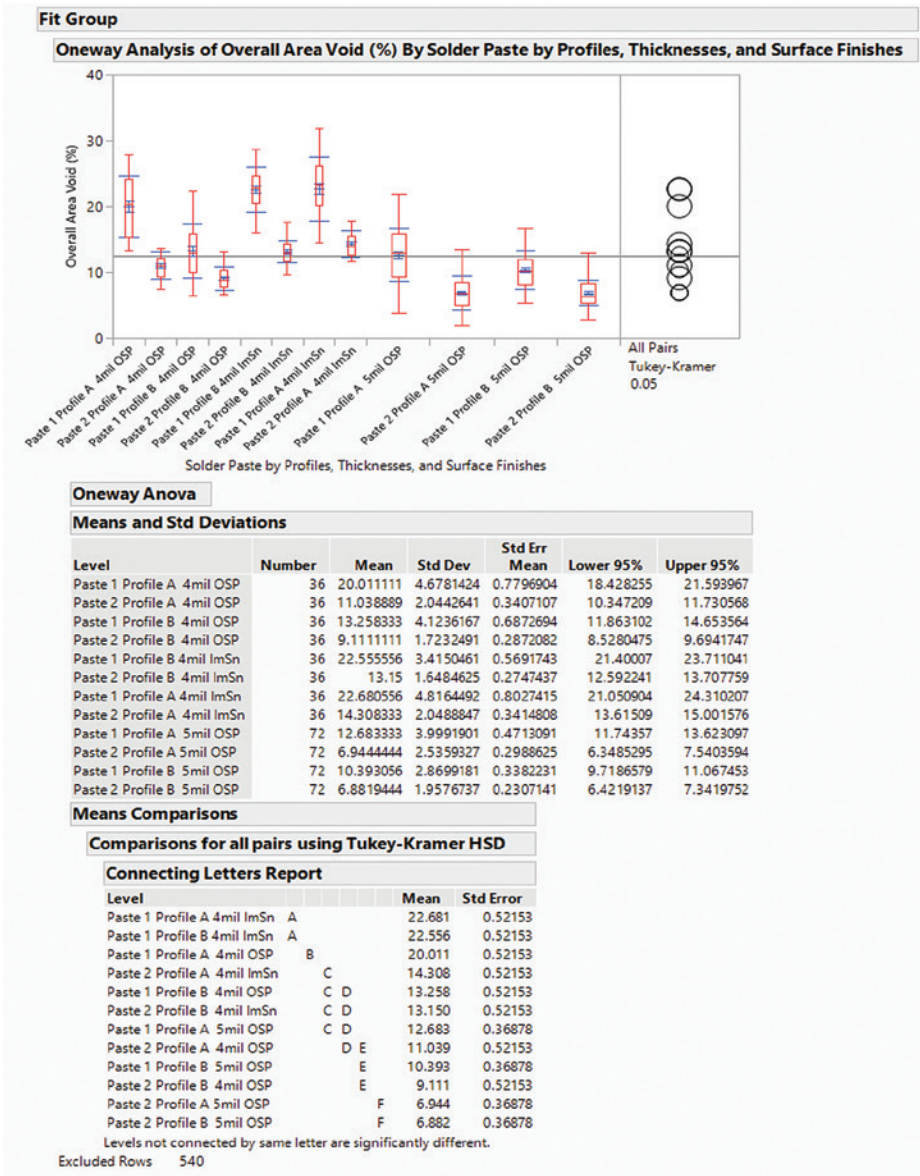


Figure 2: One-way ANOVA overall void data analysis and Tukey-Kramer comparison for Jabil boards with QFN components for all trials.

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In contrast, the mixed-alloy system (Paste 2) consistently achieved lower voiding across both OSP and ImSn conditions, reinforcing alloy selection as a secondary but important lever. Trial 3 (OSP, 5 mil) demonstrated the lowest voiding overall, with Paste 2 achieving values of 6.94% and 6.88%, well below the IPC-A-610 Class 3 threshold. This confirms the strong influence of stencil thickness in reducing voiding, while also highlighting that alloy performance interacts with surface finish. The mixed-alloy solder paste paired with OSP and a 5-mil stencil delivered the most robust voiding IPC compliance and lowest overall risk.

Discussion

The statistical analysis presented in Figure 3 confirms that stencil thickness is the most influential factor affecting solder joint voiding in QFN assemblies. Assemblies printed with the 5-mil stencil

consistently exhibited lower voiding compared to those printed with the 4-mil stencil. This trend held across all solder pastes and reflow profiles. The effect is attributed to increased solder volume, which creates a deeper molten pool during reflow. This facilitates more effective outgassing of volatiles, resulting in reduced void formation.

Solder paste composition was the next most significant contributor. Paste 2, a mixed-alloy DFHR material, outperformed the SAC305 control (Paste 1) across all test conditions. Its enhanced wetting behavior and early coalescence likely allow for more efficient volatile release, leading to fewer and smaller voids.

Reflow profile was the third key factor. Profile B, characterized by a slightly faster ramp rate between 180°C and 220°C, consistently reduced voiding relative to Profile A. This profile likely promotes earlier flux activation and more efficient outgassing during

the critical reflow phase. However, the impact of reflow profile, while measurable, was secondary to stencil thickness and solder paste selection. The highest single-void sizes occurred with the 4-mil stencil and Paste 1 under Profile A, while the smallest voids were observed using the 5-mil stencil, Paste 2, and Profile B.

Interaction effects were also statistically significant, particularly between Paste × Profile and Paste × Stencil Thickness. These interactions demonstrate that the benefits of Profile B and thicker stencils are not uniform across all materials. For example, the advantages of

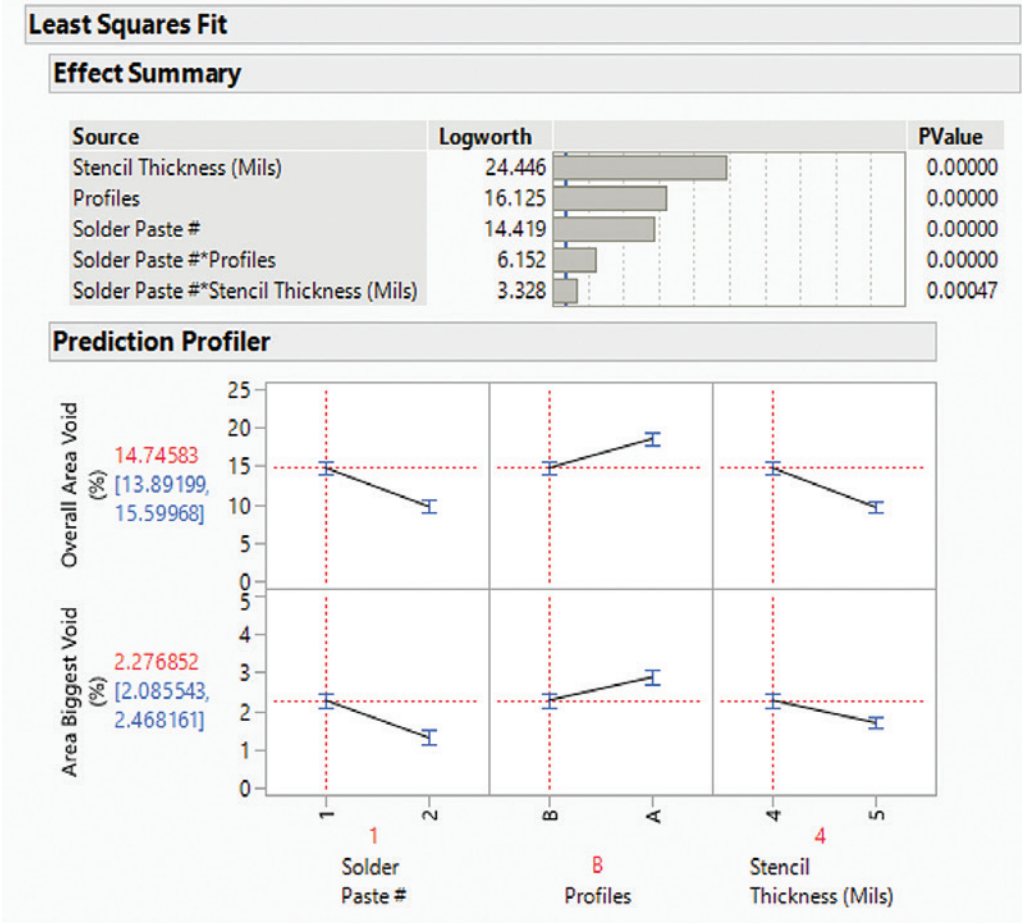


Figure 3: Effect summary and prediction profiler of multiple factors.

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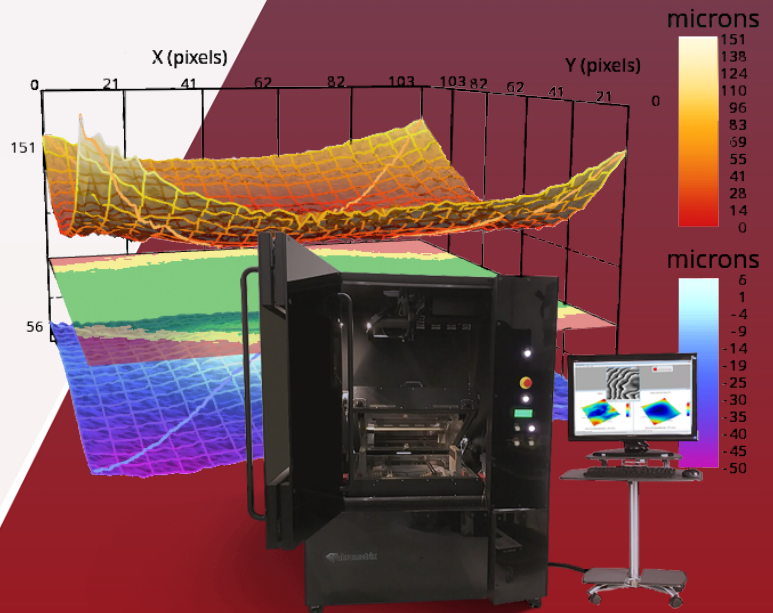
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Profile B were most pronounced when paired with Paste 2. Additionally, the performance gap between pastes widened under the 4-mil stencil condition, suggesting that material-process compatibility is critical when solder volume is limited.

Taken together, these results establish a clear hierarchy of influence:

Stencil Thickness » Reflow Profile > Solder Paste > Paste × Profile > Paste × Stencil Thickness

Interactions between solder paste and stencil thickness, while statistically significant, were the smallest in magnitude.

This analysis supports a key interpretation: Stencil thickness sets the baseline for void performance, while reflow profile and solder paste offer opportunities for further optimization. Importantly, reflow adjustments alone cannot overcome limitations imposed by stencil design or suboptimal material choices.

Finally, these results align with the reduced-factor design of experiment (DOE) approach used in this study. The decision to focus on OSP surface finish

helped isolate and evaluate the primary process variables without introducing confounding effects. Future work will expand this analysis to include ImSn surface finishes to confirm whether these findings generalize to other production-relevant surface metallization.

Figure 4 presents representative X-ray images of QFN components assembled using an OSP surface finish. The comparison includes two solder pastes (Paste 1 and Paste 2), two stencil thicknesses (4 mil and 5 mil), and two reflow profiles (Profile A and Profile B).

Clear differences in voiding behavior were observed. Assemblies produced with the 4-mil stencil showed a higher percentage of voiding compared to those made with the 5-mil stencil. This is likely due to thinner solder deposits restricting the release of entrapped gases during reflow.

Paste 2 generally exhibited smaller and more evenly distributed voids than SAC305, especially when used with the 5-mil stencil. These observations suggest that reflow profiles influence not only

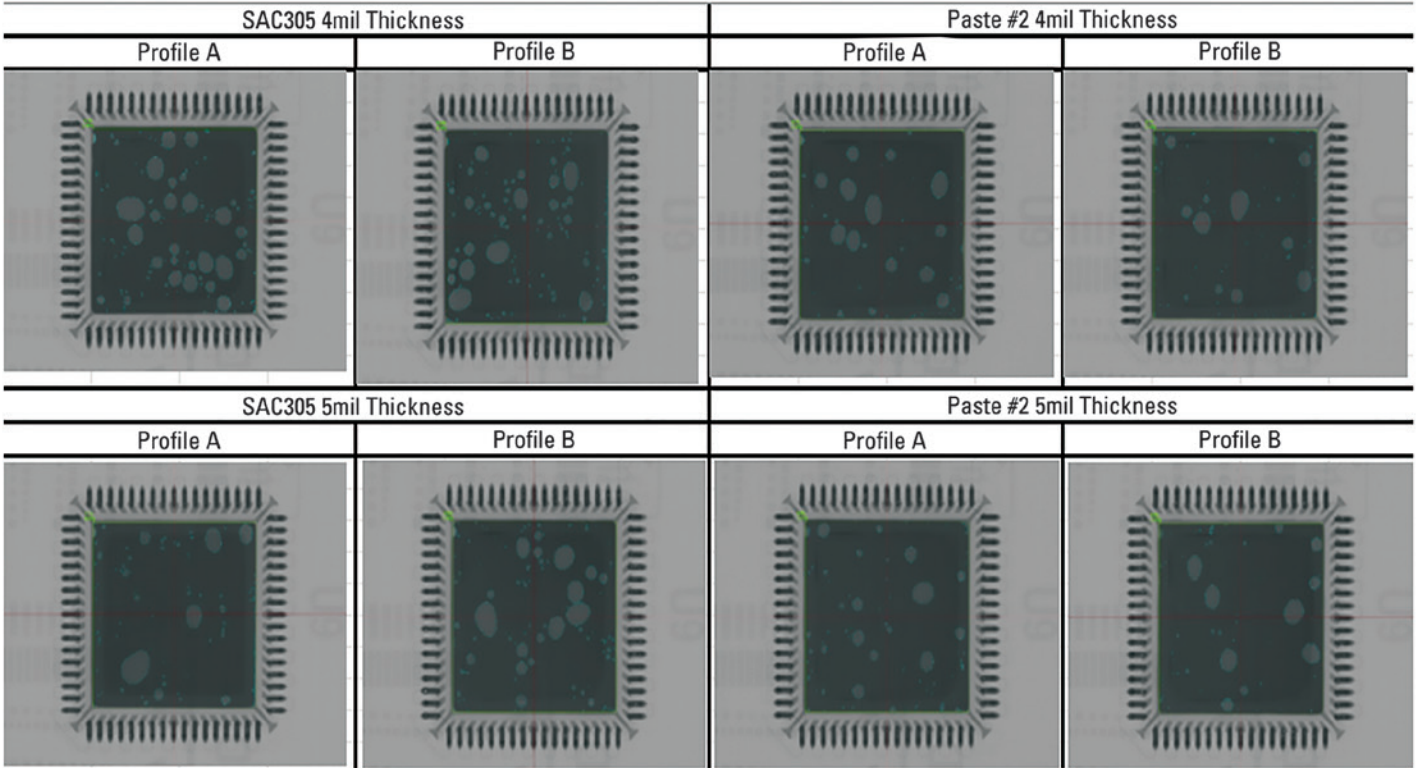


Figure 4: Representative of X-ray images of OSP 4-mil and 5-mil stencil.

the overall voiding level but also the shape and distribution of the voids.

Since void morphology can impact both thermal performance and mechanical reliability, future studies should investigate how void distribution correlates with long-term reliability. This includes further testing under thermal cycling and mechanical stress conditions.

Conclusion

This study demonstrates that solder joint voiding in QFN assemblies is primarily influenced by material-related factors. Among these, stencil thickness emerged as the dominant variable, with the 5-mil stencil consistently producing lower voiding levels compared to the 4-mil stencil. Adjustments to the reflow profile had a measurable but secondary effect on voiding, while the choice of solder paste contributed to a lesser effect.

These findings highlight that selecting favorable material combinations is critical to achieving voiding performance targets and ensuring process compliance. It should be noted that ImSn surface finish data could not be included in this analysis due to limited data availability, as Trial 3 focused primarily on OSP finishes.

These results underscore the importance of optimizing material selection early in the process development phase, as this provides a more robust foundation for subsequent fine-tuning of process parameters such as reflow profiles. For BTCs, voiding acceptance criteria beyond IPC-A-610 are often defined as “as agreed between user and supplier” (AABUS).

Overall, compliance to IPC-A-610 Class 3 requirements was reliably achieved only under favorable material combinations, most notably OSP with 5 mil stencils and the mixed-alloy solder paste. These findings highlight that stencil thickness, profile, and solder paste choice are the critical levers for voiding reduction. It is especially relevant to automotive and aerospace electronics, where voiding control is essential.

In the previous study, reflow profile modification was identified as a major factor in reducing voiding.¹ In that work, profiles were evaluated within a single and mixed alloy solder paste/stencil thick-

ness system. In the present broader DOE, profile changes continued to show a measurable effect, but the impact was secondary compared to stencil thickness. This indicates that while profile optimization can reduce voiding within a given material set, material-driven factors ultimately dominate voiding behavior across assemblies. **SMT007**

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What American and Asian PCB Companies Can Learn From Each Other



BY TIANMING LIU, FSQUALITY

I have spent much of my career working with people from different countries. Before starting our company in 2009, I lived and worked in Japan for 13 years. Since then, I have worked with customers, suppliers, engineers, and business leaders throughout Asia, North America, and Europe. Those experiences have taught me that no

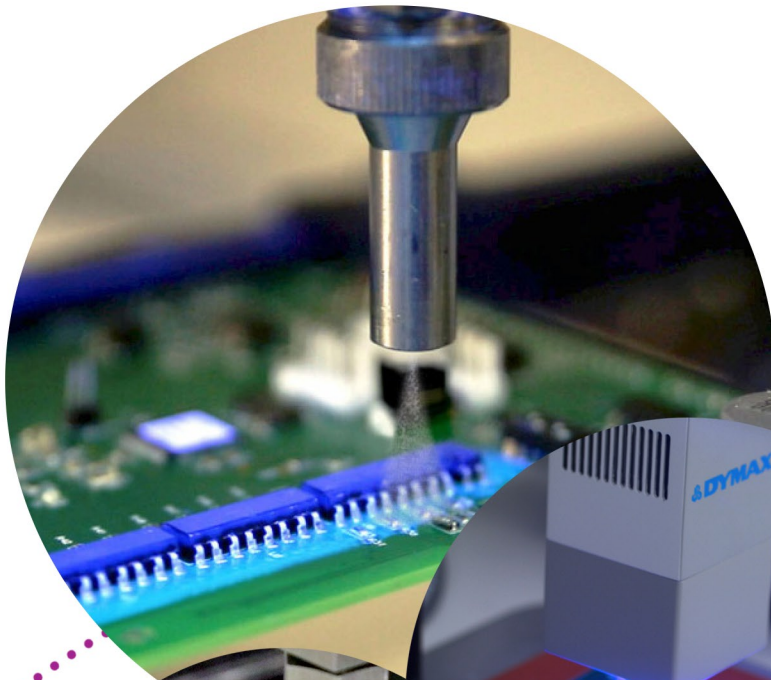
country has all the answers. Every manufacturing culture has strengths, weaknesses, and habits that can be improved.

There are many generalizations about American and Asian PCB companies. American manufacturers are often described as innovative, responsive, and expensive, while Asian manufacturers are efficient,



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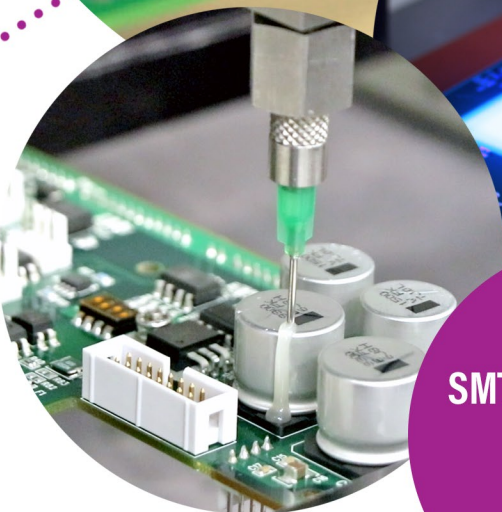


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disciplined, and focused on volume. There may be some truth behind those impressions, but they are far too simple. I have visited excellent and average factories in both regions. Geography does not guarantee quality, innovation, service, or reliability. The people running the company make that difference.

The Pros of American Companies

I admire that so many American PCB companies work with their customers throughout product development. Their engineers are often willing to get involved before the design is finished. They review stackups, materials, tolerances, impedance requirements, via structures, and potential manufacturing problems. The best American companies do not simply accept a data package and produce what is shown. They help customers improve the product before manufacturing begins.

That approach is especially valuable in the markets they serve. A design decision that appears small on a computer screen can create a serious manufacturing or reliability problem later, so when the PCB manufacturer speaks honestly and early, the customer can make a better decision before time and money are lost.

American companies are also generally comfortable with direct communication. If there is a problem, customers expect to hear about it quickly. They want access to someone who understands the technology and has the authority to act. This creates pressure, but it also builds trust. Asian manufacturers can learn from this willingness to communicate openly, especially when the news is not good. Customers can usually accept a manufacturing challenge, but they have a much harder time accepting silence or surprises.

The Pros of Asian Companies

The best Asian factories have developed strong process discipline by spending decades supporting large, demanding electronics supply chains. At higher volumes, informal methods do not work. Processes must be documented, measured, controlled, and consistently repeated across shifts, production lines, and facilities.

I have always believed that quality must be built into the process. Final inspection is necessary, but inspection cannot repair a weak manufacturing system. Materials must be controlled when they arrive. Every step of the fabrication and assembly process must all work together. When one operation is unstable, the entire product is at risk.

This is where some American companies can learn from Asian manufacturers. Flexibility and quick decision-making are valuable, but they should not depend on a single experienced person remembering how to solve every problem. Knowledge must become part of the system. A repeatable process allows a company to grow without losing the quality and responsiveness that made it successful.

Asian companies also tend to take a longer view of manufacturing investment, from new equipment and automation to employee development and factory expansion. It may take years to deliver their full return, but companies that commit to this can build capabilities that competitors find difficult to replicate. At FUJI PCB, we understand that a factory cannot wait until customers need a technology before beginning to prepare for it. By then, it is already too late.

The Practicalities of Scale and Planning

Asia has developed a broad electronics manufacturing ecosystem over many years, encompassing laminates, chemicals, components, equipment, assembly, testing, tooling, and logistics. It provides access to capacity and specialized knowledge, but scale by itself is not enough. A large factory that does not listen to its customers can still be a poor supplier.

It is an honest weakness some Asian companies must address. We can become so focused on equipment, output, yield, and efficiency that we forget how the customer experiences the relationship. Customers want dependable boards, but they also want clear explanations, useful engineering support, realistic schedules, and people who take responsibility. Manufacturing performance and customer service are inseparable.

American companies face a different challenge. Their ability to react quickly can sometimes become a substitute for planning. Solving an emergency is admirable, but preventing the emergency is better. Stronger process controls, better forecasting, deeper supplier partnerships, and long-term investment can make American manufacturers more competitive without taking away their entrepreneurial character.

Conclusion

The strongest PCB companies combine American-style engineering access, speed, creativity, and customer intimacy with Asian-style process control, scalability, continuous improvement, and long-term planning. It's possible through digital communication, shared engineering platforms, automated manufacturing data, simulation, and AI.

Technology helps, but it doesn't replace trust. AI may identify a design concern, improve scheduling, or organize manufacturing information, but

experienced people must still make responsible decisions. Customers want to know that someone understands their product, tells them the truth, and remains involved when conditions become difficult.

The Pacific Ocean is vast, but the distance between our industries is narrowing. The most valuable progress will not come from proving that one region is better, but from recognizing where each region is better and having the humility to learn from it. The companies that exchange knowledge as freely as they exchange products will build the strongest future for PCB manufacturing. **SMT007**



Tianming Liu is president of FSQuality Co. and FUJI PCB. To read past columns, [click here](#).

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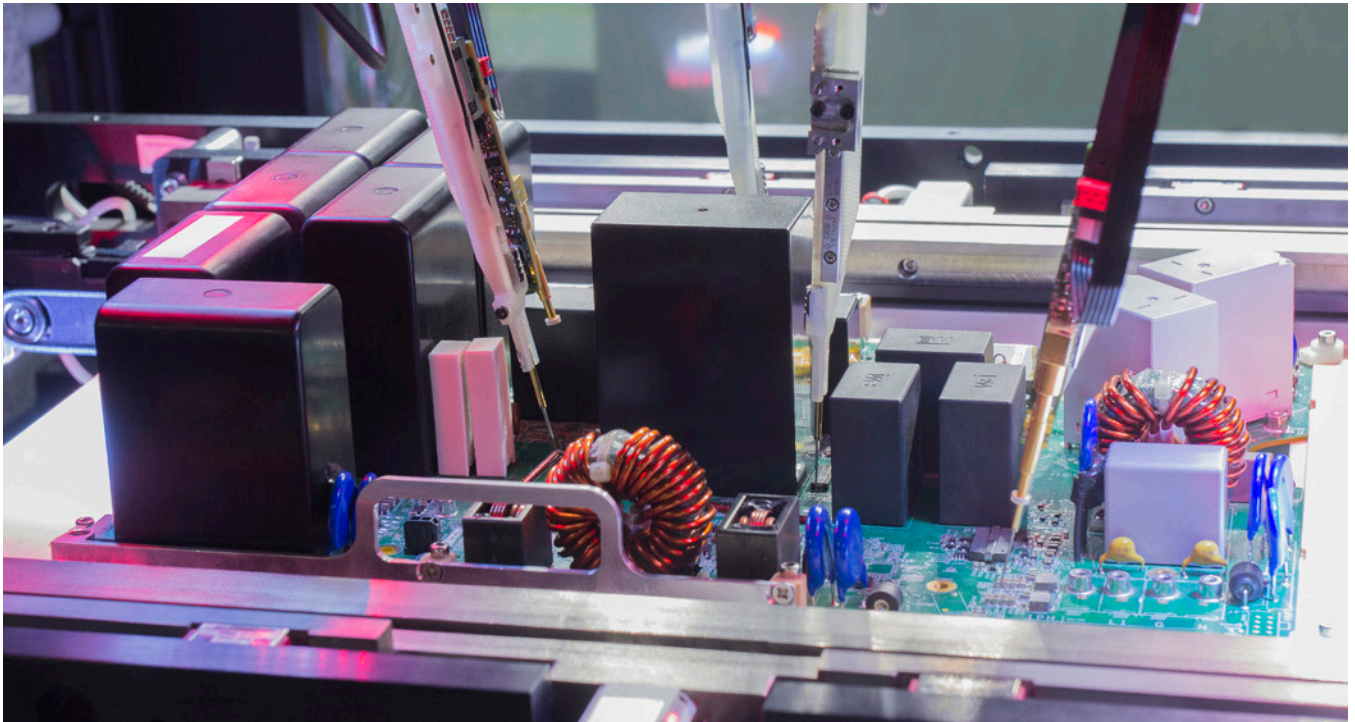
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What It Takes to Test Automotive Power Electronics Assemblies



Power electronics board assemblies are central to modern vehicle power systems. They include voltage regulators, motor drivers, inverters, DC-DC converters, and onboard chargers, which are found across the range of today's vehicles, from conventional combustion engines to hybrids and full electric vehicles.

However, modern power PCBA's do far more than just route and manage electrical energy flow through the vehicle, converting and regulating power for everything from the starter and alternator to the traction motor. Today, they also carry the diagnostics, thermal monitoring, and real-time communications that keep that power flow safe and predictable under harsh ambient conditions.

This dual role drives the integration of complex, high-power components at unprecedented production volumes. When combined with a strict zero-tolerance policy for defects and rapid cycle times, these manufacturing factors make it essential to understand exactly where test strategies fall short and what it actually takes to close those gaps.

Why Automotive Power Electronics Boards Are Hard to Test

At automotive production volumes, a zero-defect mandate means test coverage can't be optional. Even a fraction of a percent in undetected defects translates into thousands of failed units once multiplied across the line, resulting in catastrophic field failures and costly recalls.



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Power electronics board manufacturers typically detect defects using a sequential testing strategy: **In-Circuit Test (ICT)** verifies component placement, soldering integrity, and electrical continuity before the board is powered on, while Functional Test (FCT) applies input power, control signals, and varying loads to verify the board regulates power correctly and performs as intended under real operating conditions.

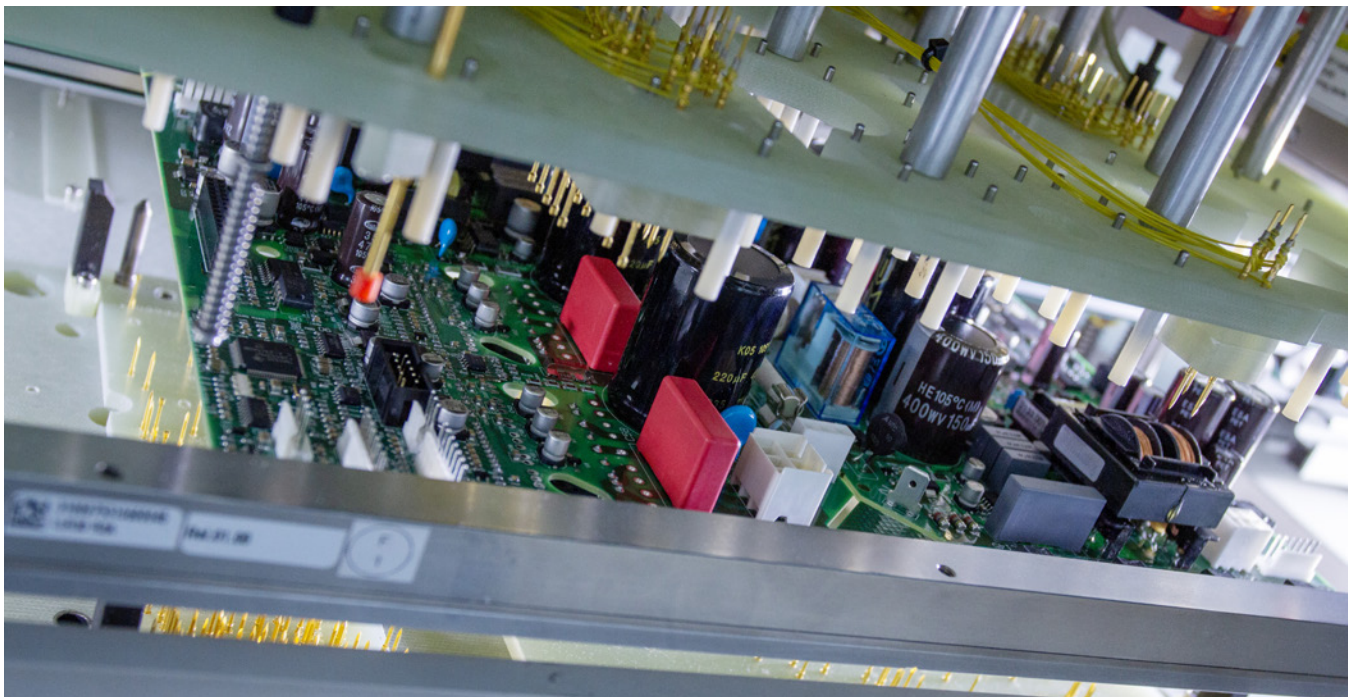
Although this sequence is well established for many production lines, not all test equipment can handle the unique barriers that next-generation power assemblies present at the speed and volumes automotive manufacturing demands. These growing technological complexities include:

1. **Bridging diverse technologies.** Today's power electronics boards host an incredible mix of components, with high-power switches and heavy magnetics alongside delicate control ICs and high-speed communication interfaces. Test equipment must be flexible enough to validate this wide array of components on a single assembly.
2. **Managing high power requirements.** Automotive power boards require testers capable of sourcing and controlling high voltages and high currents with precise synchronization and load control—instrumentation robust

enough to safely stress components at real operating levels.

3. **Mastering complex functional validation.** Once that stress is applied, comprehensive functional testing must go far beyond basic point-to-point electrical continuity to evaluating intricate control loops, measuring power conversion efficiency across operating ranges, verifying thermal management under heavy loads, and stress-testing fault protection circuits. Some functional testers aren't built to apply the dynamic loads or simulate the fault conditions required, leaving these deeper validation checks incomplete.
4. **Enforcing uncompromising safety standards.** Sourcing and measuring high voltage and current pose real hazards for both operators and test equipment. Test platforms must incorporate hardware safety features and strict automatic protocols to protect both.
5. **Navigating tall and heavy power board assemblies.** Unlike standard PCBAs, power board assemblies are dominated by tall, heavy, and bulky components that challenge handling and testing. Meeting strict automotive beat times requires testers capable of overcoming these physical weight and clearance barriers without sacrificing total test coverage.

Meeting all five challenges at once is the real test.



An electronic power board undergoes bed of nails functional test.

One Platform, Full Test Coverage for Power Electronics Boards

Overcoming these boundaries requires a radical architectural shift: Test equipment must combine highly flexible instrumentation, dynamic high-power sourcing, multi-domain test integration, and a handling framework that dynamically navigates around bulky components at maximum positioning precision and speed without collisions.

SPEA automatic testers deliver these exact capabilities, providing comprehensive test coverage at maximum line speed. SPEA bed-of-nails and [flying probe testers](#) execute the entire ICT, on-board programming, and FCT sequence, incorporating advanced capabilities specifically tuned to detect defects in power electronics board assemblies. These testers effectively resolve the core set of challenges in the following ways.

Deploying Flexible Instrumentation Architecture

SPEA ICT bed-of-nails and flying-probe testers integrate high-power resources, advanced measurement instrumentation, and flexible architectures to perform a wide range of tests. The ICT instrumentation can be configured module by module, giving it the flexibility to characterize high-power switches, magnetics, control ICs, and communication interfaces on the same board, in the same test pass, maximizing instrumentation utilization.

Simulating Real Operating Conditions

Managing high power demands requires a tester capable of simulating real-world operating conditions through load control and perfect hardware synchronization. Traditional fragmented setups cannot handle the rapid, high-energy transients needed to replicate true field environments. SPEA eliminates these limitations with a native architecture. The integrated power modules combine sources and loads to safely inject, absorb, and measure high voltage and current, stressing the board just like a real vehicle would.

Maximizing Multi-domain Test Coverage

By running ICT and FCT on a single station, these testers deliver comprehensive multi-domain coverage without the need for separate benches for every function. This unified platform drastically

enhances defect detection by enabling optical inspection, embedded software flashing, and calibration on the exact same test equipment. As a result, electronics manufacturers achieve maximum validation depth within a single footprint, eliminating the fragmented hardware, extra handling, and line bottlenecks of traditional test setups.

Containing Kilovolt Testing Hazards

SPEA testers completely isolate extreme energy. Equipped with high-power relays, high-voltage relays, and discharge resistors they safely route high-power paths during test execution. By containing these hazards within the platform itself, these testers eliminate operator risks and ensure uncompromising safety directly on the production line.

Handling Heavy Boards and Tall Components

SPEA ICT bed-of-nails and flying-probe testers feature robust conveyor systems for handling large and heavy power boards, and flying-probe testers are designed to precisely navigate the PCBA with very tall components without reducing testing speed. By combining advanced mechanical capabilities with high-speed parallel testing, these testers satisfy strict automotive beat times, preventing physically demanding power electronics boards from becoming line bottlenecks.

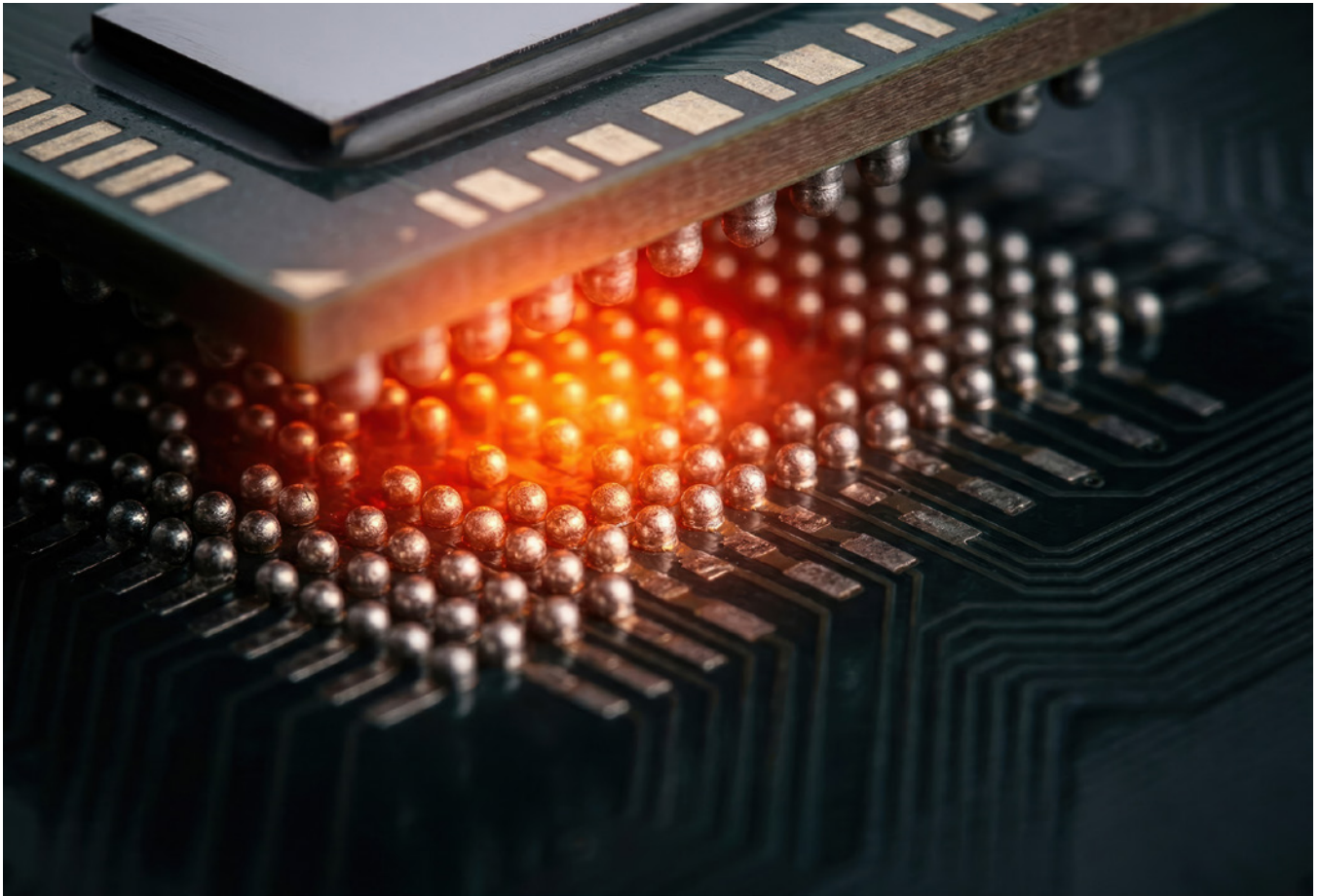
For automotive, where a zero-defect mandate is non-negotiable, this test equipment makes the difference between assuming a power electronic board is defect-free and proving its uncompromised functionality across its entire lifecycle.

By combining deep application expertise with purpose-built instrumentation, SPEA helps manufacturers achieve the quality, reliability, and cost efficiency that automotive production demands in a market where field failures carry real safety and reputational stakes, ensuring the high-power devices powering today's vehicles perform precisely as designed.



Francesca Pinto works in marketing communications for Electronic and LED lighting test products at SPEA.

Faster BGA Warpage Processing Without **Shearing or Painting**

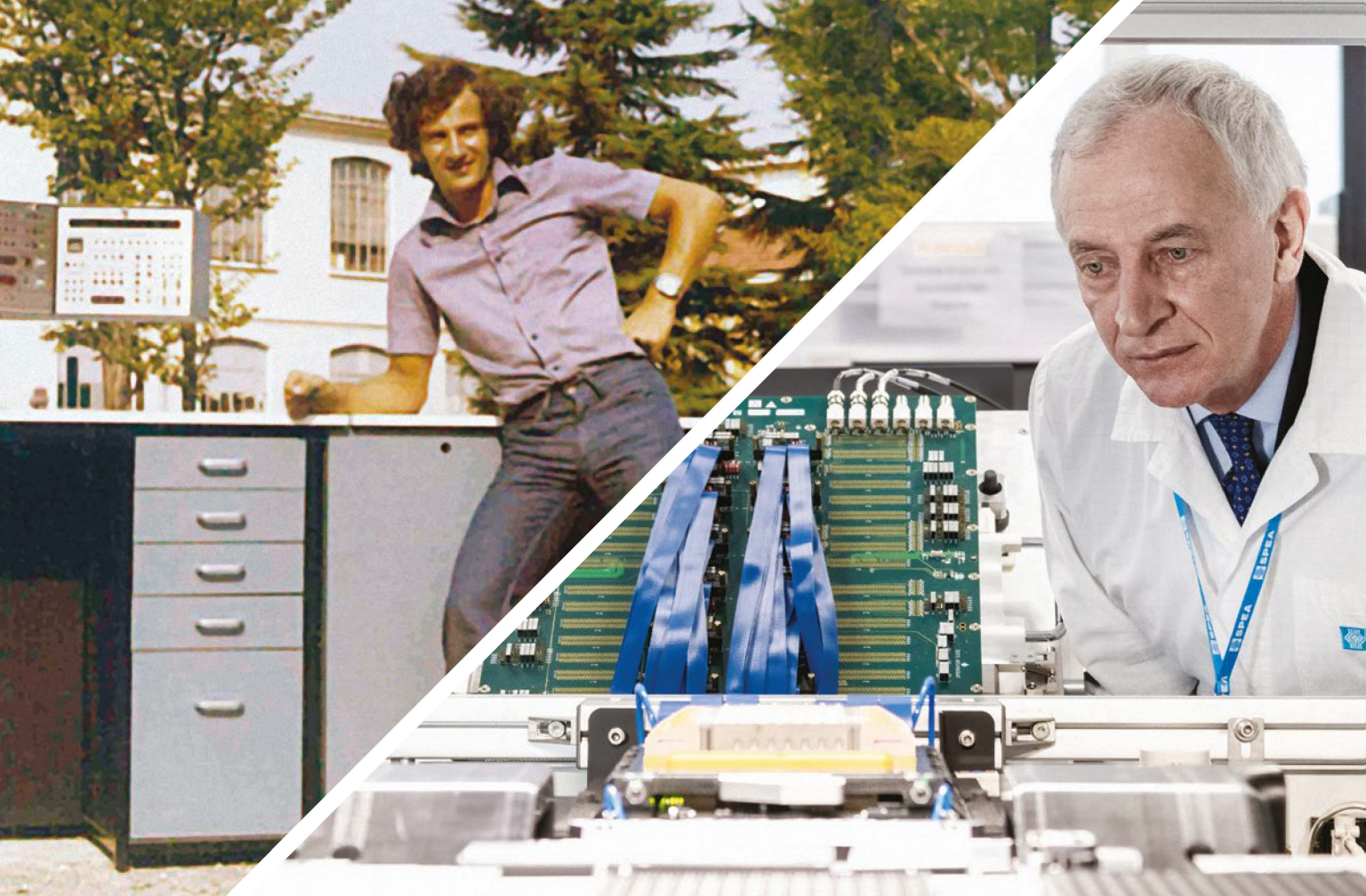


Editor's note: This article is based on a paper by the authors initially presented at APEX EXPO 2025. [Download the full paper at I-Connect007.com.](https://www.i-connect007.com)

The process of measuring BGA samples for thermal warpage is subject to industry standards from both JEDEC, in JESD22-B112C and JEITA ED7306.^{1,2} Additionally, these standards establish allowable warpage values based on ball size and ball pitch, for the JEDEC standard, pass/fail further established in JEDEC SPP-024.³ Standard practice in these standards for measuring BGA warpage is to remove the solder balls in order to measure only

the substrate surface. However, as both ball size and package thickness decrease, the practicality of removing solder balls without altering the sample shape has become increasingly challenging.

Determining warpage of BGAs can be challenging due to factors like surface preparation, size, or data processing. The solder balls can be physically sheared, which can potentially damage the substrate surface and alter the local surface topology.



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Even when the solder is completely removed, light still reflects more brightly off the copper or gold pads beneath it. Applying a coat of white paint maintains consistent surface brightness and mitigates noise due to damage caused by the shearing process. However, ball removal alters the sample composition, potentially affecting warpage and thermal mass.

Alternatively, paint can be applied to the surface while the solder balls are still intact. Post processing requires digitally selecting a region of pixels that encompasses the solder ball and scanning the entire image looking for matching areas. Processing time is dependent on the number of pixels for both the solder ball region and the full image. Searching for a 14 x 14 pixel area in a 750 x 750 image will take a greater amount of time than searching for a 14 x 14 pixel area in a 500 x 500 image. Solder balls must be removed from all acquisitions taken throughout the thermal profile. This can be accomplished either by repeating the previously described process for each individual image or by masking multiple images using the ball location from a single reference image. As samples expand, contract, or shift during the thermal profile, the masked regions may become misaligned. Careful attention is required to ensure the correct areas are masked for each temperature.

The methods presented in this article eliminate the need for solder ball shearing and painting. However, the primary advantage to these methods

is the simplified data processing and time savings associated with it.

Digital Fringe Projection

Digital fringe projection (DFP) is an optical metrology technique that measures surface contours by projecting fringes onto a sample with a digital projector and observing the resulting fringe distortion. Unlike SM, the fringes in DFP do not directly indicate height changes. Instead, the height variation is determined by comparing the distortion of measured fringes to that of a reference plane. The fringe change relative to that of the reference plane can be determined by subtracting the reference plane phase map from the sample surface phase map. DFP has minimal limitations in terms of data density, allowing smaller pixel sizes. This is advantageous to show more surface detail or measure small features of a sample surface. DFP is better suited to resolving fine surface features on smaller samples, such as solder balls. However, the measurement resolution gets worse as FOV (field of view) increases

Devices Under Test

This study used four different samples, all smaller and thinner BGA style devices, aligning with the focus of this study. Each BGA is assigned a number, with sample details provided in Table 1. A deeper analysis was conducted on the BGA 1 samples to further refine the correlation between top and bottom warpage.

Table 1: Dimensions, ball diameter, and ball pitch of tested BGAs

	Dimensions (mm)	Ball Size (mm)	Ball Pitch (mm)
BGA 1	8.0 × 8.0 × 0.85	0.19	0.28
BGA 2	12.4 × 15.0 × 0.70	0.52	0.69
BGA 3	14.0 × 14.5 × 0.75	0.17	0.25
BGA 4	12.4 × 12.4 × 0.50	0.30	0.38

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Figure 1: Masking by pixel saturation of solder balls on BGA 1.

Analysis Methodology

BGAs were placed in an oven for 24 hours at 115 °C, prior to testing. Samples were analyzed using a thermal profile, where BGA 1 and 4 had a peak temperature of 230 °C, and BGA 2 and 3 had a peak temperature of 260 °C. Bottom surface measurements were performed on the Akrometrix AXP 2.0 measurement tool with a DFP 3 module, with resolution between 2–3 µm. Top side measurements were performed on an Akrometrix AXP 3, using a 300 lines per inch grating, with 0.5 µm resolution. All BGAs were supported on a piece of dark heat-resistant glass.

Samples were tested three times each with both DFP and SM to determine if there was any kind of degradation with repeat thermal runs. The results were observed to be consistent, starting and ending with the approximately the same coplanarity values. This would indicate the peak temperature used is not high enough to alter the sample.

Surface Brightness Processing of Ball Side Data Measured by DFP

This method looks to remove the solder balls by identifying them based on their grayscale values. Images are 12-bit, meaning the grayscale values range from 0 to 4095, or black to white. Prior to

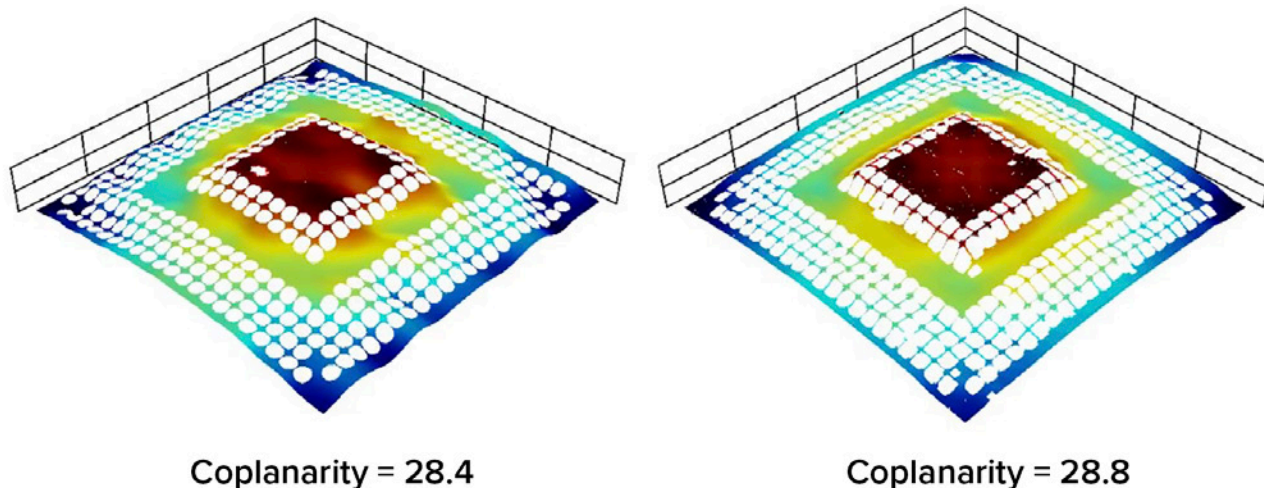


Figure 2: Processing using feature detection (left) vs. pixel saturation (right) of BGA 1.

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beginning an analysis, the surface brightness is adjusted to both illuminate the unpainted surface and saturate the ball pixels. Figure 1 shows a side-by-side comparison of a sample with saturated solder balls and the detection of their pixels. Attention should be given to the edges of the highlighted regions to notice the entire ball region is not selected. To account for this, the masked regions are expanded to remove the balls completely.

Once the balls are removed, further data processing is performed, including plane rotation, noise removal, and smoothing. Figure 2 shows a comparison of the same BGA at room temperature, painted and processed using a function known as feature detection, and not painted using the surface brightness feature. Feature detection is a software function that identifies repeating patterns based on height and shape, allowing them to be categorized automatically and, in this case, removed from the data set.

Unpainted Bottoms

Figure 3 shows the results for six of BGA 1, both in unpainted and painted conditions. Each line represents an average of three separate runs, with green indicating unpainted BGAs and red indicating painted BGAs. The two sets display a similar overall pattern. However, unpainted samples show a higher standard deviation, averaging $2.57\text{ }\mu\text{m}$, compared to $1.81\text{ }\mu\text{m}$ for painted samples. It was observed that the solder balls on the unpainted BGAs reflected light, creating secondary fringe patterns that increased noise in each measurement. While smoothing can help reduce some of this error, it does not fully eliminate it. The painted BGAs do not exhibit this issue because the solder balls' reflectivity matches that of the surface.

Digitally removing solder balls on the painted BGAs using the feature detection option took approximately three and a half hours, whereas solder ball removal on the unpainted BGAs using

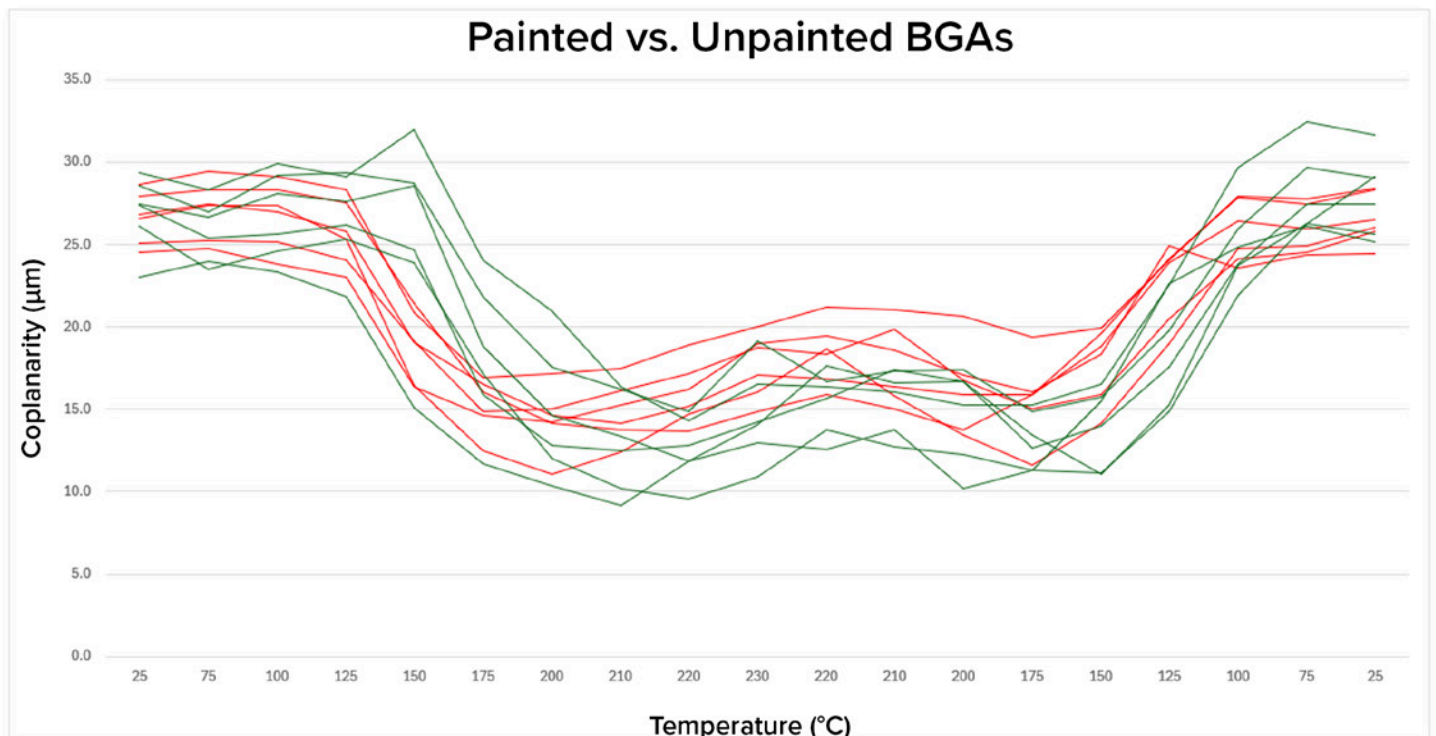


Figure 3: Coplanarity over temperature profile of painted (red) versus unpainted (green) for BGA 1.

surface brightness masking took less than 10 minutes. In other words, post-processing of the unpainted BGAs took less than 5% of the time needed for painted BGAs. Processing all acquisitions within a thermal profile can be done in a fraction of the time it would otherwise take.

Application Specific Approach

The removal of solder balls for BGA thermal warpage testing remains the industry standard, and no general recommendation is made here to replace this method for all sample types. A sample-specific threshold is needed to determine when these newly presented approaches are appropriate. Larger, thicker samples are expected to show greater mismatch between top and bottom shapes and have few issues with ball removal, making the standard approach effective. The samples in this study were selected for their package body thickness (0.50–0.85 mm) and serve as practical examples for the alternative method presented here. Thus, samples with less than 0.85 mm thickness are suggested as a starting point for these alternative methods, requiring additional industry feedback needed to refine guidelines. Additionally, a minimum solder ball size could serve as a rule for cases where effective ball removal becomes impractical.

Conclusion

Measuring unpainted BGAs with solder balls still intact offers a valid alternative to current methods, preserving sample integrity and avoiding surface damage that can occur with physical shearing of solder balls. As components continue to decrease in size, shearing may become impractical. Eliminating painting and extensive post-processing significantly reduces time, making surface brightness processing of unpainted BGAs an efficient alternative to analyzing painted ones. Further time savings can be achieved by eliminating both sample painting and post-processing of solder balls by focusing on measuring the top surface. **SMT007**

At Akrometrix, Neil Hubble is president, and Chris Gastaldo is a senior application engineer.



Neil Hubble



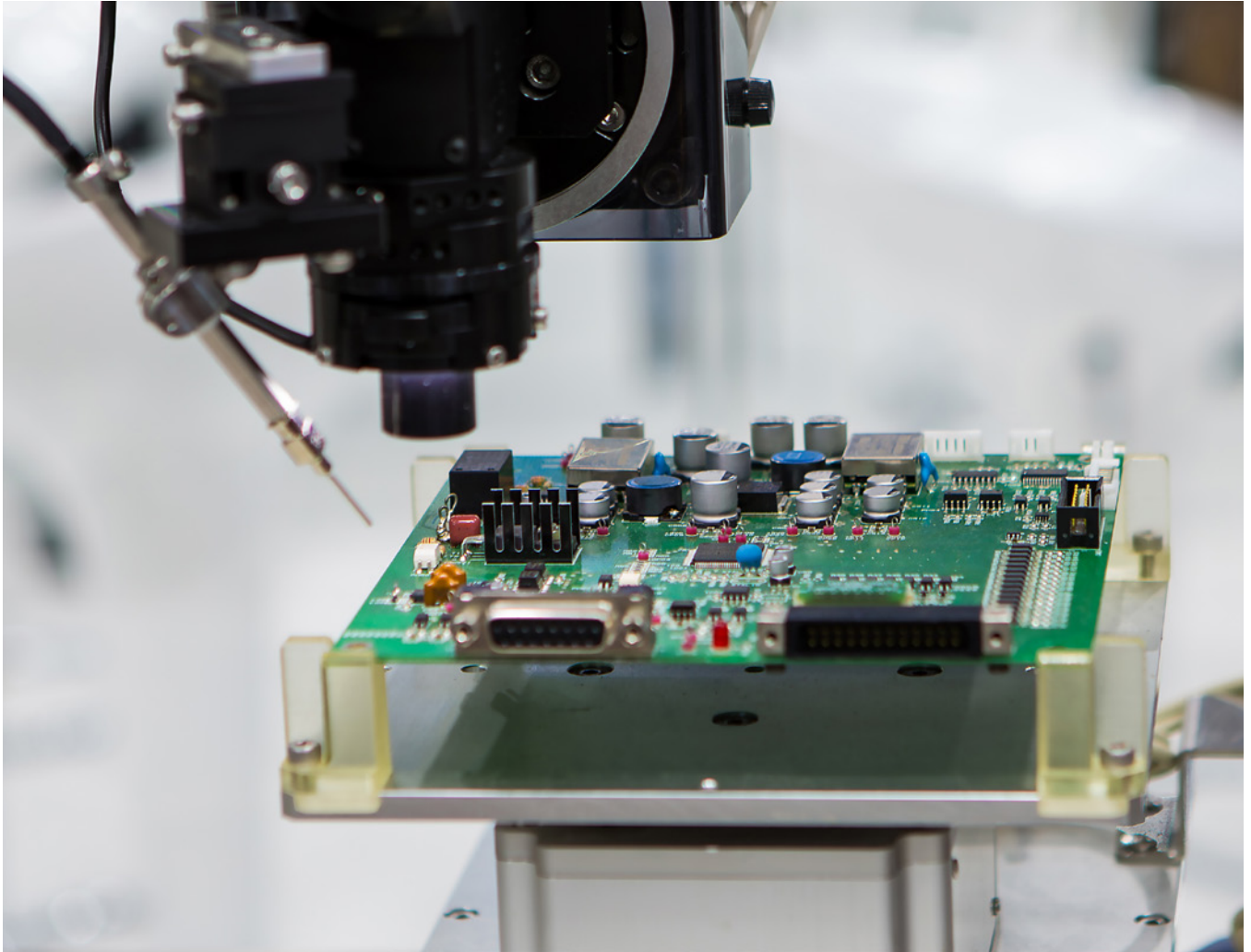
Chris Gastaldo

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Why Laser Soldering Gets So Much Attention



Production soldering techniques that persist on the shop floor each have their own unique advantages. For complete board assemblies with standard joints and built-in volume, convection reflow is a perennial choice. For through-hole joints, the solution is wave soldering. A relatively small number of solder joints may justify robotic or human hand soldering, but another soldering

technique that seems to be gaining prominence is laser soldering.

The advantages of laser soldering can be substantial, offering selective soldering, non-contact heating, localized thermal control, and access to joints that would otherwise be challenging for soldering irons, wave systems, and conventional reflow. But joint geometry, materials, optical

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Research suggests that selecting the best wavelength is not determined by the solder's specific melting temperature, but by how efficiently the light is absorbed by the joint's solder, pad, lead, and surface finish."

absorption, and production economics must all align to maximize the technology.

Still, why is laser soldering getting so much attention? It could be because rising board complexities are making it a requirement. Densely populated boards are more likely to have solder joints that cannot be reached by other well-established methods, such as wave soldering. Complexity also raises the possibility of conflicting heat requirements across the board. For example, connectors, plastic housings, and heat-sensitive components may make convection reflow a yield-crushing option. If only there were a way to deliver higher soldering temperatures in a precise, no-touch way, just to the spot where it's required. Laser soldering equipment manufacturers will tell you they have the answer.

At the heart of the system, naturally, is a laser beam focused on the solder joint, which absorbs the light and converts it into heat until the solder melts and forms the wetted joint. The soldering energy is applied precisely, heating only the solder joint; no other adjacent components experience any significant heat from the process.

Typically, near-infrared lasers (808–980 nm) are used as the working laser.¹ Recently, however, some systems have moved to a blue laser in the 450 nm range, as this wavelength often seems to have

better absorption efficiency. Occasionally, when jetting solder balls, high-powered Nd:YAG lasers (1064 nm) are employed.

Research suggests that selecting the best wavelength is not determined by the solder's specific melting temperature, but by how efficiently the light is absorbed by the joint's solder, pad, lead, and surface finish. This is where blue lasers are gaining traction, as they can reduce the energy required to reflect off metals. Infrared diode lasers, however, remain attractive because they are mature, economical, and widely available.

Laser soldering's value, which controls where, when, and how quickly heat enters an assembly, creates a narrower and more demanding process window. In addition, the number of performance parameters to optimize for laser soldering can be significant. This is both a strength and a potential weakness for laser soldering. For example, the amount of energy required may vary between individual solder joints. While this seems an easy requirement to accommodate, compared to, say, wave soldering, the parameters available add to the complexity (though those operators experienced with optimizing convection reflow profiles will see this as familiar territory).

Laser absorption parameters include:

- Beam diameter, shape, and energy distribution
- Focal distance and beam angle
- Laser power, ramp rate, and dwell time
- Thermal mass of the pad, lead, and connected copper
- Solder alloy, flux chemistry, and wire-feed rate
- Surface finish, contamination, and oxidation
- Part movement and positional tolerance
- Cooling rate and resulting intermetallic structure
- Use of cameras, pyrometers, and closed-loop power control

Keep in mind that the laser applies increasing heat while the beam is on. In contrast, a soldering iron tip applies energy at a steady temperature. Beam exposure time, therefore, becomes a critical parameter.

So, when is laser soldering a good option? Four examples might include thermal sensitivity, joint accessibility, traceability, and any follow-on work that cannot be done via wave or reflow.

Thermal Sensitivity

When key components or fragile substrates cannot survive reflow or wave soldering, the more precise methods become crucial. If the board design calls for a high-energy solder joint near a temperature-sensitive component or fixture, a laser is a good option. Laser soldering also finds a place when components on the board have reached their reflow cycling limits.

Another related situation occurs when work on the shop floor is high-mix, with reflow recipes rapidly swapping in and out. Switching to laser soldering may be a longer soldering process, but that might be offset by sidestepping the time it takes to stabilize the reflow oven to a new recipe.

Inaccessible Joints

While there are a variety of levels of inaccessibility, an obvious situation well suited to laser is when a joint resides inside a housing unreachable by a soldering iron.

Post-reflow Follow-on Work

We've already introduced the situation where components must be withheld until after reflow. Through-hole components, wires, terminals, and sensors all might create this situation.

Traceability

Laser soldering can be highly detailed about how and how much energy was delivered to each indi-

vidual joint, making traceability much more granular, a level of detail that wave or convection reflow cannot deliver.

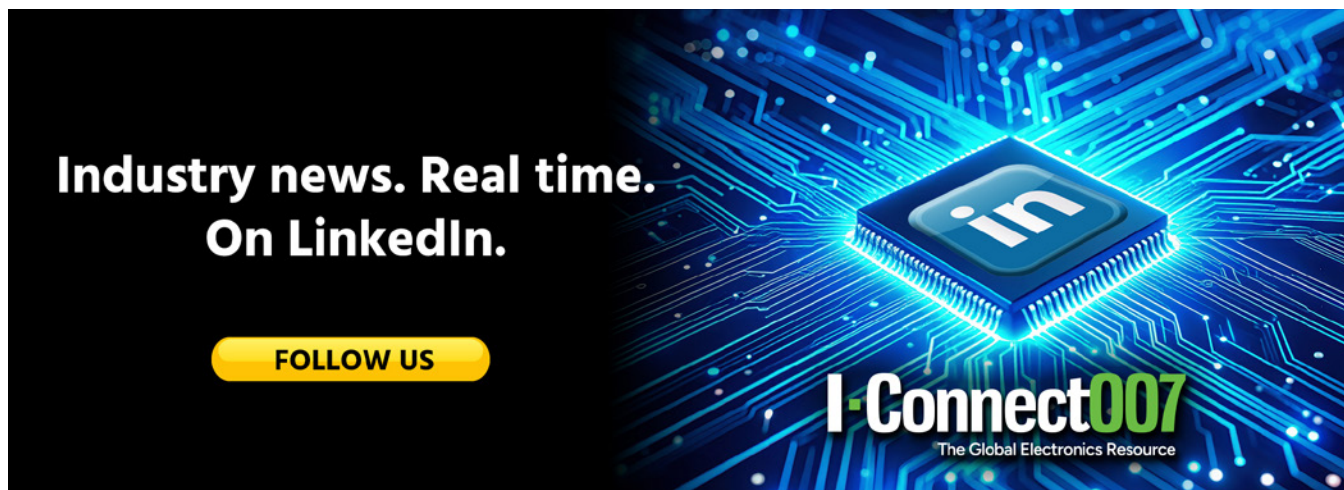
Of course, lasers aren't always the ideal soldering methodology. For example, boards built with beefy ground planes, busbars, etc., might dissipate thermal energy faster than the laser can apply it, causing cold solder joints. Copper, gold, silver, and tin absorb heat energy differently. Especially in silver's case, surface tarnish can also change the energy required. Position orientation and positional deviations can change how the laser hits the target joint, affecting energy transfer. This is also true of joints without a clear optical path. Finally, component, joint, solder, or board contamination can affect solderability. Ultimately, the laser can deliver the required heat to a solder joint; it cannot correct for poor solderability.

Conclusion

Perhaps above all else, laser soldering offers precision soldering; it is not a universal replacement for other soldering techniques. When high production volumes and low-complexity soldering converge, wave and reflow soldering continue to deliver high-throughput, affordable solutions. But as complexities increase, including higher densities and sensitive components, it stands to reason that laser soldering will meet the critical need for post-reflow soldering. **SMT007**

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When Does Reducing Silver Make Sense?

There is a single decision at the center of every die-attach conversation right now that isn't as much about chemistry as it is about control. This is most evident because silver prices have experienced significant volatility, evolving PFAS requirements are increasing regulatory and customer scrutiny, qualification windows are shrinking, and the packages that support AI, automotive, and power infrastructure must meet demanding performance and reliability requirements.

The engineer responsible for die attach material selection must balance all these requirements simultaneously: manage cost exposure, demonstrate reliability, address evolving compliance requirements, and protect throughput, while selecting the material

and process best suited to the applications.

That is a lot to put on a single bond line. When looking at silver, for example, instead of simply asking, "How can we reduce silver?" we should ask, "Where does a copper-based alternative make technical and commercial sense, and how do application requirements guide the decision?" Copper is already widely used in interconnects, lead frames, and substrate metallization. When engineered into a conductive die attach paste, it can provide the thermal, electrical, and mechanical characteristics required for appropriate applications while reducing exposure to silver-related cost volatility.

ATROX CD 560-1 is not a replacement for every silver application, but rather a copper-filler die-

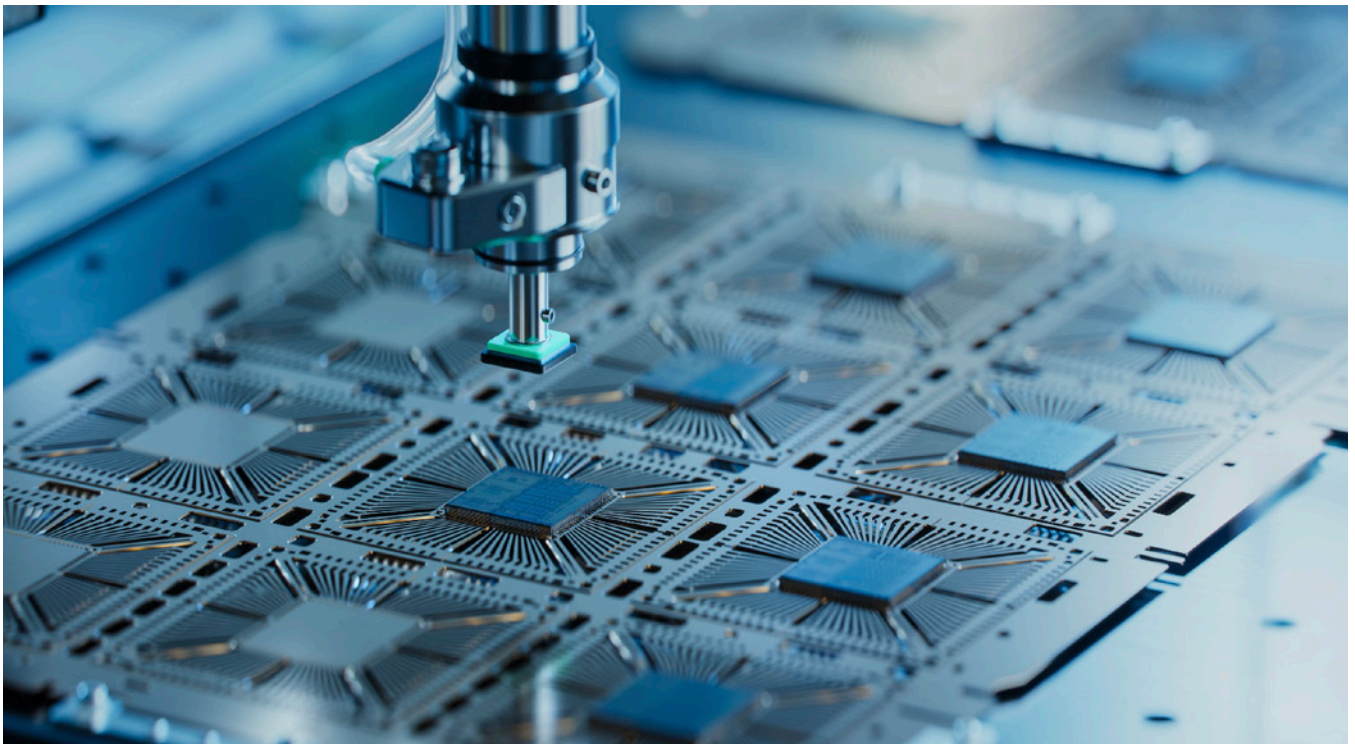


Figure 1: A close-up of a semiconductor packaging line during die attach, where a pick-and-place head positions a bare silicon die onto a lead frame substrate.

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attach technology for applications where it provides the right balance of performance, reliability, manufacturability, and cost. Silver-based technologies remain the appropriate choice where application and performance requirements demand them.

Let's look at what has happened with recent silver prices. In 2025, silver started at about \$30 an ounce. It rose 144% by the end of the year, finishing at over \$70, significantly outpacing gold.¹ Industrial consumption of silver had already reached record levels in 2024, with industrial demand totaling 680.5 million ounces and record consumption in electrical and electronics applications, including photovoltaic manufacturing.²

Silver remains strategically important in electronics and semiconductor manufacturing, with a broader industrial demand supported by structural growth in AI infrastructure, automotive applications, power-grid investment, and photovoltaics. According to the Silver Institute, global industrial silver demand reached 657.4 million ounces, or approximately 20,446 metric tons, in 2025.³

Silver pricing is influenced by both industrial demand and investment activity, contributing to the price volatility manufacturers may need to manage, a volatility profile that is more pronounced than copper's, where demand is predominantly industrial.⁴ Copper pricing is also subject to market fluctuations, but for suitable die-attach applications, switching to a copper filler material can reduce a manufacturer's direct exposure to silver price fluctuations.

For applications where copper meets the required package performance and process requirements, it can provide a pathway to reduce exposure to silver-price volatility. MacDermid's copper-filler die attach material was developed to reduce silver dependence while supporting the performance and manufacturing requirements of suitable metal lead frame packages.⁵

Qualification should therefore be driven not by commodity price alone, but by application requirements, process compatibility, and overall cost.

Volume Production Risk

A material like copper may look promising on a test coupon in the lab, but will that performance trans-

late to volume production? OSATs need field reliability data, not just supplier test results, so any new die attach chemistry must be qualified for production factors such as voiding, bleed-out, die tilt, and moisture sensitivity.

The copper-filler material is engineered for high-throughput automated dispensing on metal lead frame packages.⁶ The data points that matter for OSAT die attach reliability are the ones an OSAT can actually verify on its own equipment:

Dispensing stability: Viscosity of 10,000 centipoise (cps) at 25°C and 5 rpm, with a thixotropic index of 3.6, values that support consistent deposit shape, controlled tailing, low slump, and repeatable dispense weight over long runs.

Handling logistics: Pot life greater than 24 hours at 23°C and a 12-month shelf life at -40°C, meaning the material survives real production scheduling rather than demanding constant fresh batches.

Bond integrity: Die shear of 13.5 kg on copper and 13.0 kg on pre-plated frame (PPF) at 25°C, holding 3.5 kg and 3.0 kg respectively at 260°C (measured on a 2 x 2 mm bare silicon die, 175°C/1 hr cure)—numbers an OSAT can build a qualification plan around.

Reliability performance: Low outgassing and strong adhesion to both copper and PPF lead frames, which minimize contamination and support robust package reliability, including moisture resistance performance. An OSAT can qualify on its own package designs.

Thermal and electrical function: Bulk thermal conductivity of 2.5 watts per meter-Kelvin (W/mK) and volume resistivity of 0.0006 ohm-centimeters (ohm-cm).

The point is not that published material data is enough. It never is. The point is that this copper-filler material provides established material and process data, including dispensing characteristics, adhesion, thermal and electrical performance, that an OSAT can use as a starting point for package-

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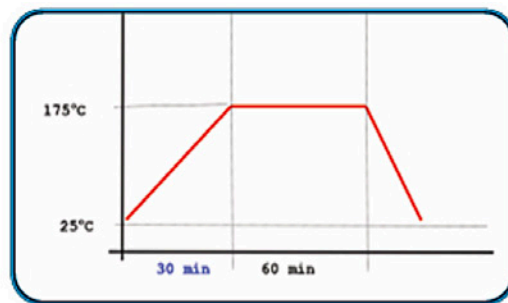
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Zone	1	2	3	4	5	6	7	Total Time (sec.)
Temp (C)	60	90	120	160	200	240	200	600

SNAP Cure Profile



Box Oven Cure Profile

Figure 2: Two die-attach cure temperature profile—a fast in-line “snap cure” ramping across seven zones in 600 seconds, and a slower “box oven” cure holding at 175°C for 60 minutes—used to set the bonding material during semiconductor assembly.

specific qualification. MSL-1 performance and zero delamination in lead frame packages, with final moisture sensitivity and reliability performance, requires validation for the customer’s specific package design and manufacturing process.

Compliance Requirements Increasing

U.S. and EU customers are increasingly seeking materials that address evolving PFAS requirements in major markets.

The U.S. Toxic Substances Control Act (TSCA) requires certain manufacturers and importers who manufactured or imported PFAS between 2011 and 2022 to report specified information to the EPA. There are also changing requirements at the state level, as Maine and Minnesota have adopted phased restrictions on products containing intentionally added PFAS. This includes broader prohibitions scheduled for 2032, subject to exemptions, determinations of currently unavoidable use, and other applicable provisions. Importantly for the semiconductor industry, Maine’s law includes exemptions for semiconductors, semiconductors incorporated into electronic equipment, and certain equipment and materials used in semiconductor manufacturing.

These distinctions illustrate why manufacturers must evaluate PFAS requirements by jurisdiction and application rather than assuming a single

regulatory pathway applies to the whole electronics industry. Even where exemptions apply to semiconductor manufacturing, regulatory scrutiny means manufacturers must better understand the PFAS used in their operations and supply chains, including associated sourcing and documentation requirements.⁷

In the EU, ECHA’s Risk Assessment Committee (RAC) and Committee for Socio-Economic Analysis (SEAC) have advanced the proposed EU-wide PFAS restriction under REACH, including consideration of targeted derogations and transition measures. The European Commission, in consultation with EU Member States, will determine the final restriction following completion of ECHA’s scientific evaluation,⁸ which addresses PFAS uses across a wide range of applications, with targeted derogations considered where supported by evidence on alternatives, costs, and benefits.⁹

Materials developed with zero added PFAS may provide manufacturers with an additional option when evaluating future material, compliance, and product stewardship requirements.

ATROX CD 560-1 is formulated with zero added PFAS, consistent with the product’s approved technical documentation. It is designed to support high-throughput manufacturing using established die-attach processing approaches. The material is compatible with time-pressure dispensing systems commonly

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used on die bonders and offers both box-oven and snap-cure options, helping manufacturers evaluate a zero-added-PFAS material without requiring a fundamentally different dispensing process.

For manufacturers considering alternative die-attach materials, this combination can help reduce the process disruption associated with qualification while allowing throughput, equipment compatibility, and reliability to be validated under their specific production conditions.

When the next customer disclosure request arrives, the engineer who has already qualified this copper-filled material can respond with a documented zero added PFAS formulation supported by appropriate product compliance documentation, rather than having to react to a new materials requirement, and that level of preparedness is valuable with a PFAS regulatory environment.¹⁰

Qualification Risk Affects the Entire Supply Chain

New materials must pass the full qualification cycle without negatively impacting throughput, yield, or equipment uptime, yet it seems that qualification is where good materials go to get delayed. A new die attach chemistry can meet every spec and still fail if it demands exotic processing, unfamiliar tooling, or an elaborate test plan that eats up the project timeline. The engineer’s goal is straightforward: Pass the qual cycle without losing throughput,

yield, or equipment uptime. This copper-filler material makes that path familiar rather than novel. Its low resin bleed-out (RBO) and low outgassing characteristics help minimize contamination and support reliable processing. Its dispensing rheology is optimized for high-throughput automated dispensing with minimal machine downtime, while box-oven and snap-cure capability provides flexibility to select a cure approach suited to the package and manufacturing process. Compatibility with time-pressure pump systems used on most die bonders can also help facilitate integration into established production environments.

A responsible qualification plan should still measure more than room-temperature die shear: deposit geometry, bondline thickness, void fraction, acoustic microscopy before and after stress, moisture sensitivity, elevated-temperature die shear, thermal resistance, and failure mode. These all belong in the record, but the difference is that this material can be evaluated through that plan using standard equipment.

The engineer who qualifies ATROX is not signing up for an untested science project. They are starting with established material and process data, then using those published parameters as a basis for package-specific qualification and validation within their own equipment and manufacturing conditions.

Table 1: The qualification cycle is one an engineer already trusts

Stage	Key Question	Evidence
Material screening	Does the material meet thermal, electrical, rheological, storage, and cure requirements?	Technical data, handling review, compatibility screening
Process development	Can the line produce stable deposits and bondlines?	Dispense capability, bondline measurement, void mapping, cure profiling
Package qualification	Does the package survive assembly and reliability stress?	Die shear, moisture sensitivity, reflow, acoustic microscopy, cross-sections, thermal and electrical testing
Production release	Can performance hold across time, sites, and suppliers?	Control plan, acceptance limits, change control, traceability, customer documentation

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02

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03

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04

DEPENDENT ON SPREADSHEETS

Critical data lives outside the system, relying on manual effort and tribal knowledge.

05

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In-Region Support Provides Added Comfort for an Engineer

In-region application engineering support can be critical to successful qualification, yet this concern is least discussed and most decisive. A material that works only when a distant applications engineer is available to fly in will not survive a production ramp. In high-volume semiconductor assembly, when a die attach issue appears on the line—a dispense anomaly, a cure-window shift, or a bond-line surprise—the clock is measured in hours, not weeks. If the only technical support is a time zone away, the qualification stalls and the line bleeds.

The choice of supplier becomes as important as the choice of chemistry. A silver-reduction program only succeeds when the material partner can stand on the factory floor with application engineering that understands the OSAT's line, the customer's qualification timeline, and the specific package architecture in front of them. This does not need to be a luxury. It is the prerequisite for converting a promising material into a production-qualified one.

MacDermid Alpha Electronics Solutions' die attach portfolio is backed by a global support footprint that includes in-region Asia application engineering, the kind of presence that turns a datasheet into a qualified, running process. The engineer who chooses it is choosing a partner who can be in the assembly facility when the problem arises, not on a conference call about it.

One Decision, Three Wins

The thread running through these five industry concerns, including price, supply-chain quality, PFAS, and technical support, is that the ATROX copper-filled offering addresses these challenges through a single material solution. For applications that meet the required thermal, mechanical, and process requirements, copper can provide an alternative to reduce dependence on silver. It is already widely used across semiconductor packaging in interconnects, lead frames, and substrate metallization, giving engineers a familiar material platform to work with. Its thermal conductivity, mechanical properties, and structural stability make it well-suited to selected die-attach applications, while its use as an alternative filler can also help reduce exposure to silver-price volatility.

An engineer can reduce silver dependence

without compromising the application's reliability requirements by selecting the material system best suited to each package. Silver remains an important choice where its properties and performance are required, while copper-filler alternatives offer another pathway for applications that meet the necessary thermal, electrical, mechanical, and process requirements. **SMT007**



Senthil Kanagavel is director of standard die attach at MacDermid Alpha Electronics Solutions.

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More Reference Tables



Table 2: Material-selection framework for silver-reduction programs

Package Requirement	Candidate Material Class	Process Evidence	Reliability Evidence	Documentation
Thermal load, current density, die size, bondline target, and surface finish	Copper-filler paste, alternative conductive paste, hybrid sinter, silver sinter, or solder	Dispense repeatability, bondline control, cure profile, voiding, bleed-out, and contamination	Die shear, moisture sensitivity, delamination, thermal resistance, electrical continuity, and cycling	PFAS position, substance declaration, regional status, traceability, and change control

Table 3: Selected published properties for ATROX CD 560-1

Attribute	Published Value
Positioning	Zero-added-PFAS copper-filled conductive die attach paste for metal lead frame packages
Viscosity	10,000 cps at 25°C and 5 rpm
Thixotropic index	3.6
Pot life	Greater than 24 hours at 23°C
Shelf life	12 months at -40°C
Bulk thermal conductivity	2.5 W/mK
Volume resistivity	0.0006 ohm-cm
Cure options	175°C for 60 minutes in a box oven or a 10-minute snap-cure profile
Representative copper die shear	13.5 kg at 25°C; 3.5 kg at 260°C
Representative PPF die shear	13.0 kg at 25°C; 3.0 kg at 260°C
Source: ATROX CD 560-1 Technical Data Sheet, Issue 15 July 2025.	

Table 4: Qualification checklist for alternative die attach programs

Stage	Key Question	Recommended Evidence
Material screening	Does the material meet thermal, electrical, rheological, storage, and cure requirements?	Technical data, handling review, and compatibility screening
Process development	Can the line produce stable deposits and bondlines?	Dispense capability, bondline measurement, void mapping, and cure profiling
Package qualification	Does the package survive assembly and reliability stress?	Die shear, moisture sensitivity, reflow, acoustic microscopy, cross-sections, and thermal and electrical testing
Production release	Can performance be maintained across time, sites, and suppliers?	Control plan, acceptance limits, change control, traceability, and customer documentation

Table 5: Cure profile specifications for ATROX CD 560-1

Profile Type	Zone / Stage	Temperature	Dwell Time	Total Time
Snap cure	Zone 1	60°C	—	—
Snap cure	Zone 2	90°C	—	—
Snap cure	Zone 3	120°C	—	—
Snap cure	Zone 4	160°C	—	—
Snap cure	Zone 5	200°C	—	—
Snap cure	Zone 6	240°C	—	—
Snap cure	Zone 7	200°C	—	600 sec.
Box oven cure	Single stage	175°C	60-minute cure hold	60 min - Additional ramp and controlled cooling required

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Interposer Rework and Precision Solder Ball Attachment

BY NASH BELL, BEST, INC.

An interposer is a thin substrate positioned between a semiconductor device, such as a BGA and PCBA. It contains conductive features that allow electrical connections to be rerouted, recreated, or modified between the component and the PCB.

Interposers may be manufactured from organic materials such as polyimide or FR-4, as well as silicon, glass, or other specialized materials. In PCB rework, they are most commonly used when the existing board design cannot easily be modified through conventional rework techniques.

Advantages and Limitations

Interposers can provide several important benefits:

- Allows an existing PCBA to be modified or upgraded without a full board redesign
- Eliminates the need to replace an expensive multilayer PCB in certain applications
- Permits connections to be rerouted when pads, traces, or internal connections are damaged or inaccessible
- Supports engineering change orders or component substitutions without requiring a new PCB revision
- Provides a practical option for prototype development and low-volume modifications

The tradeoff is additional complexity. An interposer

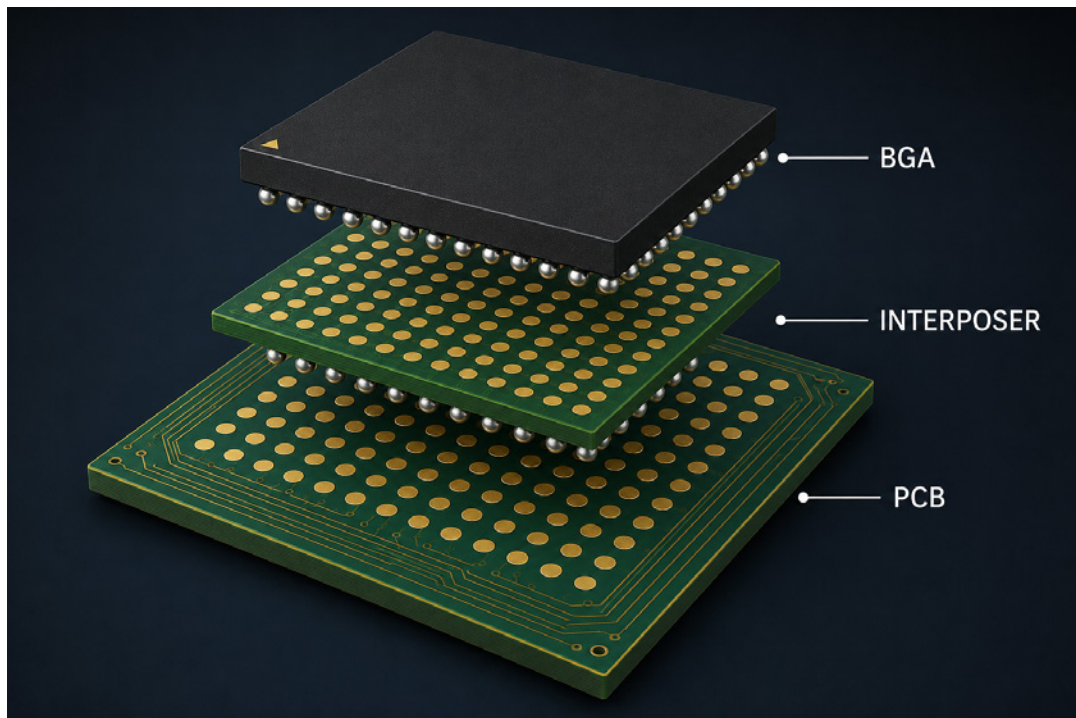


Figure 1: Typical BGA mounted to an interposer above the PCB.

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KNOCKING DOWN THE BONE PILE

introduces another substrate, added solder joints, increased stack height, tighter alignment requirements, and new thermal considerations. It can also affect signal integrity or impedance in high speed applications if not properly engineered.

Common Applications

Interposers are most useful when conventional BGA rework or localized board repair is not practical, reliable, or cost-effective. They provide another way to modify the electrical path between a component and the PCB without redesigning the complete assembly.

Common uses include:

- Bypassing damaged internal vias or connections near a BGA footprint
- Implementing engineering change orders that require signal rerouting
- Adapting an existing PCB to a replacement component with a different pinout or connection scheme
- Recovering high-value assemblies where replacing the PCB would be difficult or prohibitively expensive
- Supporting prototype modifications and design validation without committing to a new PCB revision

Interposers are also used in semiconductor packaging as an intermediate routing layer between one or more integrated circuit dies and the package substrate. Organic materials such as FR-4 and polyimide are common in board-level or flexible applications, while silicon and glass are more closely associated with advanced packaging requiring very high interconnect density or demanding electrical performance.

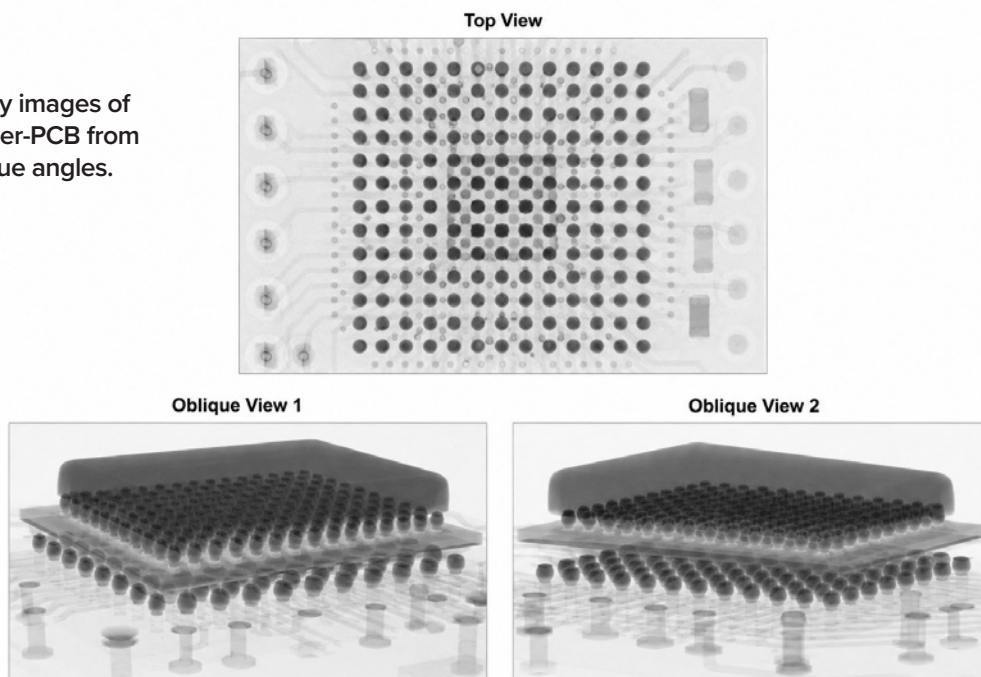
Interposer Rework

At the board level, interposer rework is used when a conventional BGA removal-and-replacement process does not adequately address the electrical or mechanical requirements of the assembly. The interposer is introduced between the BGA and the PCB to reroute connections, accommodate design changes, or create an alternative interface between the component and its original footprint.

A typical process may include:

- Remove the BGA using a controlled hot-air or infrared rework process.
- Clean and inspect the original PCB footprint
- Re-ball the BGA or interposer if required
- Prepare the PCB and interposer for assembly
- Apply solder paste or flux as required

Figure 2: X-ray images of BGA-interposer-PCB from top and oblique angles.





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- Precisely align and attach the BGA to the interposer
- Align the completed BGA/interposer stack to the PCB
- Reflow using a developed thermal profile

Inspect the completed assembly using X-ray, including oblique views when necessary, along with visual and electrical or functional testing as applicable.

Because the interposer adds another substrate and solder interface, thermal profiling becomes particularly important. The additional material affects heat transfer, temperature uniformity, and the time required for each solder interface to reach the desired temperature.

Using Mixed Alloys to Control Reflow

One useful strategy is to use different solder alloys at the two interconnect levels. This staged approach is often referred to as step soldering because the

assembly sequence takes advantage of alloys with different melting temperatures.

For example, the BGA can first be attached to the interposer using a lead-free alloy such as SAC305, which has a liquidus temperature of approximately 217°C. The completed BGA/interposer assembly can then be attached to the PCB using eutectic tin-lead solder, which melts at 183°C.

The second reflow profile can therefore be developed to fully reflow the lower-temperature tin-lead interface while keeping the upper lead-free BGA-to-interposer joints below their liquidus temperature. This reduces the likelihood of remelting the first solder interface during final attachment and helps preserve component alignment and solder-joint geometry.

This is particularly useful after the BGA and interposer have already been aligned and inspected as a subassembly. Instead of subjecting both interfaces to another complete high-temperature reflow cycle, the second process can be focused on forming the

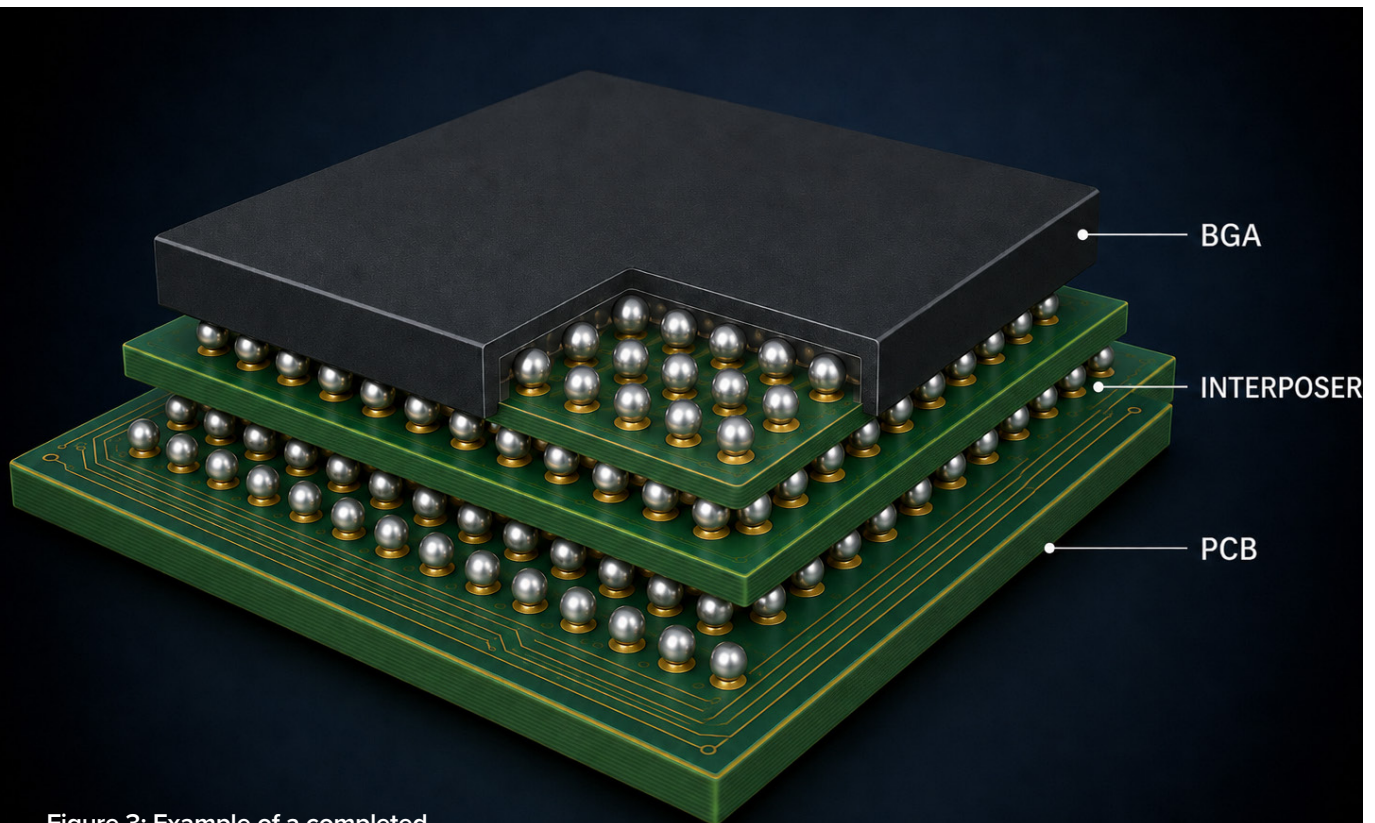
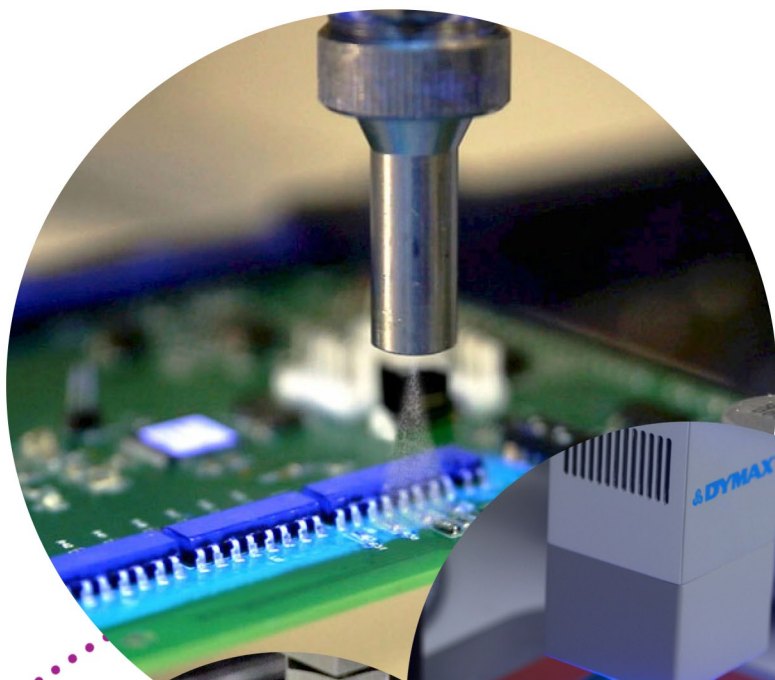


Figure 3: Example of a completed BGA-interposer-PCB stack.



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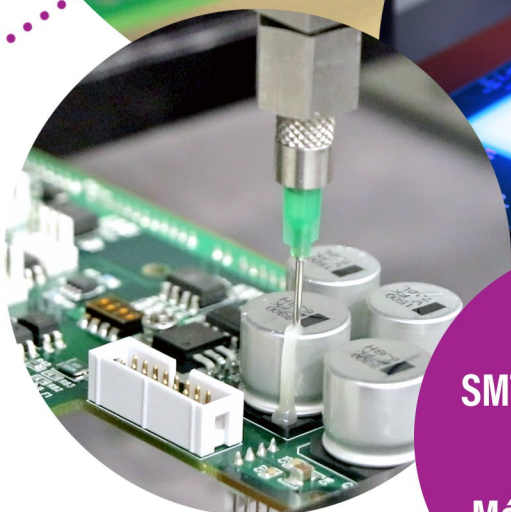


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interposer-to-PCB joints.

Careful thermal characterization is still essential. Thermocouples should be used to verify temperatures at both interfaces because the actual solder-joint temperature will depend on the component, interposer construction, PCB thermal mass, heater configuration, and dwell time. The key benefit is the ability to control the two soldering events independently rather than repeatedly bringing both interfaces through liquidus.

X-ray Inspection Challenges

Interposer assemblies can also be more difficult to evaluate using X-ray inspection than a conventional BGA installation. Because the assembly contains multiple vertically stacked solder-ball interfaces, the upper and lower solder joints may overlap in the X-ray image, making it harder to isolate and evaluate an individual connection.

This overlap can make defects such as opens, bridging, voiding, or inconsistent joint formation more difficult to interpret from a single top-down image. Oblique-angle X-ray inspection can help separate the interfaces visually, but the effectiveness of the inspection depends on the interposer design, ball pitch, material density, and capabilities of the X-ray system.

Equipment Commonly Used

Depending on the assembly, interposer rework may require:

- Precision hot-air or infrared BGA rework equipment with bottom-side heating
- Optical alignment and component-placement capability
- PCB preheating equipment
- Reballing fixtures and stencils
- Solder paste, solder spheres, and flux compatible with each interface
- Interposer alignment or support fixtures
- Stereo microscopy
- X-ray inspection
- Thermocouples and profiling equipment

Alternatives to Interposer Rework

An interposer should not automatically be considered the preferred solution for every BGA-related failure. Depending on the failure mode, board construction, reliability requirements, and assembly value, a simpler repair may be more appropriate.

Alternatives can include bonded replacement pads, jumper-wire repair to an accessible trace or via, PCB trace repair, conventional BGA removal and replacement, or complete PCB replacement when the damage or risk is too extensive to justify repair.

Conclusion

Interposer rework provides an additional option when conventional BGA rework, localized PCB repair, or board replacement does not adequately address the needs of an assembly. It can be especially valuable for high-cost electronics, difficult-to-replace multilayer PCBs, engineering changes, prototype modifications, and specialized advanced-packaging applications.

The process also introduces additional solder joints, alignment requirements, thermal considerations, and inspection challenges. For that reason, interposer rework should be approached as an engineered process rather than simply an extension of standard BGA rework.

The interposer design, alloy selection, reflow sequence, thermal profile, inspection method, and reliability requirements should all be evaluated together before the repair strategy is finalized.

When properly designed and controlled, an interposer can provide a practical way to recover valuable hardware, implement difficult design changes, and extend the useful life of assemblies that might otherwise require replacement. **SMT007**



Nash Bell is president of BEST, Inc. To read past columns, [click here](#).

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IPC Standards Released for Q3 2026



Each quarter, the Global Electronics Association releases a list of standards that are new or have been updated. To view a complete list of newly published standards and standards revisions, translations, proposed standards for ballot, final drafts for industry review, working drafts, and project approvals, visit electronics.org/ipc-standards.

These are the latest releases for Q3 2026.

IPC-6013F, Qualification and Performance Specification for Flexible/Rigid-Flexible Printed Boards

IPC-6013F covers qualification and performance requirements for flexible printed boards designed to IPC-2221 and IPC-2223 and utilizing materials qualified to the IPC-420X series. The flexible printed board may be single-sided, double-sided, multilayer, or rigid-flex multilayer. All these construc-

tions may include stiffeners, PTHs, microvias, and blind/buried vias. Revision F incorporates new and updated requirements for rigid-to-flex transition zones, printed board edge plating, printed board cavities, dewetting, copper penetration as a function of wicking, etchback, and hole formation, and also minimum dielectric spacing.

IPC-2591 V2.1, Connected Factory Exchange (CFX)

IPC-2591 V2.1 standard establishes the requirements for the omnidirectional exchange of information between manufacturing processes and associated host systems for assembly manufacturing. This standard applies to communication between all executable processes in the manufacture of printed board assemblies, whether automated, semiautomated, or manual, and to related mechanical assembly and transactional processes. IPC-2591, Version 1.7, includes enhancements for closed-loop between AOI and SPI, and fields added to Heartbeat to provide repeated active fault and recipe information in each message. Visit www.ipc-cfx.org for software developer resources, training programs and information on the IPC-CFX-2591 Validation System and Qualified Products List (QPL).

IPC-Hermes-9852 V1.7, The Global Standard for Machine-to-Machine Communication in SMT Assembly

IPC-Hermes-9852 V1.7 standard is an open, vendor-neutral standard that replaces the legacy SMEA

interface to enable seamless board-handover communication between machines on an SMT assembly line. By transmitting rich product and process data alongside the physical handoff, it eliminates manual setup errors, reduces changeover times, and serves as a foundational building block for factory automation.

IPC J-STD-002F, Solderability Tests for Component Leads, Terminations, Lugs, Terminals, and Conductors

IPC J-STD-002F prescribes test methods, defect definitions, acceptance criteria, and illustrations for assessing the solderability of electronic component leads, terminations, solid wires, stranded wires, lugs, and tabs. The IPC-J-STD-002E standard also includes a test method for the resistance to dissolution/dewetting of metallization. IPC-J-STD-002F is intended for use by both supplier and user. The IPC-J-STD-002F standard was developed by ECIA, IPC and JEDEC.

IPC-4105, Specification for Metal Base Copper Clad Laminates for Rigid Printed Boards

IPC-4105 is a new document that covers the requirements for metal-base materials that are referred to as metal-based laminate listed in the specification sheets that are contained in the list of the main body. These are to be used primarily for rigid and multilayer printed boards for electronic interconnections. **SMT007**

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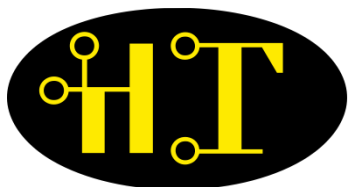
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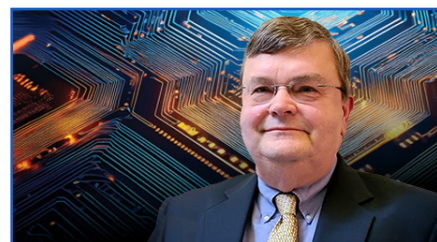
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is published by IPC Publishing Group, Inc.,
3000 Lakeside Dr., Suite 105N, Bannockburn, IL 60015

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October 2026, Volume 42, Number 10
SMT007 MAGAZINE is published monthly,
by IPC Publishing Group, Inc., dba I-Connect007.

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